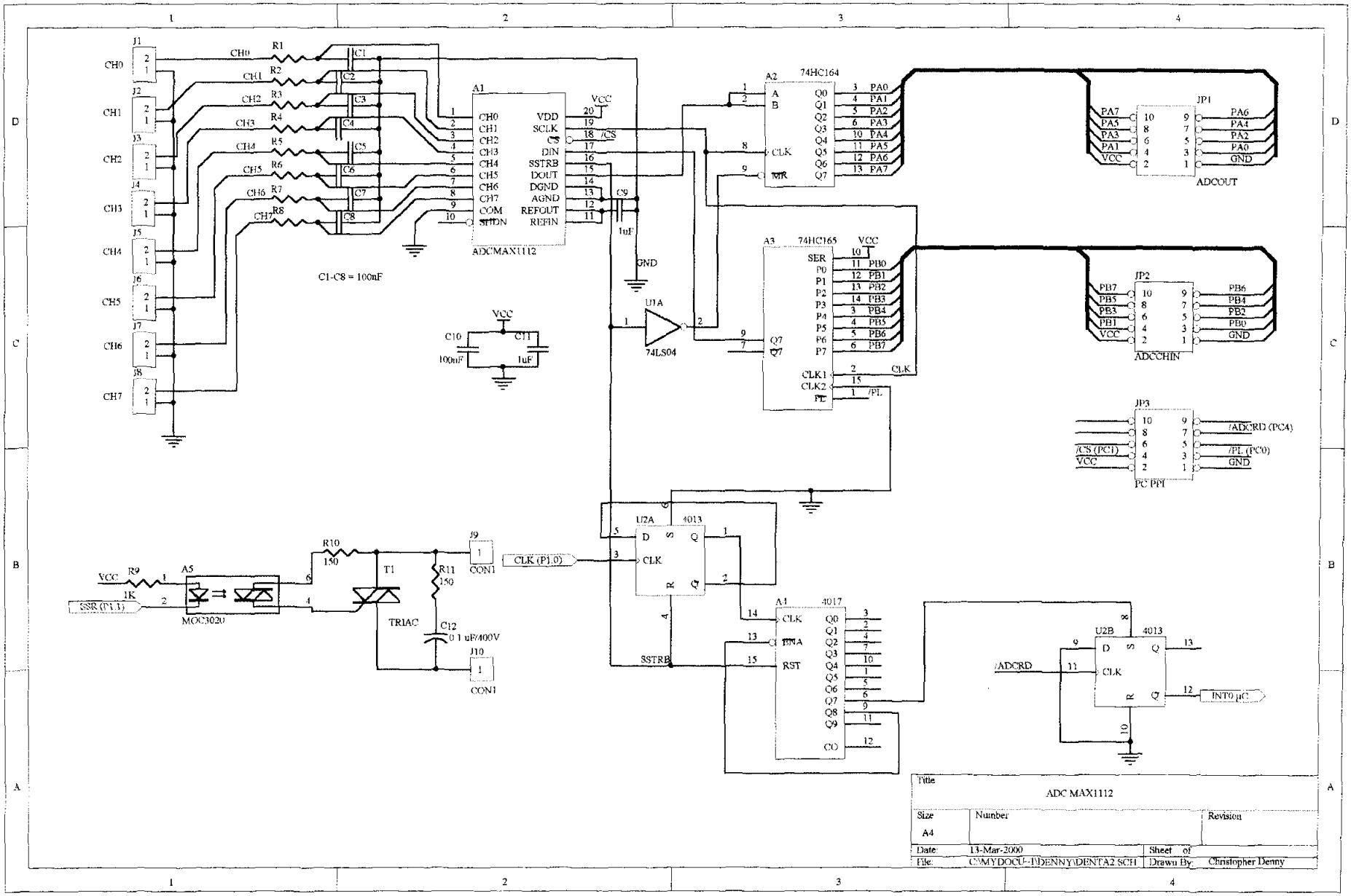
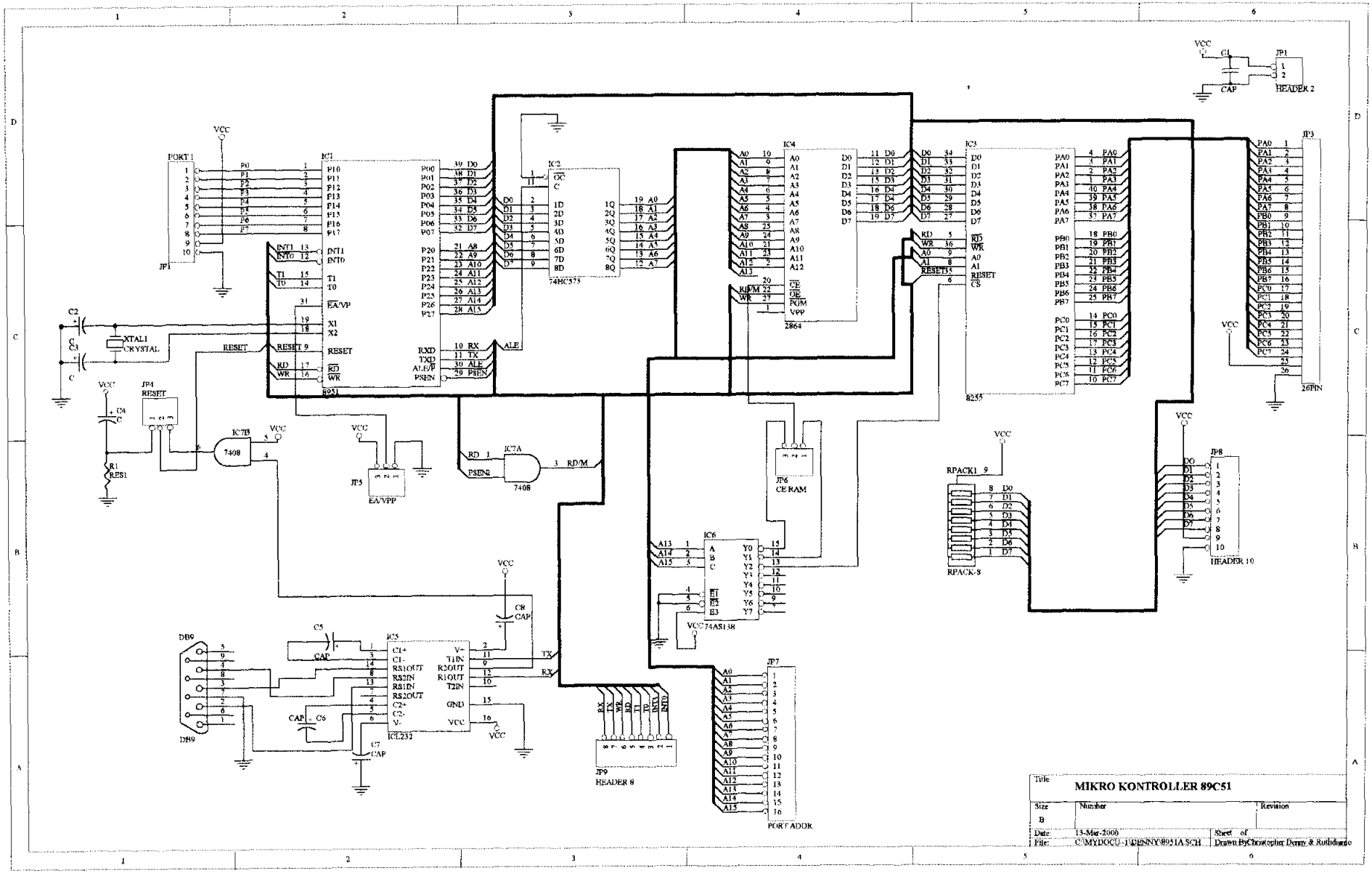

J1
CH0
R1
C1
A1
ADCMAX1112
VCC
GND
C9
1uF
/CS
C1-C8 = 100nF
A2
74HC164
A3
74HC165
U1A
74LS04
JP1
ADCOUT
JP2
ADCCHIN
JP3
PC PPI
/ADCRD (PC4)
/CS (PC1)
/PL (PC0)
C10
100nF
C11
1uF
U2A
4013
U2B
4013
A4
4017
R10
150
R11
150
T1
TRIAC
C12
0.1 uF/400V
R9
1K
A5
MOC3020
SSR (P1.3)
J9
CON1
J10
CON1
CLK (P1.0)
SSTRB
/ADCRD
INT0 µC
Title
ADC MAX1112
Size
A4
Number
Revision
Date:
13-Mar-2000
Sheet of
File:
C:\MYDOCU~1\DENNY\DENTA2.SCH
Drawn By:
Christopher Denny


MIKRO KONTROLLER 89C51
Size B
Number
Revision
Date: 13-Mar-2000
File: C:\MYDOCU~1\DENNY\8951A.SCH
Sheet of
Drawn By:Christopher Denny & Rutilidarto
8951
74HC573
2864
8255
74AS138
ICL232
7408
CRYSTAL
RESET
HEADER 2
HEADER 10
HEADER 8
26PIN
RPACK-8
CE RAM
EA/VPP
PORT ADDR

# LAMPIRAN III : LISTING PROGRAM

## 1. LAMPIRAN PROGRAM UTAMA DALAM BAHASA ASEMBLER.

```
PA          EQU   4000H
PB          EQU   4001H
PC          EQU   4002H
PCW         EQU   4003H
CW          EQU   0090H

DPA         DATA  0021H
DPB         DATA  0022H
DPC         DATA  0022H
I           DATA  0023H
SENSOR          DATA    0024H

;----------------------------
;     PROGRAM MEMORY
;----------------------------
            .CODE
            ORG   2000H

            MOV   R2,#0FFH
Del1        MOV   R3,#0FFH
            DJNZ  R3,$
            DJNZ  R2,Del1

            AJMP  Start

            ORG 2100H

;     --------------------
;     Initialization Proc.
;     --------------------
;           -----------
;           Init. Timer
;           -----------
Init        MOV   TMOD,#00100010B         ;T1 mode2, T0 mode2
            MOV   TL1,#0FAH          ;T1 mode2 generate BR=9600 Bps
            MOV   TH1,#0FAH
            MOV   TCON,#01000000B         ;T1 on,T0 off

;           ------------
;           Init. Serial
;           ------------
            MOV   SCON,#01010000B         ;Mode1,REN
            MOV   PCON,#80H          ;SMOD=0

;           --------------
;           Init Interrupt
;           --------------
            MOV   IE,#00000000B
            RET
```

```
sclk
            MOV   R2,#80H
            DJNZ  R2,$
            RET

;--------------------------------
;     MAIN PROGRAM LOCATION
;--------------------------------
Start
            MOV   P1,#00H
            MOV   SP,#40H
            MOV   IE,#00H
            ACALL Init

;--------------------------------
;       INISIALISASI PPI
;--------------------------------

            MOV   DPTR,#PCW
            MOV   A,#CW
            MOVX  @DPTR,A

;--------------------------------
;     ULANG
;--------------------------------
                MOV     A,#00H
                MOV     P1,A
                MOV     DPA,#00H  ; kondisi awal Port A
                MOV     DPC,#00H  ; Kondisi awal Port C

ULANG
                MOV     A,#255
                MOV     SBUF,A
                JNB     TI,$
                CLR     TI

            MOV   DPB,#8FH  ; AKTIFKAN CHENEL 0
            MOV   DPTR,#PB
            MOV   A,DPB
            MOVX  @DPTR,A

            ACALL CLKADC
            JNB   TI,$
            CLR   TI

            MOV     DPB,#0CFH
            MOV   DPTR,#PB
            MOV   A,DPB    ; AKTIFKAN CHENEL 1
            MOVX  @DPTR,A

            ACALL CLKADC
            JNB   TI,$
            CLR   TI

            CLR     P1.1
            MOV   A,SBUF
```

```
            JNB   A.0,HIDUP
            CLR   P1.1
            AJMP  MATI

HIDUP       SETB  P1.1
            CLR   RI
            AJMP  ULANG

MATI        CLR   RI

            AJMP  ULANG

CLKADC            MOV   DPTR,#PC
            MOV   A,#00H    ; PL = 0
            MOVX  @DPTR,A
            MOV   DPTR,#PC
            MOV   A,#01H    ; PL = 1
            MOVX  @DPTR,A

            MOV   I,#08H        ; CLOCK 8 KALI
CLOCK1            CLR   P1.0
            ACALL       SCLK
            SETB  P1.0
                ACALL   SCLK
            DJNZ  I,CLOCK1

                MOV     DPTR,#PA
            MOVX  A,@DPTR
            MOV   DPA,A
            MOV     SBUF,DPA

            MOV   I,#02H        ; CLOCK 2 KALI
CLOCK2            CLR   P1.0
            ACALL       SCLK
            SETB  P1.0
                ACALL   SCLK
            DJNZ  I,CLOCK2
            RET
END□
```

## 2. PROGRAM PENGOLAHAN DATA DAN TAMPILAN SUHU DALAM BAHASA PASCAL

```
PROGRAM TAMPILAN_SUHU;
uses crt,dos,GRAPH;
const RX_Buffer      = $2F8;      { RX Buffer COM2 }
      TX_Buffer      = $2F8;      { TX Buffer COM2 }
      Int_Enbl_Reg   = $2F9;      { Interrupt Enable Register }
      Int_Iden_Reg   = $3FA;      { Interrupt Indentification
Register }
      Line_Cont_Reg  = $2FB;      { Line Control Register }
      Modem_Cont_Reg = $2FC;      { Modem Control Register }
      Line_Stat_Reg  = $2FD;      { Line Status Register }
      Modem_Stat_Reg = $2FE;      { Modem Status Register }
      Gray10  : FillPatternType = ($AA, $AA, $AA, $AA, $AA, $AA,
$AA, $AA);
type
     complex = record
                a,b   : real;
                c,d   : byte;
               end;

var   data10,input   : array [0..1023] of integer;
      T,L  : array [0..550]   of REAL;
      vT,vL  : array [0..550]   of byte;
      gain    : array [0..99]   of word;
      Int0C_Save : pointer;     {interrupt service routine IRQ3 }
      i,data,S : byte;
      regs: registers;
      Grdriver,Grmode: integer;
      dummy : byte;
      TERMO,LM,LM1,M: real;
      tegangan:real;
      DATA0,DATA1,FLAG:BYTE;
      fil     : file of complex;
      dat     : complex;
      n,x: word;
      tempx, tempy: word;


procedure Intr_Com;  interrupt;
begin
     data:=port[RX_Buffer];       { baca buffer RX }
     port[$20]:=$20;              { End Of Interrupt 8259 }
     IF DATA=255 THEN FLAG:=0;
     CASE FLAG OF
     0 : FLAG:=1;
     1 : BEGIN
              FLAG:=2;
              DATA0:=DATA;
              TERMO := ( data0*0.595041)+28;
              END;
     2 : BEGIN
              FLAG :=0;
```

```
                DATA1:=DATA;
                LM    :=   ( DATA1*0.6603) - 55.849057;
                END;
      END;

end;

Procedure Open_Com;
var   dummy : byte;
begin
    GetIntVec($0B,Int0C_save);
    SetIntVec($0B,Addr(Intr_com));

port[Line_Cont_Reg ]:=$80;    { D7=1 set baud rate 9600 bps}
port[TX_Buffer     ]:=$0B;    { divisor LSB  $2F8=$0B }
port[Int_Enbl_Reg  ]:=0;      { divisor MSB  $2F9=0 }
port[Line_Cont_Reg ]:=$03;    { 8 bit data, 1 stop bit, no parity }
port[Int_Enbl_Reg  ]:=$01;    { enable interrupt saat ada data RX }
port[Modem_Cont_Reg]:=$09;    { D0 = DTR = 0 => 89C51= Reset    }
dummy:=port[RX_Buffer];        { kosongkan RX buffer }
port[$21]:=port[$21] and $F7; { Enable IRQ3 }
end;

Procedure Close_Com;
begin
     port[$21]:=port[$21] or $08;  { Disable IRQ3 }
     SetIntvec($0B,Int0C_save);
end;

procedure Area;
var x,y:integer;
begin
   SetFillPattern(Gray10,black);  {rectangle}
   Bar(50,60,570,360);
   setcolor(yellow);
   line(50,40,50,437);   {sb y}
   line(50,437,480,437); {sb x}
   setcolor(yellow);
   for y:=0to24 do line(51,53+(y*16),55,53+(y*16)); {grs kcl sb y}
   for y:=0to20do line(50+(y*20),432,50+(y*20),437); {grs kcl sb
                                                      x}
   setcolor(darkgray);
   for x:=0 to 11  do line(55,53+(x*32),480,53+(x*32)); {hor line}
   for x:=0 to 9 do line(90+(x*40),55,90+(x*40),437); {ver line}
   outtextxy(150,15 ,' GRAFIK PENGUKURAN TEGANGAN - SUHU');
   setcolor(white);
   outtextxy(12,26 ,' Volt');
   outtextxy(10,50 ,' 4.00');
   outtextxy(10,82 ,' 3.66');
   outtextxy(10,114,' 3.33');
   outtextxy(10,146,' 3.00');
   outtextxy(10,178,' 2.67');
   outtextxy(10,210,' 2.33');
   outtextxy(10,242,' 2.00');
   outtextxy(10,274,' 1.67');
   outtextxy(10,306,' 1.33');
```

```
    outtextxy(10,338,' 1.00');
    outtextxy(10,370,' 0.67');
    outtextxy(10,402,' 0.33');
    outtextxy(20,434,'  0');

    outtextxy(40 ,440,' ');
    outtextxy(80 ,440,'10');
    outtextxy(120,440,'20');
    outtextxy(160,440,'30');
    outtextxy(200,440,'40');
    outtextxy(245,440,'50');
    outtextxy(285,440,'60');
    outtextxy(325,440,'70');
    outtextxy(365,440,'80');
    outtextxy(405,440,'90');
    outtextxy(445,440,'100 øC');

    setcolor(7);
    line(50,457,80,457);
    outtextxy(100,455,'Termokopel');

    setcolor(10);
    line(200,457,230,457);
    outtextxy(250,455,'LM 335');

end;

procedure InisialisasiGraph;
begin
     grdriver:= detect;
     grmode  := VGAHi;
     Initgraph(grDriver,grMode,'c:\tp\bgi');
end;

procedure Capture;
begin
    assign(fil,'SUHU.dat');
    rewrite(fil);
end;

{Program Utama}
begin
  clrscr;
  write(' MASUKAN SUHU MAX: ');READLN(S);
  CLRSCR;
  TEXTCOLOR(7);
  n:=0;
  writeln(' DATA PENGUKURAN SUHU ');
  capture;
  Open_com;

  REPEAT
       IF LM>S THEN
          PORT[TX_BUFFER]:=$0
       ELSE
       BEGIN
```

```
          PORT[TX_BUFFER]:=$1;
          GOTOXY(10,8); WRITELN('DATA 0 =',DATA0:3);
          GOTOXY(10,10); WRITELN('TERMOKOPEL =',TERMO:3:0);
          GOTOXY(10,12); WRITELN('DATA 1 =',DATA1:3);
          GOTOXY(10,14); WRITELN('LM335 =',LM:3:0);
          l[n]:=lm;
          t[n]:=termo;
          vl[n]:=data1;
          vt[n]:=data0;
          with dat do
          begin
             a:=lm;
             b:=termo;
             c:=data1;
             d:=data0;
          end;
          write(fil, dat);
          delay(1000);
          inc(n);
       END;
  UNTIL (KEYPRESSED);
  Close_com;
  inisialisasigraph;
  area;
  x:=1;
  repeat
     setcolor(10);
     if x=1 then
     begin
        tempx:=52+round(4*l[x]);
        tempy:=502-round(1.84*vl[x]);
        moveto(tempx,tempy);
     end
     else
        lineto(52+round(4*l[x]),502-round(1.84*vl[x]));
     inc(x);
  until x=n;
  x:=1;
  repeat
     setcolor(7);
     if x=1 then
     begin
        tempx:=52+round(4*t[x]);
        tempy:=427-round(1.43*vt[x]);
        moveto(tempx,tempy);
     end
     else
        lineto(52+round(4*t[x]),427-round(1.43*vt[x]));
     inc(x);
  until x=n;
  readln;
  close(fil);
  closegraph;
end.
```

19-1231; Rev 1, 10/98

EVALUATION KIT AVAILABLE

MAXIM

# +5V, Low-Power, Multi-Channel, Serial 8-Bit ADCs



## General Description

The MAX1112/MAX1113 are low-power, 8-bit, 8-channel analog-to-digital converters (ADCs) that feature an internal track/hold, voltage reference, clock, and serial interface. They operate from a single +4.5V to +5.5V supply and consume only 135µA while sampling at rates up to 50ksps. The MAX1112's 8 analog inputs and the MAX1113's 4 analog inputs are software-configurable, allowing unipolar/bipolar and single-ended/differential operation.

Successive-approximation conversions are performed using either the internal clock or an external serial-interface clock. The full-scale analog input range is determined by the 4.096V internal reference, or by an externally applied reference ranging from 1V to $V_{DD}$. The 4-wire serial interface is compatible with the SPI™, QSPI™, and MICROWIRE™ serial-interface standards. A serial-strobe output provides the end-of-conversion signal for interrupt-driven processors.

The MAX1112/MAX1113 have a software-programmable, 2µA automatic power-down mode to minimize power consumption. Using power-down, the supply current is reduced to 13µA at 1ksps, and only 82µA at 10ksps. Power-down can also be controlled using the $\overline{SHDN}$ input pin. Accessing the serial interface automatically powers up the device.

The MAX1112 is available in 20-pin SSOP and DIP packages. The MAX1113 is available in small 16-pin QSOP and DIP packages.

## Applications

Portable Data Logging

Hand-Held Measurement Devices

Medical Instruments

System Diagnostics

Solar-Powered Remote Systems

4–20mA-Powered Remote Data-Acquisition Systems

***Pin Configurations appear at end of data sheet.***

*SPI and QSPI are trademarks of Motorola, Inc.*
*MICROWIRE is a trademark of National Semiconductor Corp.*

## Features

- **+4.5V to +5.5V Single Supply**
- **Low Power: 135µA at 50ksps**
  **13µA at 1ksps**
- **8-Channel Single-Ended or 4-Channel Differential Inputs (MAX1112)**
- **4-Channel Single-Ended or 2-Channel Differential Inputs (MAX1113)**
- **Internal Track/Hold; 50kHz Sampling Rate**
- **Internal 4.096V Reference**
- **SPI/QSPI/MICROWIRE-Compatible Serial Interface**
- **Software-Configurable Unipolar or Bipolar Inputs**
- **Total Unadjusted Error: ±1LSB (max)**
  **±0.3LSB (typ)**

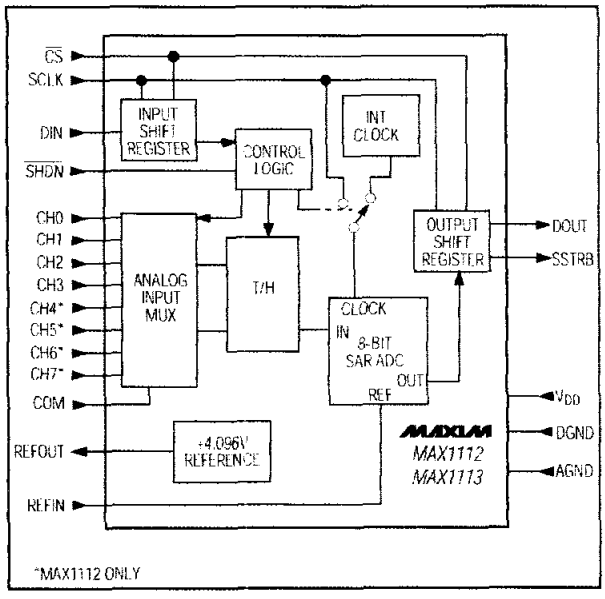
## Ordering Information

| PART | TEMP. RANGE | PIN-PACKAGE |
|---|---|---|
| **MAX1112**CPP | 0°C to +70°C | 20 Plastic DIP |
| MAX1112CAP | 0°C to +70°C | 20 SSOP |
| MAX1112C/D | 0°C to +70°C | Dice* |

**Dice are specified at $T_A$ = +25°C, DC parameters only.*

***Ordering Information continued at end of data sheet.***

## Functional Diagram



## ABSOLUTE MAXIMUM RATINGS

$V_{DD}$ to AGND .....-0.3V to 6V
AGND to DGND .....-0.3V to 0.3V
CH0–CH7, COM, REFIN,
REFOUT to AGND .....-0.3V to ($V_{DD}$ + 0.3V)
Digital Inputs to DGND .....-0.3V to 6V
Digital Outputs to DGND .....-0.3V to ($V_{DD}$ + 0.3V)
Continuous Power Dissipation ($T_A$ = +70°C)
16 Plastic DIP (derate 10.53mW/°C above +70°C) .....842mW
16 QSOP (derate 8.30mW/°C above +70°C) .....667mW
16 CERDIP (derate 10.00mW/°C above +70°C) .....800mW
20 Plastic DIP (derate 11.11mW/°C above +70°C) .....889mW
20 SSOP (derate 8.00mW/°C above +70°C) .....640mW
20 CERDIP (derate 11.11mW/°C above +70°C) .....889mW
Operating Temperature Ranges
MAX1112C_P/MAX1113C_E .....0°C to +70°C
MAX1112E_P/MAX1113E_E .....-40°C to +85°C
MAX1112MJP/MAX1113MJE .....-55°C to +125°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## ELECTRICAL CHARACTERISTICS

($V_{DD}$ = +4.5V to +5.5V; unipolar input mode; COM = 0V; $f_{SCLK}$ = 500kHz, external clock (50% duty cycle); 10 clocks/conversion cycle (50ksps); 1µF capacitor at REFOUT; $T_A$ = $T_{MIN}$ to $T_{MAX}$; unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **DC ACCURACY** | | | | | | |
| Resolution | | | 8 | | | Bits |
| Relative Accuracy (Note 1) | INL | | | ±0.1 | ±0.5 | LSB |
| Differential Nonlinearity | DNL | No missing codes over temperature | | | ±1 | LSB |
| Offset Error | | | | ±0.3 | ±1 | LSB |
| Gain Error (Note 2) | | Internal or external reference | | | ±1 | LSB |
| Gain Temperature Coefficient | | External reference, 4.096V | | ±0.8 | | ppm/°C |
| Total Unadjusted Error | TUE | MAX111_C/E | | ±0.3 | ±1 | LSB |
| Channel-to-Channel Offset Matching | | | | ±0.1 | | LSB |
| **DYNAMIC SPECIFICATIONS** (10.034kHz sine-wave input, 4.096Vp-p, 50ksps, 500kHz external clock) | | | | | | |
| Signal-to-Noise and Distortion Ratio | SINAD | | | 49 | | dB |
| Total Harmonic Distortion (up to the 5th harmonic) | THD | | | -70 | | dB |
| Spurious-Free Dynamic Range | SFDR | | | 68 | | dB |
| Channel-to-Channel Crosstalk | | $V_{CH\_}$ = 4.096Vp-p, 25kHz (Note 3) | | -75 | | dB |
| Small-Signal Bandwidth | | -3dB rolloff | | 1.5 | | MHz |
| Full-Power Bandwidth | | | | 800 | | kHz |

## ELECTRICAL CHARACTERISTICS (continued)

($V_{DD}$ = +4.5V to +5.5V; unipolar input mode: COM = 0V; $f_{SCLK}$ = 500kHz, external clock (50% duty cycle); 10 clocks/conversion cycle (50ksps); 1µF capacitor at REFOUT; $T_A$ = $T_{MIN}$ to $T_{MAX}$; unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **CONVERSION RATE** | | | | | | | |
| Conversion Time (Note 4) | $t_{CONV}$ | Internal clock | | | 25 | 55 | µs |
| | | External clock, 500kHz, 10 clocks/conversion | | 20 | | | |
| Track/Hold Acquisition Time | $t_{ACQ}$ | External clock, 2MHz | | 1 | | | µs |
| Aperture Delay | | | | | 10 | | ns |
| Aperture Jitter | | | | | <50 | | ps |
| Internal Clock Frequency | | | | | 400 | | kHz |
| External Clock-Frequency Range | | (Note 5) | | 50 | | 500 | kHz |
| | | Used for data transfer only | | | | 2 | MHz |
| **ANALOG INPUT** | | | | | | | |
| Input Voltage Range, Single-Ended and Differential (Note 6) | | Unipolar input, COM = 0V | | 0 | | $V_{REFIN}$ | V |
| | | Bipolar input, COM = $V_{REFIN}$ / 2 | | | | COM ± $V_{REFIN}$ / 2 | |
| Multiplexer Leakage Current | | On/off leakage current, $V_{CH\_}$ = 0V or $V_{DD}$ | | | ±0.01 | ±1 | µA |
| Input Capacitance | | | | | 18 | | pF |
| **INTERNAL REFERENCE** | | | | | | | |
| REFOUT Voltage | | | | 3.936 | 4.096 | 4.256 | V |
| REFOUT Short-Circuit Current | | | | | 6 | | mA |
| REFOUT Temperature Coefficient | | | | | ±50 | | ppm/°C |
| Load Regulation (Note 7) | | 0mA to 0.5mA output load | | | 4.5 | | mV |
| Capacitive Bypass at REFOUT | | | | 1 | | | µF |
| **EXTERNAL REFERENCE AT REFIN** | | | | | | | |
| Input Voltage Range | | | | 1 | | $V_{DD}$ + 50mV | V |
| Input Current | | (Note 8) | | | 1 | 20 | µA |
| **POWER REQUIREMENTS** | | | | | | | |
| Supply Voltage | $V_{DD}$ | | | 4.5 | | 5.5 | V |
| Supply Current | $I_{DD}$ | Full-scale input, $C_{LOAD}$ = 10pF | Operating mode | | 135 | 250 | µA |
| | | | Reference disabled | | 95 | | |
| | | Power-down | Software | | 2 | | |
| | | | $\overline{SHDN}$ at DGND | | 3.2 | 10 | |
| Power-Supply Rejection (Note 9) | PSR | $V_{DD}$ = 4.5V to 5.5V; external reference, 4.096V; full-scale input | | | ±0.4 | ±4 | mV |

## ELECTRICAL CHARACTERISTICS (continued)

($V_{DD}$ = +4.5V to +5.5V; unipolar input mode; COM = 0V; $f_{SCLK}$ = 500kHz, external clock (50% duty cycle); 10 clocks/conversion cycle (50ksps); 1µF capacitor at REFOUT; $T_A$ = $T_{MIN}$ to $T_{MAX}$; unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **DIGITAL INPUTS: DIN, SCLK, $\overline{CS}$** | | | | | | |
| DIN, SCLK, $\overline{CS}$ Input High Voltage | $V_{IH}$ | | 3 | | | V |
| DIN, SCLK, $\overline{CS}$ Input Low Voltage | $V_{IL}$ | | | | 0.8 | V |
| DIN, SCLK, $\overline{CS}$ Input Hysteresis | $V_{HYST}$ | | | 0.2 | | V |
| DIN, SCLK, $\overline{CS}$ Input Leakage | $I_{IN}$ | Digital inputs = 0V or $V_{DD}$ | | | ±1 | µA |
| DIN, SCLK, $\overline{CS}$ Input Capacitance | $C_{IN}$ | (Note 5) | | | 15 | pF |
| **$\overline{SHDN}$ INPUT** | | | | | | |
| $\overline{SHDN}$ Input High Voltage | $V_{SH}$ | | $V_{DD}$ - 0.4 | | | V |
| $\overline{SHDN}$ Input Mid-Voltage | $V_{SM}$ | | 1.1 | | $V_{DD}$ - 1.1 | V |
| $\overline{SHDN}$ Voltage, Floating | $V_{FLT}$ | $\overline{SHDN}$ = open | | $V_{DD}$ / 2 | | V |
| $\overline{SHDN}$ Input Low Voltage | $V_{SL}$ | | | | 0.4 | V |
| $\overline{SHDN}$ Input Current | | $\overline{SHDN}$ = 0V or $V_{DD}$ | | | ±4 | µA |
| $\overline{SHDN}$ Maximum Allowed Leakage for Mid-Input | | $\overline{SHDN}$ = open | | | ±100 | nA |
| **DIGITAL OUTPUTS: DOUT, SSTRB** | | | | | | |
| Output Low Voltage | $V_{OL}$ | $I_{SINK}$ = 5mA | | | 0.4 | V |
| | | $I_{SINK}$ = 16mA | | | 0.8 | |
| Output High Voltage | $V_{OH}$ | $I_{SOURCE}$ = 0.5mA | $V_{DD}$ - 0.5 | | | V |
| Three-State Leakage Current | $I_L$ | $\overline{CS}$ = $V_{DD}$ | | ±0.01 | ±10 | µA |
| Three-State Output Capacitance | $C_{OUT}$ | $\overline{CS}$ = $V_{DD}$ (Note 5) | | | 15 | pF |

## TIMING CHARACTERISTICS (Figures 8 and 9)

($V_{DD}$ = +4.5V to +5.5V, $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted.)

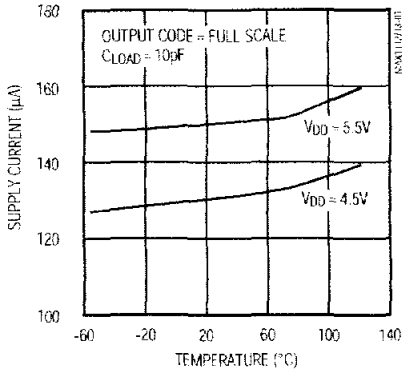
| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Track/Hold Acquisition Time | tACQ | | | 1 | | | µs |
| DIN to SCLK Setup | tDS | | | 100 | | | ns |
| DIN to SCLK Hold | tDH | | | 0 | | | ns |
| SCLK Fall to Output Data Valid | tDO | *Figure 1*, $C_{LOAD}$ = 100pF | MAX111_C/E | 20 | | 200 | ns |
| | | | MAX111_M | 20 | | 240 | |
| $\overline{CS}$ Fall to Output Enable | tDV | Figure 1, $C_{LOAD}$ = 100pF | | | | 240 | ns |
| $\overline{CS}$ Rise to Output Disable | tTR | Figure 2, $C_{LOAD}$ = 100pF | | | | 240 | ns |
| $\overline{CS}$ to SCLK Rise Setup | tCSS | | | 100 | | | ns |
| $\overline{CS}$ to SCLK Rise *Hold* | tCSH | | | 0 | | | ns |
| SCLK Pulse Width High | tCH | | | 200 | | | ns |
| SCLK Pulse Width Low | tCL | | | 200 | | | ns |
| SCLK Fall to SSTRB | tSSTRB | $C_{LOAD}$ = 100pF | | | | 240 | ns |
| $\overline{CS}$ Fall to SSTRB Output Enable (Note 5) | tSDV | Figure 1, external clock mode only, $C_{LOAD}$ = 100pF | | | | 240 | ns |
| $\overline{CS}$ Rise to SSTRB Output Disable (Note 5) | tSTR | Figure 2, external clock mode only, $C_{LOAD}$ = 100pF | | | | 240 | ns |
| SSTRB Rise to SCLK Rise (Note 5) | tSCK | Figure 11, internal clock mode only | | 0 | | | ns |
| Wakeup Time | tWAKE | External reference | | | 20 | | µs |
| | | Internal reference (Note 10) | | | 24 | | ms |

**Note 1:** Relative accuracy is the analog value's deviation (at any code) from its theoretical value after the full-scale range is calibrated.
**Note 2:** $V_{REFIN}$ = 4.096V, offset nulled.
**Note 3:** On-channel grounded; sine wave applied to all off-channels.
**Note 4:** Conversion time is defined as the number of clock cycles multiplied by the clock period; clock has 50% duty cycle.
**Note 5:** Guaranteed by design. Not subject to production testing.
**Note 6:** Common-mode range for the analog inputs is from AGND to $V_{DD}$.
**Note 7:** External load should not change during the conversion for specified accuracy.
**Note 8:** External reference at 4.096V, full-scale input, 500kHz external clock.
**Note 9:** Measured as | $V_{FS}$ (4.5V) - $V_{FS}$ (5.5V) |.
**Note 10:** 1µF at REFOUT; internal reference settling to 0.5LSB.

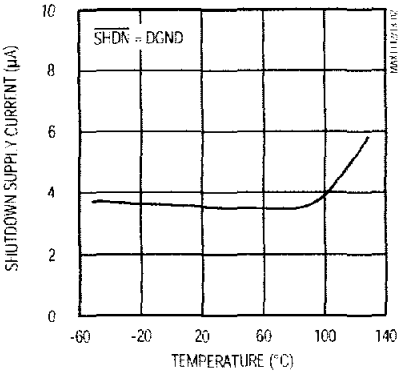
## Typical Operating Characteristics

($V_{DD}$ = +5.0V; $f_{SCLK}$ = 500kHz; external clock (50% duty cycle); $R_L$ = ∞; $T_A$ = +25°C, unless otherwise noted.)

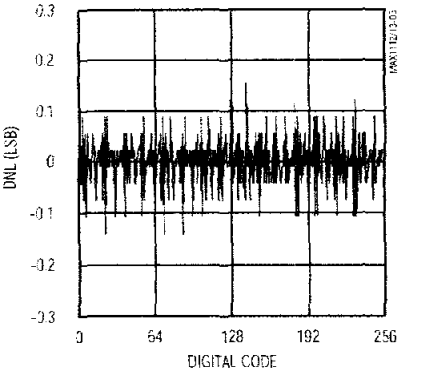
**SUPPLY CURRENT vs. TEMPERATURE**



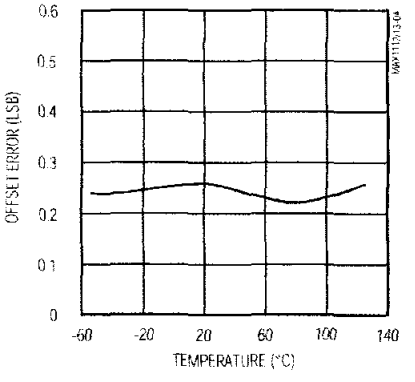

**SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE**



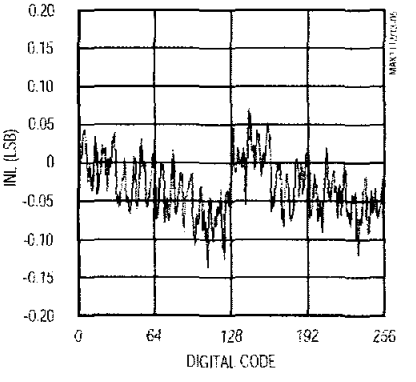

**DIFFERENTIAL NONLINEARITY vs. CODE**



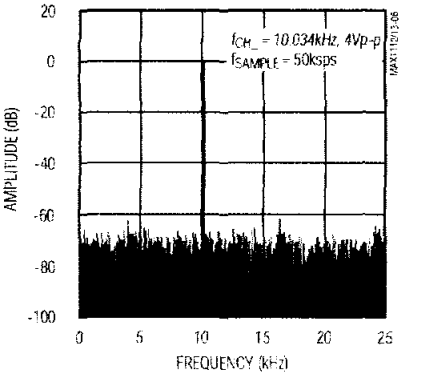

**OFFSET ERROR vs. TEMPERATURE**




**INTEGRAL NONLINEARITY vs. CODE**




**FFT PLOT**



## Pin Description

| PIN | | NAME | FUNCTION |
|---|---|---|---|
| MAX1112 | MAX1113 | | |
| 1–4 | 1–4 | CH0–CH3 | Sampling Analog Inputs |
| 5–8 | — | CH4–CH7 | Sampling Analog Inputs |
| 9 | 5 | COM | Ground Reference for Analog Inputs. Sets zero-code voltage in single-ended mode. Must be stable to ±0.5LSB. |
| 10 | 6 | $\overline{SHDN}$ | Three-Level Shutdown Input. Normally floats. Pulling $\overline{SHDN}$ low shuts the MAX1112/ MAX1113 down to 10µA (max) supply current; otherwise, the devices are fully operational. Pulling $\overline{SHDN}$ high shuts down the internal reference. |
| 11 | 7 | REFIN | Reference Voltage Input for Analog-to-Digital Conversion. Connect to REFOUT to use the internal reference. |
| 12 | 8 | REFOUT | Internal Reference Generator Output. Bypass with a 1µF capacitor to AGND. |
| 13 | 9 | AGND | Analog Ground |
| 14 | 10 | DGND | Digital Ground |
| 15 | 11 | DOUT | Serial-Data Output. Data is clocked out on SCLK's falling edge. High impedance when $\overline{CS}$ is high. |
| 16 | 12 | SSTRB | Serial-Strobe Output. In internal clock mode, SSTRB goes low when the MAX1112/ MAX1113 begin the A/D conversion and goes high when the conversion is complete. In external clock mode, SSTRB pulses high for two clock periods before the MSB is shifted out. High impedance when $\overline{CS}$ is high (external clock mode only). |
| 17 | 13 | DIN | Serial-Data Input. Data is clocked in at SCLK's rising edge. |
| 18 | 14 | $\overline{CS}$ | Active-Low Chip Select. Data is not clocked into DIN unless $\overline{CS}$ is low. When $\overline{CS}$ is high, DOUT is high impedance. |
| 19 | 15 | SCLK | Serial-Clock Input. Clocks data in and out of serial interface. In external clock mode, SCLK also sets the conversion speed (duty cycle must be 45% to 55%). |
| 20 | 16 | $V_{DD}$ | Positive Supply Voltage, +4.5V to +5.5V |

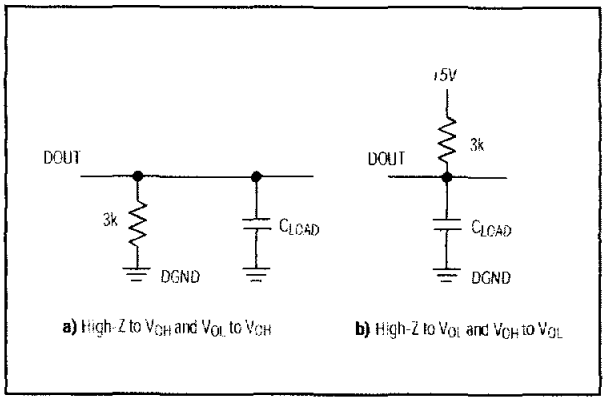



*Figure 1. Load Circuits for Enable Time*

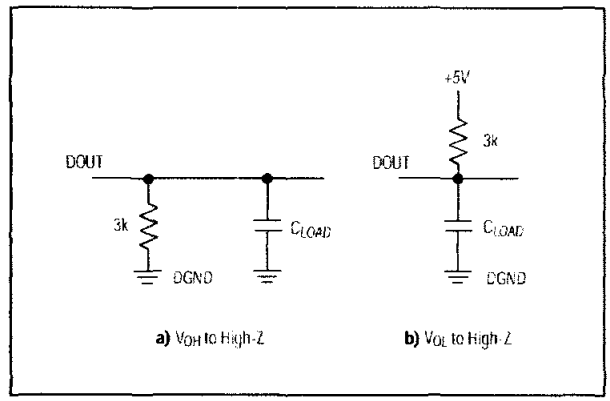



*Figure 2. Load Circuits for Disable Time*

## Detailed Description

The MAX1112/MAX1113 analog-to-digital converters (ADCs) use a successive-approximation conversion technique and input track/hold (T/H) circuitry to convert an analog signal to an 8-bit digital output. A flexible serial interface provides easy interface to microprocessors (µPs). Figure 3 shows the Typical Operating Circuit.

### Pseudo-Differential Input

The sampling architecture of the ADC's analog comparator is illustrated in Figure 4, the equivalent input circuit. In single-ended mode, IN+ is internally switched to the selected input channel, CH_, and IN- is switched to COM. In differential mode, IN+ and IN- are selected from the following pairs: CH0/CH1, CH2/CH3, CH4/CH5, and CH6/CH7. Configure the MAX1112 channels with Table 1 and the MAX1113 channels with Table 2.

In differential mode, IN- and IN+ are internally switched to either of the analog inputs. This configuration is pseudo-differential to the effect that only the signal at IN+ is sampled. The return side (IN-) must remain stable within ±0.5LSB (±0.1LSB for best results) with respect to AGND during a conversion. To accomplish this, connect a 0.1µF capacitor from IN- (the selected analog input) to AGND if necessary.

During the acquisition interval, the channel selected as the positive input (IN+) charges capacitor CHOLD. The acquisition interval spans two SCLK cycles and ends on the falling SCLK edge after the last bit of the input control word has been entered. At the end of the acquisition interval, the T/H switch opens, retaining charge on CHOLD as a sample of the signal at IN+.

The conversion interval begins with the input multiplexer switching CHOLD from the positive input (IN+) to the negative input (IN-). In single-ended mode, IN- is simply COM. This unbalances node ZERO at the input of the comparator. The capacitive DAC adjusts during the remainder of the conversion cycle to restore node ZERO to 0V within the limits of 8-bit resolution. This action is equivalent to transferring a charge of 18pF x ($V_{IN+}$ - $V_{IN-}$) from CHOLD to the binary-weighted capacitive DAC, which in turn forms a digital representation of the analog input signal.

### Track/Hold

The T/H enters its tracking mode on the falling clock edge after the sixth bit of the 8-bit contro byte has been shifted in. It enters its hold mode on the falling clock edge after the eighth bit of the control byte has been shifted in. If the converter is set up for single-ended inputs, IN- is connected to COM, and the converter samples the "+" input; if it is set up for differential inputs, IN- connects to the "-" input, and the difference (IN+ - IN-) is sampled. At the end of the conversion, the positive input connects back to IN+, and CHOLD charges to the input signal.

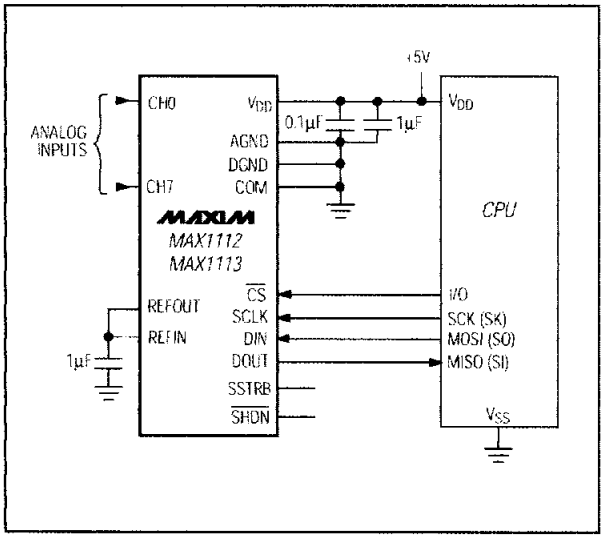



Figure 3. Typical Operating Circuit

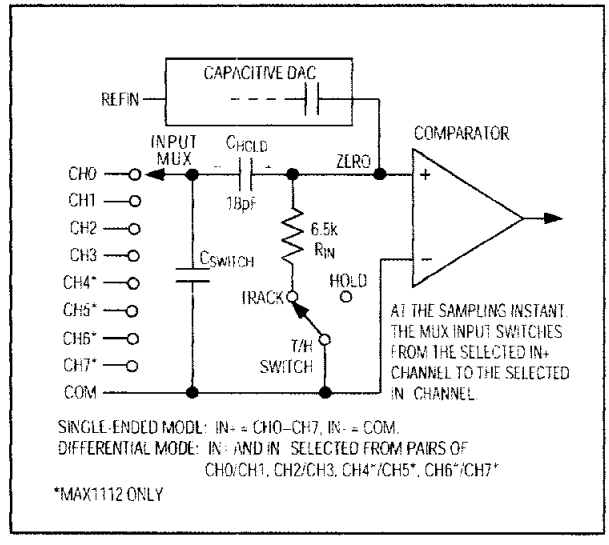



Figure 4. Equivalent Input Circuit

Table 1a. MAX1112 Channel Selection in Single-Ended Mode (SGL/$\overline{DIF}$ = 1)

| SEL2 | SEL1 | SEL0 | CH0 | CH1 | CH2 | CH3 | CH4 | CH5 | CH6 | CH7 | COM |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | + | | | | | | | | - |
| 1 | 0 | 0 | | + | | | | | | | - |
| 0 | 0 | 1 | | | + | | | | | | - |
| 1 | 0 | 1 | | | | + | | | | | - |
| 0 | 1 | 0 | | | | | + | | | | - |
| 1 | 1 | 0 | | | | | | + | | | - |
| 0 | 1 | 1 | | | | | | | + | | - |
| 1 | 1 | 1 | | | | | | | | + | - |

Table 1b. MAX1112 Channel Selection in Differential Mode (SGL/$\overline{DIF}$ = 0)

| SEL2 | SEL1 | SEL0 | CH0 | CH1 | CH2 | CH3 | CH4 | CH5 | CH6 | CH7 |
|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | + | - | | | | | | |
| 0 | 0 | 1 | | | + | - | | | | |
| 0 | 1 | 0 | | | | | + | - | | |
| 0 | 1 | 1 | | | | | | | + | - |
| 1 | 0 | 0 | - | + | | | | | | |
| 1 | 0 | 1 | | | - | + | | | | |
| 1 | 1 | 0 | | | | | - | + | | |
| 1 | 1 | 1 | | | | | | | - | + |

Table 2a. MAX1113 Channel Selection in Single-Ended Mode (SGL/$\overline{DIF}$ = 1)

| SEL2 | SEL1 | SEL0 | CH0 | CH1 | CH2 | CH3 | COM |
|---|---|---|---|---|---|---|---|
| 0 | 0 | X | + | | | | - |
| 1 | 0 | X | | + | | | - |
| 0 | 1 | X | | | + | | - |
| 1 | 1 | X | | | | + | - |

Table 2b. MAX1113 Channel Selection in Differential Mode (SGL/$\overline{DIF}$ = 0)

| SEL2 | SEL1 | SEL0 | CH0 | CH1 | CH2 | CH3 |
|---|---|---|---|---|---|---|
| 0 | 0 | X | + | - | | |
| 0 | 1 | X | | | + | - |
| 1 | 0 | X | - | + | | |
| 1 | 1 | X | | | - | + |

The time required for the T/H to acquire an input signal is a function of how quickly its input capacitance is charged. If the input signal's source impedance is high, the acquisition time lengthens, and more time must be allowed between conversions. The acquisition time, $t_{ACQ}$, is the minimum time needed for the signal to be acquired. It is calculated by:

$$t_{ACQ} = 6 \times (R_S + R_{IN}) \times 18pF$$

where $R_{IN}$ = 6.5kΩ, $R_S$ = the source impedance of the input signal, and $t_{ACQ}$ is never less than 1µs. Note that source impedances below 2.4kΩ do not significantly affect the AC performance of the ADC.

### Input Bandwidth

The ADC's input tracking circuitry has a 1.5MHz small-signal bandwidth, so it is possible to digitize high-speed transient events and measure periodic signals with bandwidths exceeding the ADC's sampling rate by using undersampling techniques. To avoid high-frequency signals being aliased into the frequency band of interest, anti-alias filtering is recommended.

### Analog Inputs

Internal protection diodes, which clamp the analog input to $V_{DD}$ and AGND, allow the channel input pins to swing from (AGND - 0.3V) to ($V_{DD}$ + 0.3V) without damage. However, for accurate conversions near full scale, the inputs must not exceed $V_{DD}$ by more than 50mV or be lower than AGND by 50mV.

**If the analog input exceeds 50mV beyond the supplies, do not forward bias the protection diodes of off channels over 2mA.**

The MAX1112/MAX1113 can be configured for differential or single-ended inputs with bits 2 and 3 of the control byte (Table 3). In single-ended mode, analog inputs are internally referenced to COM with a full-scale input range from COM to $V_{REFIN}$ + COM. For bipolar operation, set COM to $V_{REFIN}$ / 2.

In differential mode, choosing unipolar mode sets the differential input range at 0V to $V_{REFIN}$. In unipolar mode, the output code is invalid (code zero) when a negative differential input voltage is applied. Bipolar mode sets the differential input range to ±$V_{REFIN}$ / 2. Note that in this mode, the common-mode input range includes both supply rails. Refer to Table 4 for input voltage ranges.

### Quick Look

To quickly evaluate the MAX1112/MAX1113's analog performance, use the circuit of Figure 5. The MAX1112/MAX1113 require a control byte to be written to DIN before each conversion. Tying DIN to +5V feeds

## Table 3. Control-Byte Format

| BIT 7 (MSB) | BIT 6 | BIT 5 | BIT 4 | BIT 3 | BIT 2 | BIT 1 | BIT 0 (LSB) |
|---|---|---|---|---|---|---|---|
| START | SEL2 | SEL1 | SEL0 | UNI/$\overline{BIP}$ | SGL/$\overline{DIF}$ | PD1 | PD0 |

| BIT | NAME | DESCRIPTION |
|---|---|---|
| 7 (MSB) | START | The first logic "**1**" bit after $\overline{CS}$ goes low defines the beginning of the control byte. |
| 6<br>5<br>4 | SEL2<br>SEL1<br>SEL0 | Select which of the input channels are to be used for the conversion (Tables 1 and 2). |
| 3 | UNI/$\overline{BIP}$ | **1** = unipolar, **0** = bipolar. Selects unipolar or bipolar conversion mode (Table 4). |
| 2 | SGL/$\overline{DIF}$ | **1** = single ended, **0** = differential. Selects single-ended or differential conversions. In single-ended mode, input signal voltages are referred to COM. In differential mode, the voltage difference between two channels is measured. See Tables 1 and 2. |
| 1 | PD1 | **1** = fully operational, **0** = power-down.<br>Selects fully operational or power-down mode. |
| 0 (LSB) | PD0 | **1** = external clock mode, **0** = internal clock mode.<br>Selects external or internal clock mode. |

**Table 4. Full-Scale and Zero-Scale Voltages**

| UNIPOLAR MODE | | BIPOLAR MODE | | |
|---|---|---|---|---|
| Full Scale | Zero Scale | Positive Full Scale | Zero Scale | Negative Full Scale |
| $V_{REFIN}$ + COM | COM | +$V_{REFIN}$ / 2 + COM | COM | -$V_{REFIN}$ / 2 + COM |

in control bytes of $FF (hex), which trigger single-ended, unipolar conversions on CH7 (MAX1112) or CH3 (MAX1113) in external clock mode without powering down between conversions. In external clock mode, the SSTRB output pulses high for two clock periods before the most significant bit (MSB) of the 8-bit conversion result is shifted out of DOUT. Varying the analog input alters the output code. A total of 10 clock cycles is required per conversion. All transitions of the SSTRB and DOUT outputs occur on SCLK's falling edge.

### How to Start a Conversion

A conversion is started by clocking a control byte into DIN. With $\overline{CS}$ low, each rising edge on SCLK clocks a bit from DIN into the MAX1112/MAX1113's internal shift register. After $\overline{CS}$ falls, the first arriving logic "1" bit at DIN defines the MSB of the control byte. Until this first start bit arrives, any number of logic "0" bits can be clocked into DIN with no effect. Table 3 shows the control-byte format.

The MAX1112/MAX1113 are compatible with MICROWIRE, SPI, and QSPI devices. For SPI, select the correct clock polarity and sampling edge in the SPI control registers: set CPOL = 0 and CPHA = 0. MICROWIRE, SPI, and QSPI all transmit a byte and receive a byte at the same time. Using the Typical Operating Circuit (Figure 3), the simplest software interface requires three 8-bit transfers to perform a conversion (one 8-bit transfer to configure the ADC, and two more 8-bit transfers to clock out the

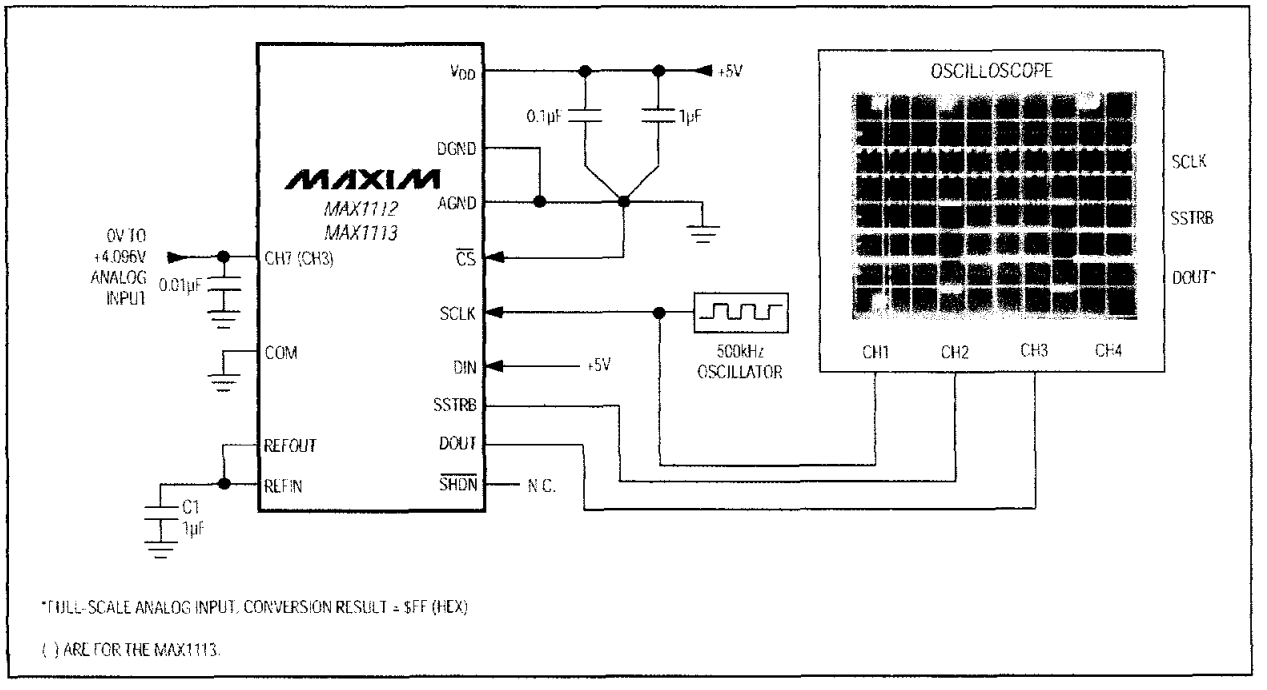



*Figure 5. Quick-Look Circuit*

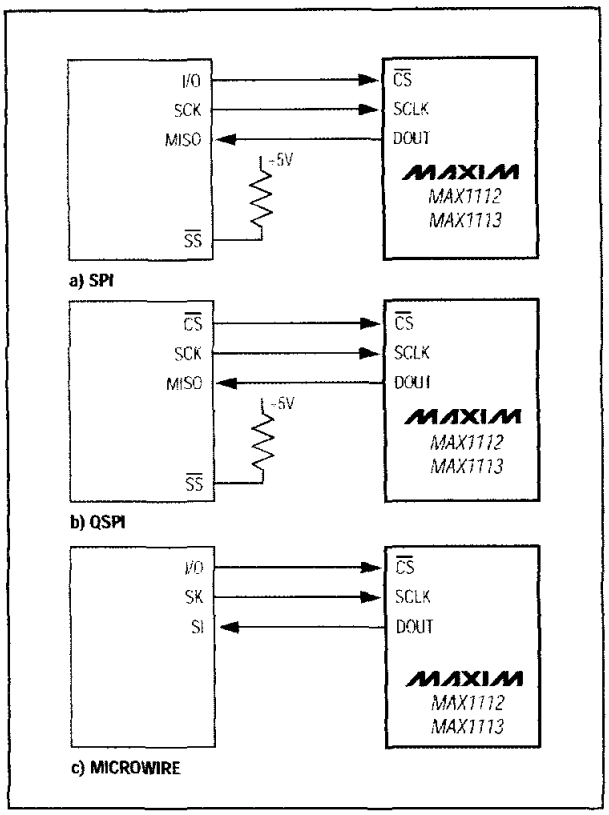



*Figure 6. Common Serial-Interface Connections to the MAX1112/MAX1113*

8-bit conversion result). Figure 6 shows the MAX1112/MAX1113 common serial-interface connections.

### *Simple Software Interface*

Make sure the CPU's serial interface runs in master mode so the CPU generates the serial clock. Choose a clock frequency from 50kHz to 500kHz.

1) Set up the control byte for external clock mode and call it TB1. TB1 should be of the format 1XXXXX11 binary, where the Xs denote the particular channel and conversion mode selected.
2) Use a general-purpose I/O line on the CPU to pull $\overline{CS}$ low.
3) Transmit TB1 and, simultaneously, receive a byte and call it RB1. Ignore RB1.
4) Transmit a byte of all zeros ($00 hex) and, simultaneously, receive byte RB2.
5) Transmit a byte of all zeros ($00 hex) and, simultaneously, receive byte RB3.
6) Pull $\overline{CS}$ high.

Figure 7 shows the timing for this sequence. Bytes RB2 and RB3 contain the result of the conversion padded with two leading zeros and six trailing zeros. The total conversion time is a function of the serial-clock frequency and the amount of idle time between 8-bit transfers. Make sure that the total conversion time does not exceed 1ms, to avoid excessive T/H droop.

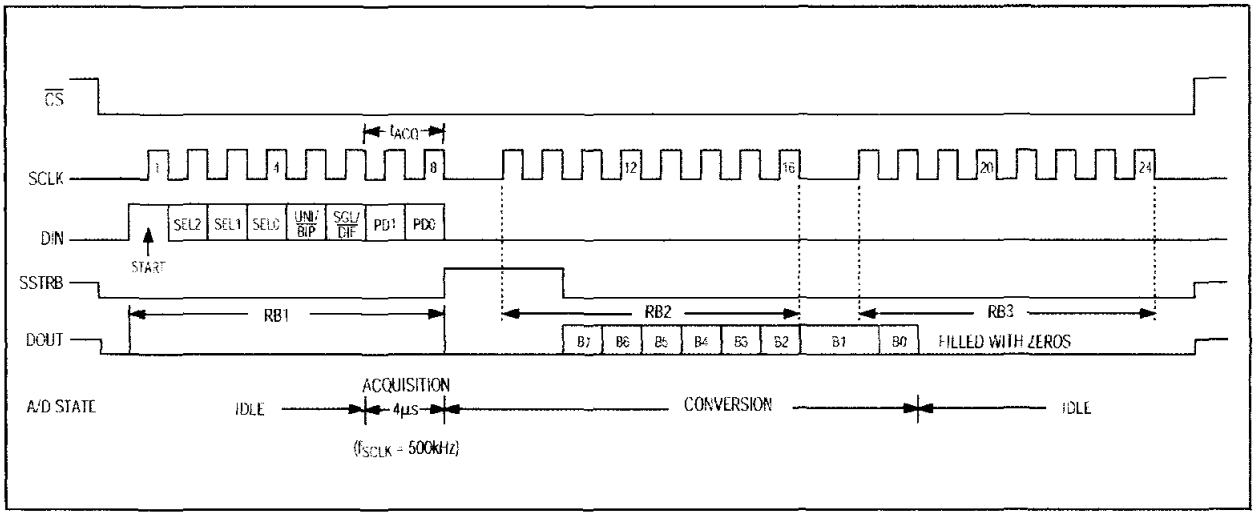



*Figure 7. Single-Conversion Timing, External Clock Mode, 24 Clocks*

### Digital Output

In unipolar input mode, the output is straight binary (Figure 15). For bipolar inputs, the output is two's-complement (Figure 16). Data is clocked out at SCLK's falling edge in MSB-first format.

### Clock Modes

The MAX1112/MAX1113 can use either an external serial clock or the internal clock to perform the successive-approximation conversion. In both clock modes, the external clock shifts data in and out of the devices. Bit PD0 of the control byte programs the clock mode. Figures 8–11 show the timing characteristics common to both modes.

### External Clock

In external clock mode, the external clock not only shifts data in and out, it also drives the analog-to-digital conversion steps. SSTRB pulses high for two clock periods after the last bit of the control byte. Successive-approximation bit decisions are made and appear at DOUT on each of the next eight SCLK falling edges (Figure 7). After the eight data bits are clocked out, subsequent clock pulses clock out zeros from the DOUT pin.

SSTRB and DOUT go into a high-impedance state when $\overline{CS}$ goes high; after the next $\overline{CS}$ falling edge, SSTRB outputs a logic low. Figure 9 shows the SSTRB timing in external clock mode.

The conversion must complete in 1ms, or droop on the sample-and-hold capacitors may degrade conversion results. Use internal clock mode if the serial-clock frequency is less than 50kHz, or if serial-clock interruptions could cause the conversion interval to exceed 1ms.

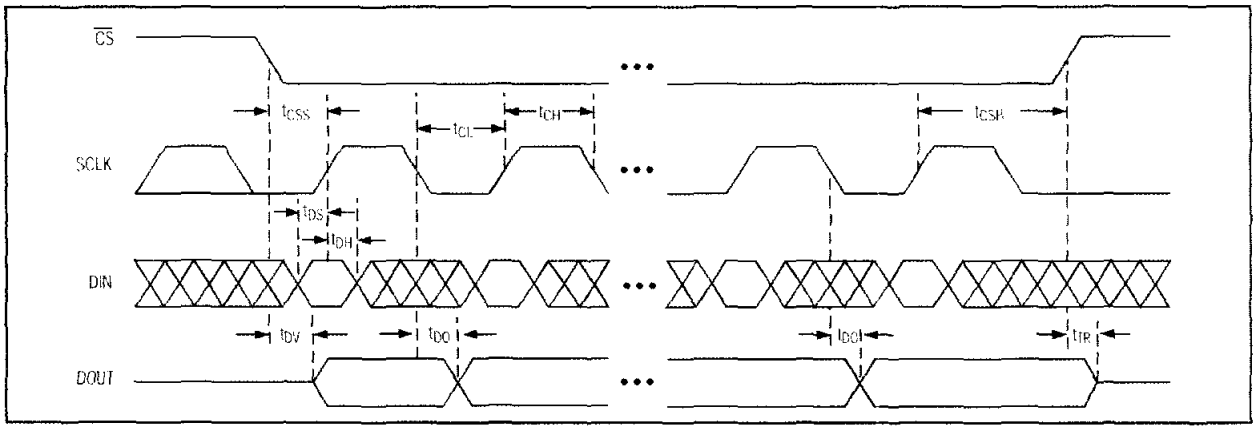



*Figure 8. Detailed Serial-Interface Timing*

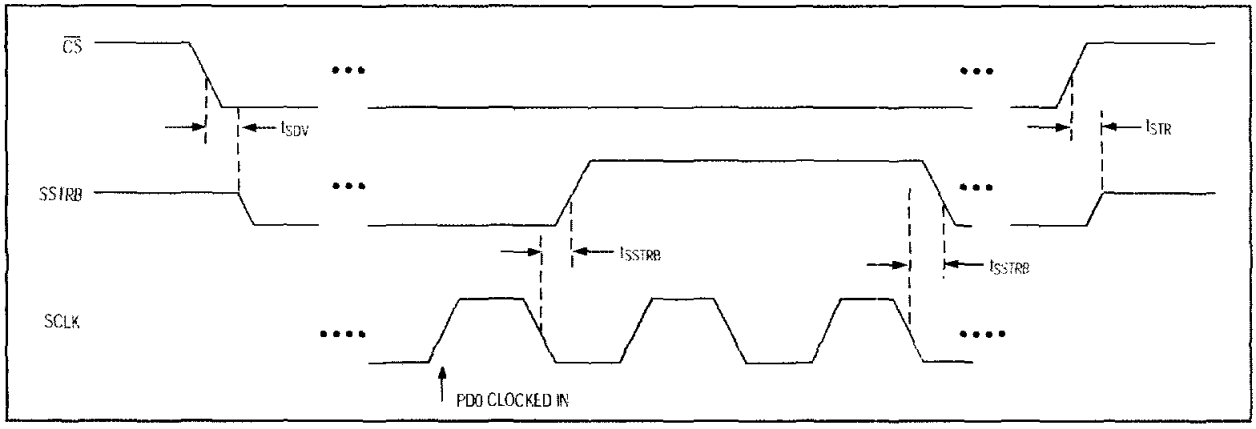



*Figure 9. External Clock Mode SSTRB Detailed Timing*

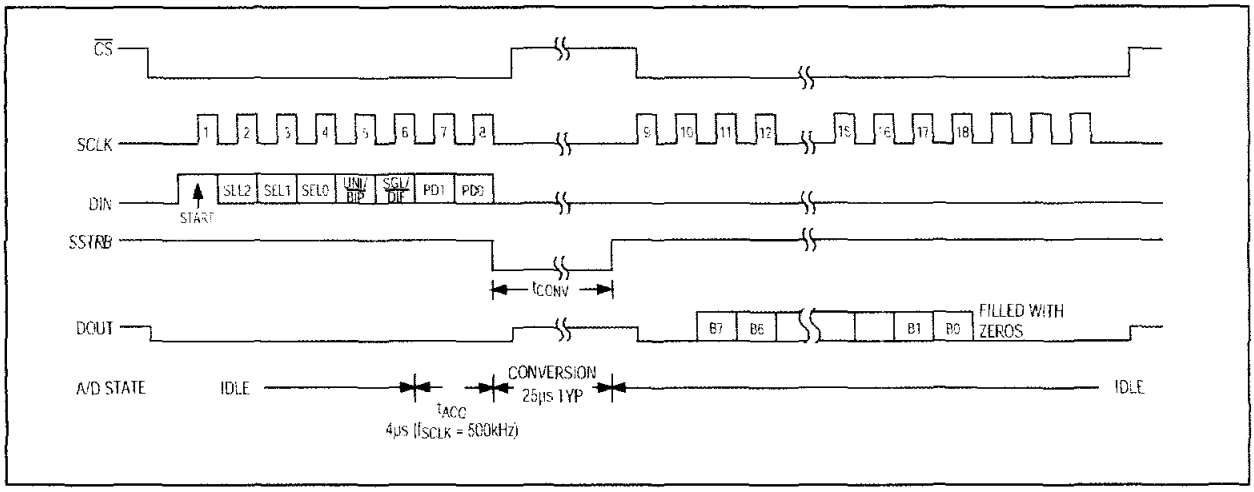



*Figure 10. Internal Clock Mode Timing*

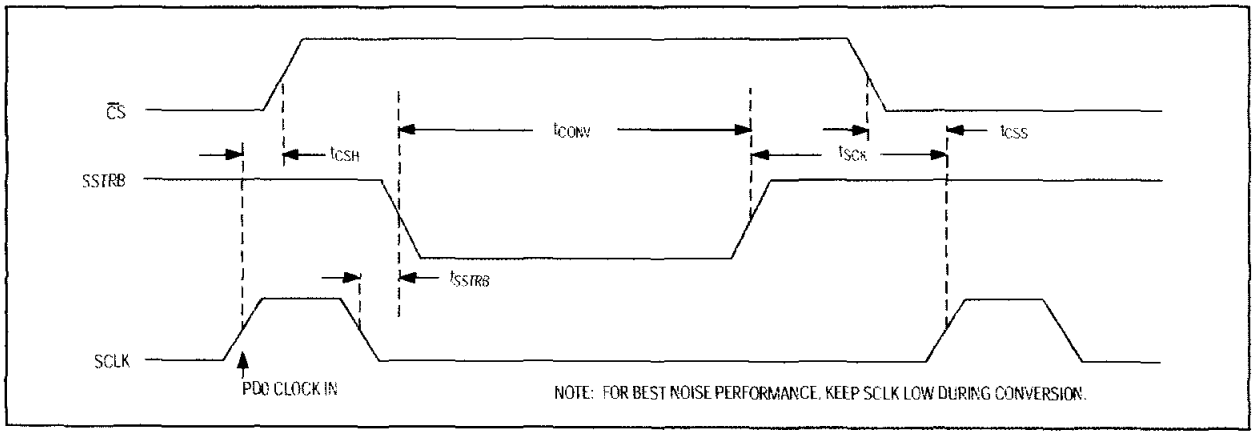



*Figure 11. Internal Clock Mode SSTRB Detailed Timing*

### *Internal Clock*

Internal clock mode frees the µP from the burden of running the SAR conversion clock. This allows the conversion results to be read back at the processor's convenience, at any clock rate up to 2MHz. SSTRB goes low at the start of the conversion and then goes high when the conversion is complete. SSTRB is low for 25µs (typically), during which time SCLK should remain low for best noise performance.

An internal register stores data when the conversion is in progress. SCLK clocks the data out of this register at any time after the conversion is complete. After SSTRB goes high, the second falling clock edge produces the MSB of the conversion at DOUT, followed by the remaining bits in MSB-first format (Figure 10). $\overline{CS}$ does not need to be held low once a conversion is started. Pulling $\overline{CS}$ high prevents data from being clocked into the MAX1112/MAX1113 and three-states DOUT, but it does not adversely affect an internal clock-mode conversion already in progress. When internal clock mode is selected, SSTRB does not go into a high-impedance state when $\overline{CS}$ goes high.

Figure 11 shows the SSTRB timing in internal clock mode. In this mode, data can be shifted in and out of the MAX1112/MAX1113 at clock rates up to 2MHz, provided that the minimum acquisition time, $t_{ACQ}$, is kept above 1µs.

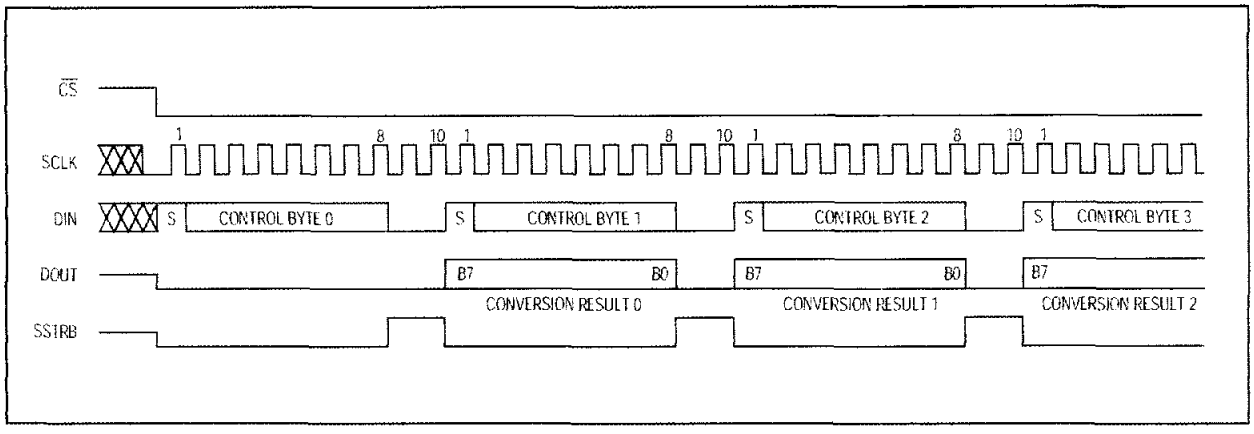



*Figure 12a. Continuous Conversions, External Clock Mode, 10 Clocks/Conversion Timing*

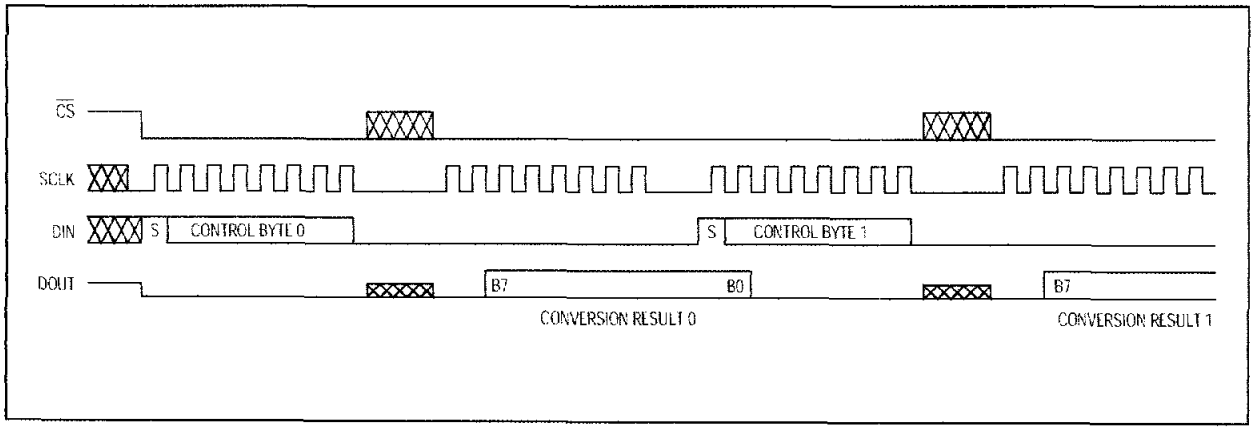



*Figure 12b. Continuous Conversions, External Clock Mode, 16 Clocks/Conversion Timing*

### Data Framing

The falling edge of $\overline{CS}$ does not start a conversion. The first logic high clocked into DIN is interpreted as a start bit and defines the first bit of the control byte. A conversion starts on the falling edge of SCLK, after the eighth bit of the control byte (the PD0 bit) is clocked into DIN. The start bit is defined as:

The first high bit clocked into DIN with $\overline{CS}$ low any time the converter is idle, e.g., after $V_{DD}$ is applied.

OR

The first high bit clocked into DIN after the MSB of a conversion in progress is clocked onto the DOUT pin.

If $\overline{CS}$ is toggled before the current conversion is complete, then the next high bit clocked into DIN is recognized as a start bit; the current conversion is terminated, and a new one is started.

The fastest the MAX1112/MAX1113 can run is 10 clocks per conversion. Figure 12a shows the serial-interface timing necessary to perform a conversion every 10 SCLK cycles in external clock mode.

Many microcontrollers require that conversions occur in multiples of eight SCLK clocks; 16 clocks per conversion is typically the fastest that a microcontroller can drive the MAX1112/MAX1113. Figure 12b shows the serial-interface timing necessary to perform a conversion every 16 SCLK cycles in external clock mode.

## Applications Information

### Power-On Reset

When power is first applied, and if $\overline{SHDN}$ is not pulled low, internal power-on reset circuitry activates the MAX1112/MAX1113 in internal clock mode. SSTRB is high on power-up and, if $\overline{CS}$ is low, the first logical 1 on DIN is interpreted as a start bit. Until a conversion takes place, DOUT shifts out zeros. No conversions should be performed until the reference voltage has stabilized (see the Wakeup Time specifications in the *Timing Characteristics*).

### Power-Down

When operating at speeds below the maximum sampling rate, the MAX1112/MAX1113's automatic power-down mode can save considerable power by placing the converters in a low-current shutdown state between conversions. Figure 13 shows the average supply current as a function of the sampling rate.

Select power-down with PD1 of the DIN control byte with $\overline{SHDN}$ high or floating (Table 3). Pull $\overline{SHDN}$ low at any time to shut down the converters completely. $\overline{SHDN}$ overrides PD1 of the control byte. Figures 14a and 14b illustrate the various power-down sequences in both external and internal clock modes.

### Software Power-Down

Software power-down is activated using bit PD1 of the control byte. When software power-down is asserted, the ADCs continue to operate in the last specified clock mode until the conversion is complete. The ADCs then power down into a low quiescent-current state. In internal clock mode, the interface remains active, and conversion results may be clocked out after the MAX1112/MAX1113 have entered a software power-down.

The first logical 1 on DIN is interpreted as a start bit, which powers up the MAX1112/MAX1113. If the DIN byte contains PD1 = 1, then the chip remains powered up. If PD1 = 0, power-down resumes after one conversion.

**Table 5. Hard-Wired Power-Down and Internal Reference State**

| $\overline{SHDN}$ STATE | DEVICE MODE | INTERNAL REFERENCE |
|---|---|---|
| 1 | Enabled | Disabled |
| Floating | Enabled | Enabled |
| 0 | Power-Down | Disabled |

### Hard-Wired Power-Down

Pulling $\overline{SHDN}$ low places the converters in hard-wired power-down. Unlike software power-down, the conversion is not completed; it stops coincidentally with $\overline{SHDN}$ being brought low. $\overline{SHDN}$ also controls the state of the internal reference (Table 5). Letting $\overline{SHDN}$ float enables the internal 4.096V voltage reference. When returning to normal operation with $\overline{SHDN}$ floating, there is a $t_{RC}$ delay of approximately 1MΩ x $C_{LOAD}$, where $C_{LOAD}$ is the capacitive loading on the $\overline{SHDN}$ pin. Pulling $\overline{SHDN}$ high disables the internal reference, which saves power when using an external reference.

### External Reference

An external reference between 1V and $V_{DD}$ should be connected directly at the REFIN terminal. The DC input impedance at REFIN is extremely high, consisting of leakage current only (typically 10nA). During a conversion, the reference must be able to deliver up to 20µA average load current and have an output impedance of 1kΩ or less at the conversion clock frequency. If the reference has higher output impedance or is noisy, bypass it close to the REFIN pin with a 0.1µF capacitor.

If an external reference is used with the MAX1112/MAX1113, tie $\overline{SHDN}$ to $V_{DD}$ to disable the internal reference and decrease power consumption.

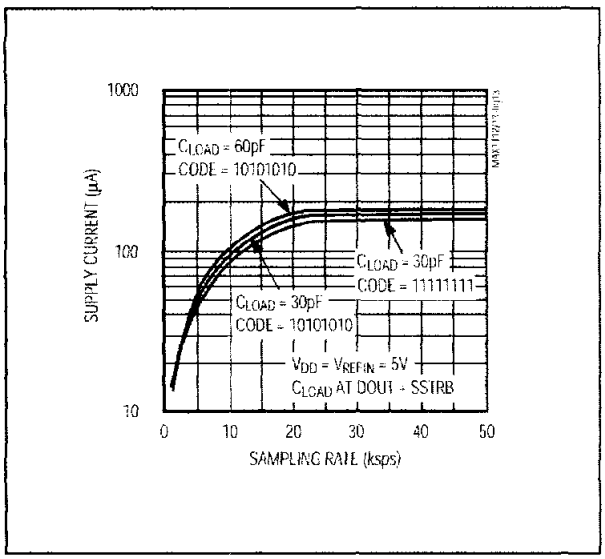



*Figure 13. Average Supply Current vs. Sampling Rate*

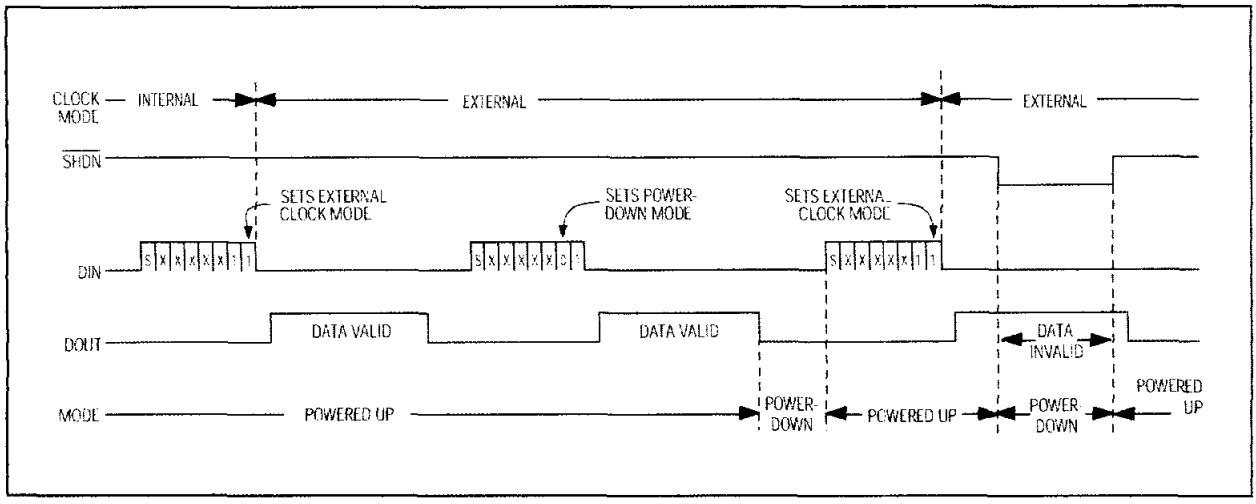



*Figure 14a. Power-Down Modes, External Clock Timing Diagram*

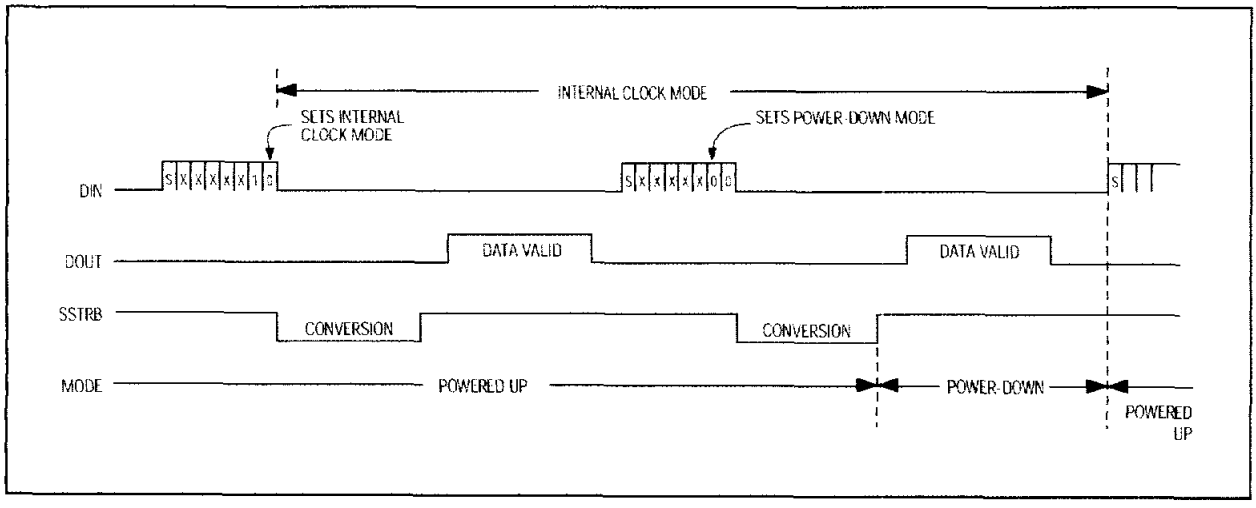



*Figure 14b. Power-Down Modes, Internal Clock Timing Diagram*

### Internal Reference

To use the MAX1112/MAX1113 with the internal reference, connect REFIN to REFOUT. The full-scale range of the MAX1112/MAX1113 with the internal reference is typically 4.096V with unipolar inputs, and ±2.048V with bipolar inputs. The internal reference should be bypassed to AGND with a 1µF capacitor placed as close to the REFIN pin as possible.

### Transfer Function

Table 4 shows the full-scale voltage ranges for unipolar and bipolar modes. Figure 15 depicts the nominal, unipolar I/O transfer function, and Figure 16 shows the bipolar I/O transfer function when using a 4.096V reference. Code transitions occur at integer LSB values. Output coding is binary, with 1LSB = 16mV (4.096V/256) for unipolar operation and 1LSB = 16mV [(4.096V/2 - -4.096V/2)/256] for bipolar operation.

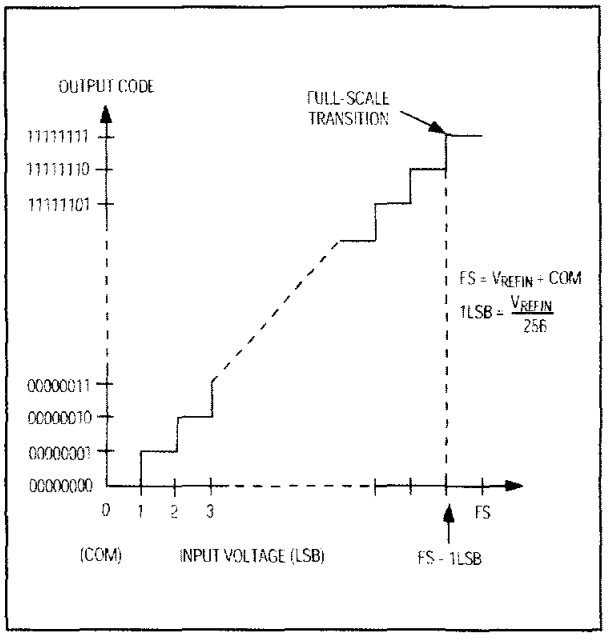



Figure 15. Unipolar Transfer Function

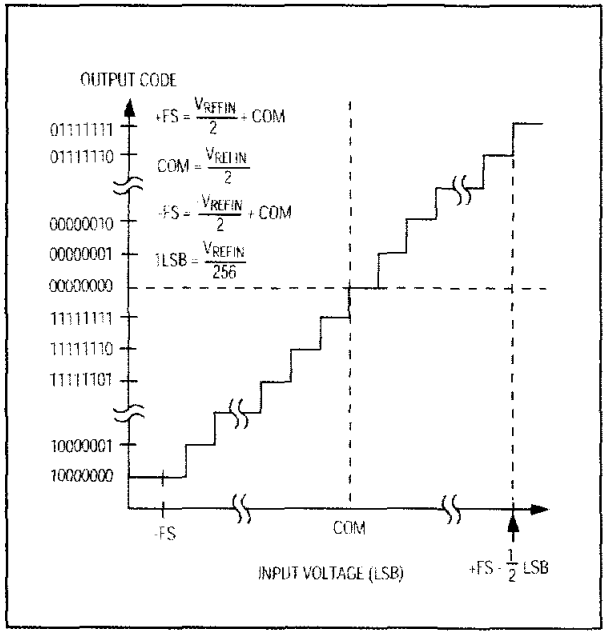



Figure 16. Bipolar Transfer Function

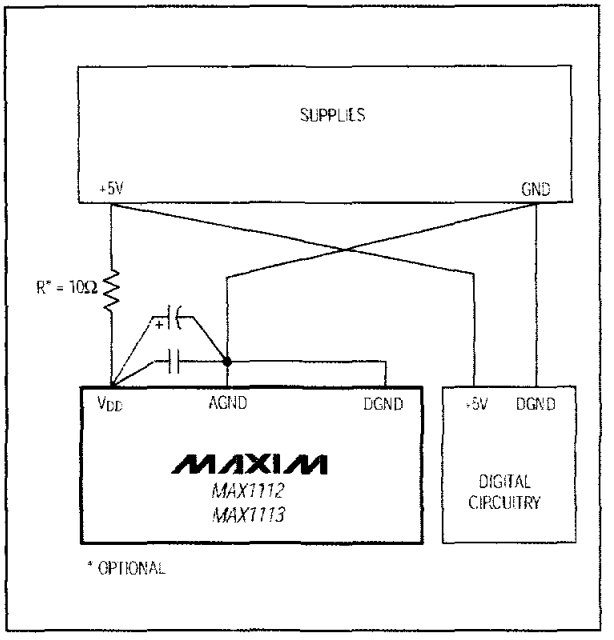



Figure 17. Power-Supply Grounding Connections

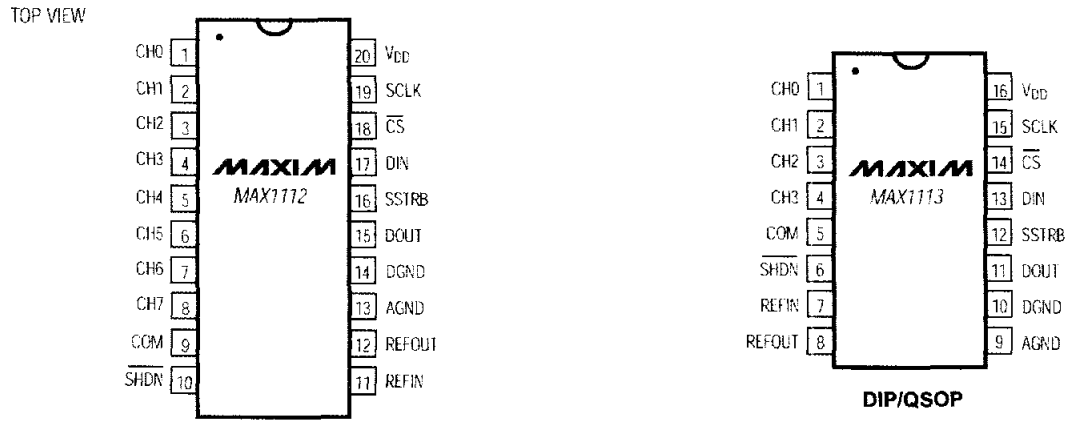
### Layout, Grounding, and Bypassing

For best performance, use printed circuit boards. Wire-wrap boards are not recommended. Board layout should ensure that digital and analog signal lines are separated from each other. Do not run analog and digital (especially clock) lines parallel to one another, or digital lines underneath the ADC package.

Figure 17 shows the recommended system ground connections. A single-point analog ground (star ground point) should be established at AGND, separate from the logic ground. Connect all other analog grounds and DGND to the star ground. No other digital system ground should be connected to this ground. The ground return to the power supply for the star ground should be low impedance and as short as possible for noise-free operation.

High-frequency noise in the $V_{DD}$ power supply may affect the comparator in the ADC. Bypass the supply to the star ground with 0.1µF and 1µF capacitors close to the $V_{DD}$ pin of the MAX1112/MAX1113. Minimize capacitor lead lengths for best supply-noise rejection. If the +5V power supply is very noisy, a 10Ω resistor can be connected to form a lowpass filter.

## Pin Configurations




## Ordering Information (continued)

| PART | TEMP. RANGE | PIN-PACKAGE |
|---|---|---|
| MAX1112EPP | -40°C to +85°C | 20 Plastic DIP |
| MAX1112EAP | -40°C to +85°C | 20 SSOP |
| MAX1112MJP | -55°C to +125°C | 20 CERDIP** |
| **MAX1113**CPE | 0°C to +70°C | 16 Plastic DIP |
| MAX1113CEE | 0°C to +70°C | 16 QSOP |
| MAX1113EPE | -40°C to +85°C | 16 Plastic DIP |
| MAX1113EEE | -40°C to +85°C | 16 QSOP |
| MAX1113MJE | -55°C to +125°C | 16 CERDIP** |

** *Contact factory for availability.*

## Chip Information

TRANSISTOR COUNT: 1996

SUBSTRATE CONNECTED TO DGND

## Features

- **Compatible with MCS-51™ Products**
- **4 Kbytes of In-System Reprogrammable Flash Memory**
  **Endurance: 1,000 Write/Erase Cycles**
- **Fully Static Operation: 0 Hz to 24 MHz**
- **Three-Level Program Memory Lock**
- **128 x 8-Bit Internal RAM**
- **32 Programmable I/O Lines**
- **Two 16-Bit Timer/Counters**
- **Six Interrupt Sources**
- **Programmable Serial Channel**
- **Low Power Idle and Power Down Modes**

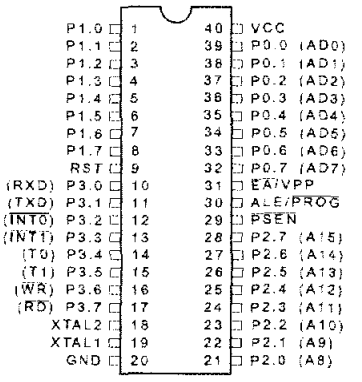
## Description

The AT89C51 is a low-power, high-performance CMOS 8-bit microcomputer with 4 Kbytes of Flash Programmable and Erasable Read Only Memory (PEROM). The device is manufactured using Atmel's high density nonvolatile memory technology and is compatible with the industry standard MCS-51™ instruction set and pinout. The on-chip Flash allows the program memory to be reprogrammed in-system or by a conventional nonvolatile memory programmer. By combining a versatile 8-bit CPU with Flash on a monolithic chip, the Atmel AT89C51 is a powerful microcomputer which provides a highly flexible and cost effective solution to many embedded control applications.

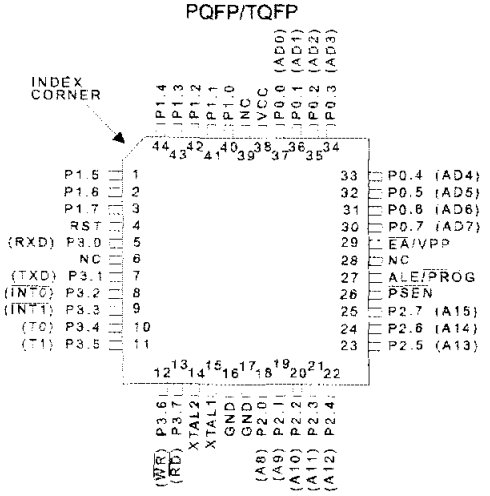
*(continued)*

## Pin Configurations

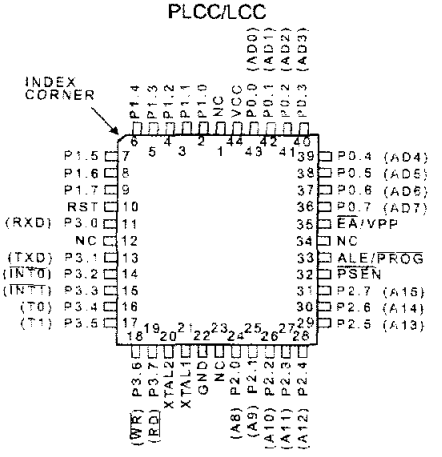
PDIP/Cerdip




PQFP/TQFP




PLCC/LCC

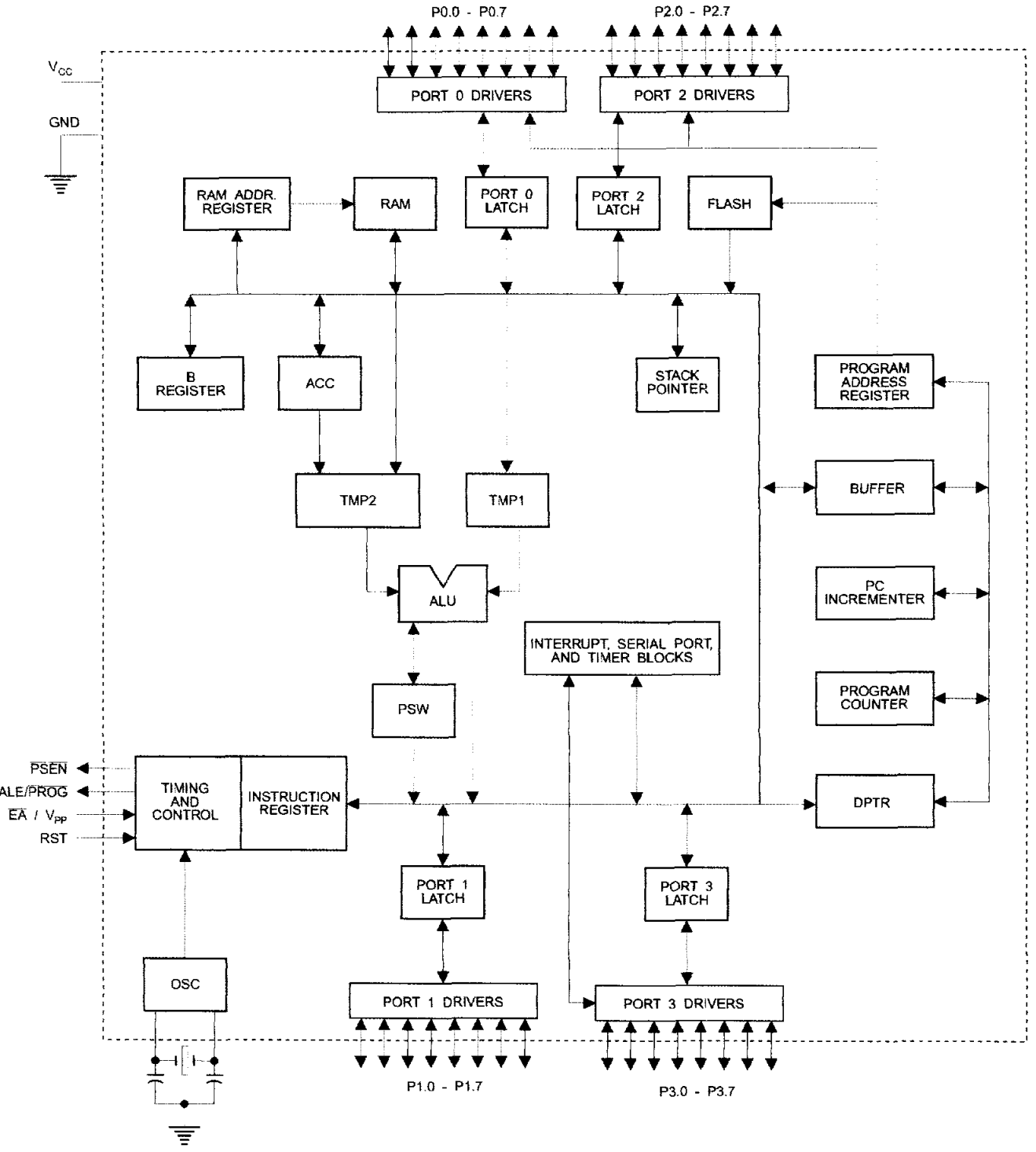



# 8-Bit Microcontroller with 4 Kbytes Flash

# AT89C51

0265E

## Block Diagram



## Description (Continued)

The AT89C51 provides the following standard features: 4 Kbytes of Flash, 128 bytes of RAM, 32 I/O lines, two 16-bit timer/counters, a five vector two-level interrupt architecture, a full duplex serial port, on-chip oscillator and clock circuitry. In addition, the AT89C51 is designed with static logic for operation down to zero frequency and supports two software selectable power saving modes. The Idle Mode stops the CPU while allowing the RAM, timer/counters, serial port and interrupt system to continue functioning. The Power Down Mode saves the RAM contents but freezes the oscillator disabling all other chip functions until the next hardware reset.

## Pin Description

$V_{CC}$

Supply voltage.

GND

Ground.

Port 0

Port 0 is an 8-bit open drain bidirectional I/O port. As an output port each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high-impedance inputs.

Port 0 may also be configured to be the multiplexed low-order address/data bus during accesses to external program and data memory. In this mode P0 has internal pullups.

Port 0 also receives the code bytes during Flash programming, and outputs the code bytes during program verification. External pullups are required during program verification.

Port 1

Port 1 is an 8-bit bidirectional I/O port with internal pullups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current ($I_{IL}$) because of the internal pullups.

Port 1 also receives the low-order address bytes during Flash programming and program verification.

Port 2

Port 2 is an 8-bit bidirectional I/O port with internal pullups. The Port 2 output buffers can sink/source four TTL inputs. When 1s are written to Port 2 pins they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current ($I_{IL}$) because of the internal pullups.

Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application it uses strong internal pullups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

Port 3

Port 3 is an 8-bit bidirectional I/O port with internal pullups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current ($I_{IL}$) because of the pullups.

Port 3 also serves the functions of various special features of the AT89C51 as listed below:

| Port Pin | Alternate Functions |
|---|---|
| P3.0 | RXD (serial input port) |
| P3.1 | TXD (serial output port) |
| P3.2 | $\overline{INT0}$ (extenal interrupt 0) |
| P3.3 | $\overline{INT1}$ (extenal interrupt 1) |
| P3.4 | T0 (timer 0 extenal input) |
| P3.5 | T1 (timer 1 external input) |
| P3.6 | $\overline{WR}$ (extenal data memory write strobe) |
| P3.7 | $\overline{RD}$ (external data memory read strobe) |

Port 3 also receives some control signals for Flash programming and programming verification.

RST

Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device.

ALE/$\overline{PROG}$

Address Latch Enable output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input ($\overline{PROG}$) during Flash programming.

In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external Data Memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcrontroller is in external execution mode.

$\overline{PSEN}$

Program Store Enable is the read strobe to external program memory.

*(continued)*

## Pin Description (Continued)

When the AT89C51 is executing code from external program memory, PSEN is activated twice each machine cycle, except that two PSEN activations are skipped during each access to external data memory.

EA/VPP

External Access Enable. EA must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed, EA will be internally latched on reset.

EA should be strapped to VCC for internal program executions.

This pin also receives the 12-volt programming enable voltage (VPP) during Flash programming, for parts that require 12-volt VPP.

XTAL1

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

XTAL2

Output from the inverting oscillator amplifier.

## Oscillator Characteristics

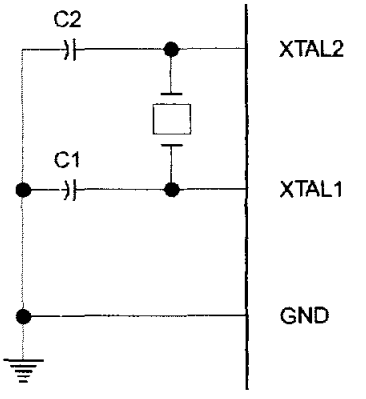
XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier which can be configured for use as an on-chip oscillator, as shown in Figure 1. Either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven as shown in Figure 2. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

## Idle Mode

In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special functions registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

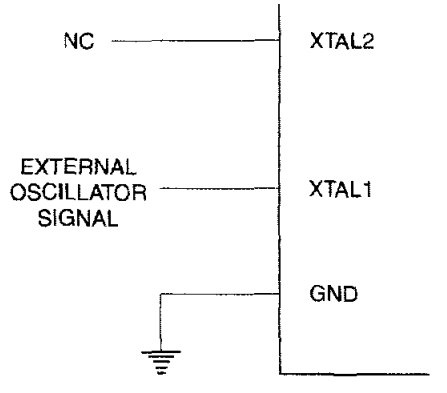
It should be noted that when idle is terminated by a hardware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hard-

**Figure 1.** Oscillator Connections




Notes: C1, C2 = 30 pF ± 10 pF for Crystals
= 40 pF ± 10 pF for Ceramic Resonators

**Figure 2.** External Clock Drive Configuration




## Status of External Pins During Idle and Power Down

| Mode | Program Memory | ALE | PSEN | PORT0 | PORT1 | PORT2 | PORT3 |
|---|---|---|---|---|---|---|---|
| Idle | Internal | 1 | 1 | Data | Data | Data | Data |
| Idle | External | 1 | 1 | Float | Data | Address | Data |
| Power Down | Internal | 0 | 0 | Data | Data | Data | Data |
| Power Down | External | 0 | 0 | Float | Data | Data | Data |

ware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.

## Power Down Mode

In the power down mode the oscillator is stopped, and the instruction that invokes power down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the power down mode is terminated. The only exit from power down is a hardware reset. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before $V_{CC}$ is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

## Program Memory Lock Bits

On the chip are three lock bits which can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in the table below:

When lock bit 1 is programmed, the logic level at the $\overline{EA}$ pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value, and holds that value until reset is activated. It is necessary that the latched value of $\overline{EA}$ be in agreement with the current logic level at that pin in order for the device to function properly.

## Lock Bit Protection Modes

| Program Lock Bits | | | | |
|---|---|---|---|---|
| | LB1 | LB2 | LB3 | Protection Type |
| 1 | U | U | U | No program lock features. |
| 2 | P | U | U | MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, $\overline{EA}$ is sampled and latched on reset, and further programming of the Flash is disabled. |
| 3 | P | P | U | Same as mode 2, also verify is disabled. |
| 4 | P | P | P | Same as mode 3, also external execution is disabled. |

## Programming the Flash

The AT89C51 is normally shipped with the on-chip Flash memory array in the erased state (that is, contents = FFH) and ready to be programmed. The programming interface accepts either a high-voltage (12-volt) or a low-voltage ($V_{CC}$) program enable signal. The low voltage programming mode provides a convenient way to program the AT89C51 inside the user's system, while the high-voltage programming mode is compatible with conventional third party Flash or EPROM programmers.

The AT89C51 is shipped with either the high-voltage or low-voltage programming mode enabled. The respective top-side marking and device signature codes are listed in the following table.

| | $V_{PP}$ = 12 V | $V_{PP}$ = 5 V |
|---|---|---|
| Top-Side Mark | AT89C51<br>xxxx<br>yyww | AT89C51<br>xxxx-5<br>yyww |
| Signature | (030H)=1EH<br>(031H)=51H<br>(032H)=FFH | (030H)=1EH<br>(031H)=51H<br>(032H)=05H |

The AT89C51 code memory array is programmed byte-by-byte in either programming mode. *To program any non-blank byte in the on-chip Flash Memory, the entire memory must be erased using the Chip Erase Mode.*

**Programming Algorithm:** Before programming the AT89C51, the address, data and control signals should be set up according to the Flash programming mode table and Figures 3 and 4. To program the AT89C51, take the following steps.

1. Input the desired memory location on the address lines.
2. Input the appropriate data byte on the data lines.
3. Activate the correct combination of control signals.
4. Raise $\overline{EA}/V_{PP}$ to 12 V for the high-voltage programming mode.
5. Pulse ALE/$\overline{PROG}$ once to program a byte in the Flash array or the lock bits. The byte-write cycle is self-timed and typically takes no more than 1.5 ms. Repeat steps 1 through 5, changing the address and data for the entire array or until the end of the object file is reached.

**Data Polling:** The AT89C51 features $\overline{Data}$ Polling to indicate the end of a write cycle. During a write cycle, an at-



(continued)

## Programming the Flash (Continued)

empted read of the last byte written will result in the complement of the written datum on PO.7. Once the write cycle has been completed, true data are valid on all outputs, and the next cycle may begin. Data Polling may begin any ime after a write cycle has been initiated.

**Ready/Busy**: The progress of byte programming can also be monitored by the RDY/BSY output signal. P3.4 is pulled low after ALE goes high during programming to indicate BUSY. P3.4 is pulled high again when programming is done to indicate READY.

**Program Verify**: If lock bits LB1 and LB2 have not been programmed, the programmed code data can be read back via the address and data lines for verification. The lock bits cannot be verified directly. Verification of the lock bits is achieved by observing that their features are enabled.

**Chip Erase**: The entire Flash array is erased electrically by using the proper combination of control signals and by holding ALE/PROG low for 10 ms. The code array is written with all "1"s. The chip erase operation must be executed before the code memory can be re-programmed.

**Reading the Signature Bytes**: The signature bytes are read by the same procedure as a normal verification of locations 030H,

031H, and 032H, except that P3.6 and P3.7 must be pulled to a logic low. The values returned are as follows.

(030H) = 1EH indicates manufactured by Atmel
(031H) = 51H indicates 89C51
(032H) = FFH indicates 12 V programming
(032H) = 05H indicates 5 V programming

## Programming Interface

Every code byte in the Flash array can be written and the entire array can be erased by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

All major programming vendors offer worldwide support for the Atmel microcontroller series. Please contact your local programming vendor for the appropriate software revision.

## Flash Programming Modes

| Mode | | RST | $\overline{PSEN}$ | ALE/$\overline{PROG}$ | EA/$V_{PP}$ | P2.6 | P2.7 | P3.6 | P3.7 |
|---|---|---|---|---|---|---|---|---|---|
| Write Code Data | | H | L | ⎍ | H/12V[1] | L | H | H | H |
| Read Code Data | | H | L | H | H | L | L | H | H |
| Write Lock | Bit - 1 | H | L | ⎍ | H/12V | H | H | H | H |
| | Bit - 2 | H | L | ⎍ [2] | H/12V | H | H | L | L |
| | Bit - 3 | H | L | ⎍ | H/12V | H | L | H | L |
| Chip Erase | | H | L | ⎍ | H/12V | H | L | L | L |
| Read Signature Byte | | H | L | H | H | L | L | L | L |

Notes: 1. The signature byte at location 032H designates whether $V_{PP}$ = 12 V or $V_{PP}$ = 5 V should be used to enable programming.

2. Chip Erase requires a 10 ms $\overline{PROG}$ pulse.

**Figure 3.** Programming the Flash

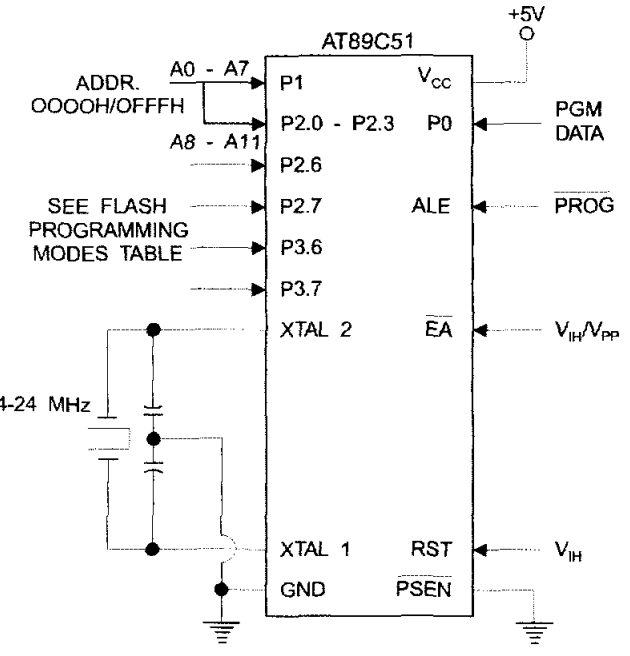
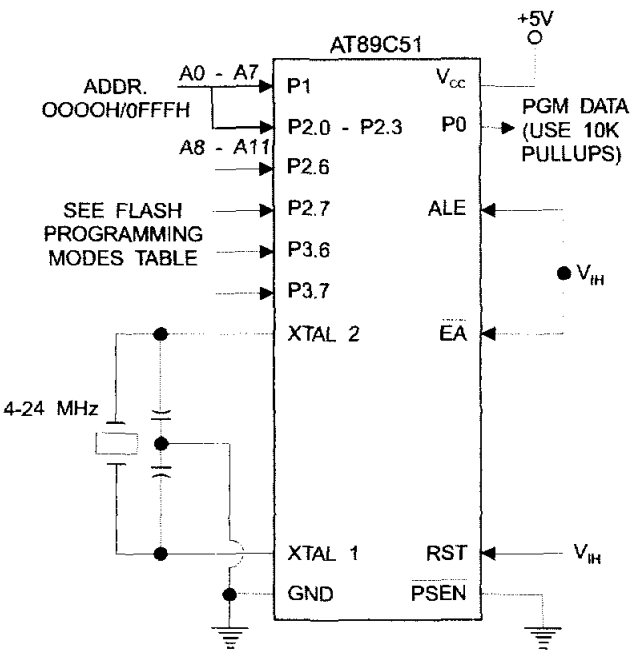



**Figure 4.** Verifying the Flash



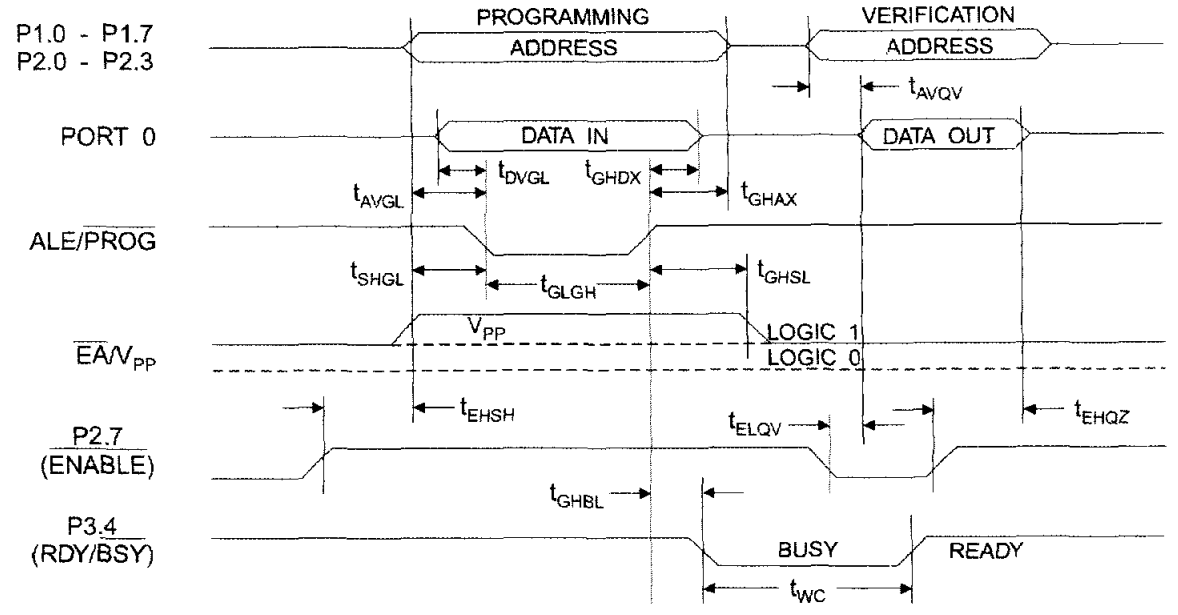

## Flash Programming and Verification Characteristics

$T_A$ = 21°C to 27°C, $V_{CC}$ = 5.0 ± 10%

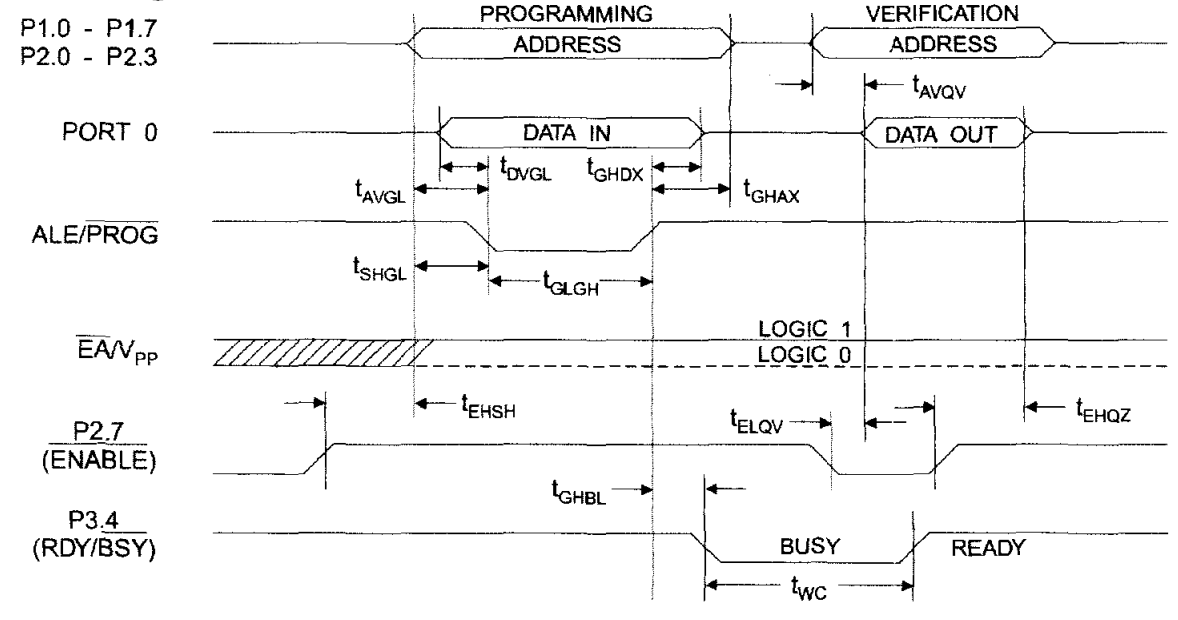
| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $V_{PP}$[1] | Programming Enable Voltage | 11.5 | 12.5 | V |
| $I_{PP}$[1] | Programming Enable Current | | 1.0 | mA |
| $1/t_{CLCL}$ | Oscillator Frequency | 4 | 24 | MHz |
| $t_{AVGL}$ | Address Setup to $\overline{PROG}$ Low | $48t_{CLCL}$ | | |
| $t_{GHAX}$ | Address Hold After $\overline{PROG}$ | $48t_{CLCL}$ | | |
| $t_{DVGL}$ | Data Setup to $\overline{PROG}$ Low | $48t_{CLCL}$ | | |
| $t_{GHDX}$ | Data Hold After $\overline{PROG}$ | $48t_{CLCL}$ | | |
| $t_{EHSH}$ | P2.7 ($\overline{ENABLE}$) High to $V_{PP}$ | 48tCLCL | | |
| $t_{SHGL}$ | $V_{PP}$ Setup to $\overline{PROG}$ Low | 10 | | µs |
| $t_{GHSL}$[1] | $V_{PP}$ Hold After $\overline{PROG}$ | 10 | | µs |
| $t_{GLGH}$ | $\overline{PROG}$ Width | 1 | 110 | µs |
| $t_{AVQV}$ | Address to Data Valid | | 48tCLCL | |
| $t_{ELQV}$ | $\overline{ENABLE}$ Low to Data Valid | | $48t_{CLCL}$ | |
| $t_{EHQV}$ | Data Float After $\overline{ENABLE}$ | 0 | $48t_{CLCL}$ | |
| $t_{GHBL}$ | $\overline{PROG}$ High to $\overline{BUSY}$ Low | | 1.0 | µs |
| $t_{WC}$ | Byte Write Cycle Time | | 2.0 | ms |

Note: 1. Only used in 12-volt programming mode.

## Flash Programming and Verification Waveforms - High Voltage Mode




## Flash Programming and Verification Waveforms - Low Voltage Mode



## Absolute Maximum Ratings*

| | |
|---|---|
| Operating Temperature | -55°C to +125°C |
| Storage Temperature | -65°C to +150°C |
| Voltage on Any Pin with Respect to Ground | -1.0 V to +7.0 V |
| Maximum Operating Voltage | 6.6 V |
| DC Output Current | 15.0 mA |

*NOTICE: *Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## D.C. Characteristics

$T_A$ = -40°C to 85°C, $V_{CC}$ = 5.0 V ± 20% (unless otherwise noted)

| Symbol | Parameter | Condition | Min | Max | Units |
|---|---|---|---|---|---|
| $V_{IL}$ | Input Low Voltage | (Except $\overline{EA}$) | -0.5 | 0.2 $V_{CC}$-0.1 | V |
| $V_{IL1}$ | Input Low Voltage ($\overline{EA}$) | | -0.5 | 0.2 $V_{CC}$-0.3 | V |
| $V_{IH}$ | Input High Voltage | (Except XTAL1, RST) | 0.2 $V_{CC}$+0.9 | $V_{CC}$+0.5 | V |
| $V_{IH1}$ | Input High Voltage | (XTAL1, RST) | 0.7 $V_{CC}$ | $V_{CC}$+0.5 | V |
| $V_{OL}$ | Output Low Voltage[1] (Ports 1,2,3) | $I_{OL}$ = 1.6 mA | | 0.45 | V |
| $V_{OL1}$ | Output Low Voltage[1] (Port 0, ALE, $\overline{PSEN}$) | $I_{OL}$ = 3.2 mA | | 0.45 | V |
| $V_{OH}$ | Output High Voltage (Ports 1,2,3, ALE, $\overline{PSEN}$) | $I_{OH}$ = -60 µA, $V_{CC}$ = 5 V ± 10% | 2.4 | | V |
| | | $I_{OH}$ = -25 µA | 0.75 $V_{CC}$ | | V |
| | | $I_{OH}$ = -10 µA | 0.9 $V_{CC}$ | | V |
| $V_{OH1}$ | Output High Voltage (Port 0 in External Bus Mode) | $I_{OH}$ = -800 µA, $V_{CC}$ = 5 V ± 10% | 2.4 | | V |
| | | $I_{OH}$ = -300 µA | 0.75 $V_{CC}$ | | V |
| | | $I_{OH}$ = -80 µA | 0.9 $V_{CC}$ | | V |
| $I_{IL}$ | Logical 0 Input Current (Ports 1,2,3) | $V_{IN}$ = 0.45 V | | -50 | µA |
| $I_{TL}$ | Logical 1 to 0 Transition Current (Ports 1,2,3) | $V_{IN}$ = 2 V | | -650 | µA |
| $I_{LI}$ | Input Leakage Current (Port 0, EA) | 0.45 < $V_{IN}$ < $V_{CC}$ | | ±10 | µA |
| RRST | Reset Pulldown Resistor | | 50 | 300 | KΩ |
| $C_{IO}$ | Pin Capacitance | Test Freq. = 1 MHz, $T_A$ = 25°C | | 10 | pF |
| $I_{CC}$ | Power Supply Current | Active Mode, 12 MHz | | 20 | mA |
| | | Idle Mode, 12 MHz | | 5 | mA |
| | Power Down Mode[2] | $V_{CC}$ = 6 V | | 100 | µA |
| | | $V_{CC}$ = 3 V | | 40 | µA |

Notes: 1. Under steady state (non-transient) conditions, $I_{OL}$ must be externally limited as follows:
Maximum $I_{OL}$ per port pin:10 mA
Maximum $I_{OL}$ per 8-bit port:
Port 0:26 mA
Ports 1,2, 3:15 mA
Maximum total IOL for all output pins:71 mA
If IOL exceeds the test condition, VOL may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. Minimum VCC for Power Down is 2 V.

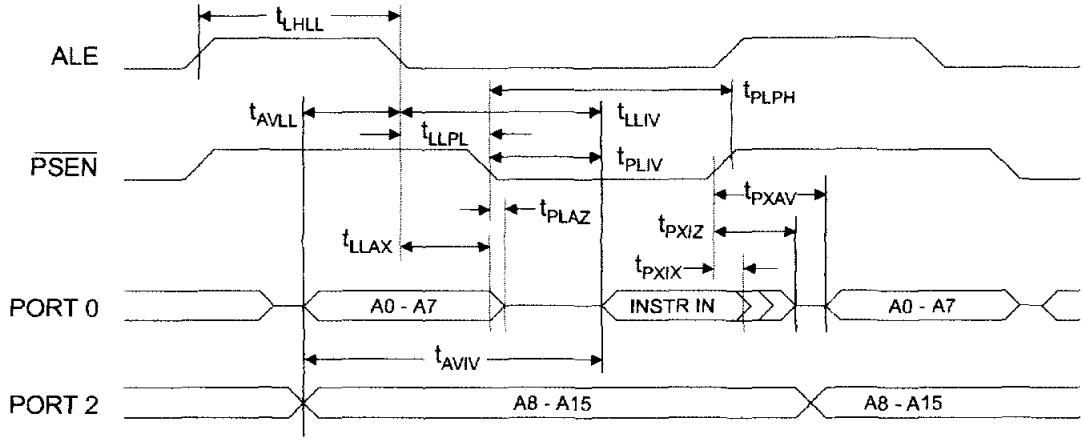
## A.C. Characteristics

Under Operating Conditions; Load Capacitance for Port 0, ALE/$\overline{PROG}$, and $\overline{PSEN}$ = 100 pF; Load Capacitance for all other outputs = 80 pF)

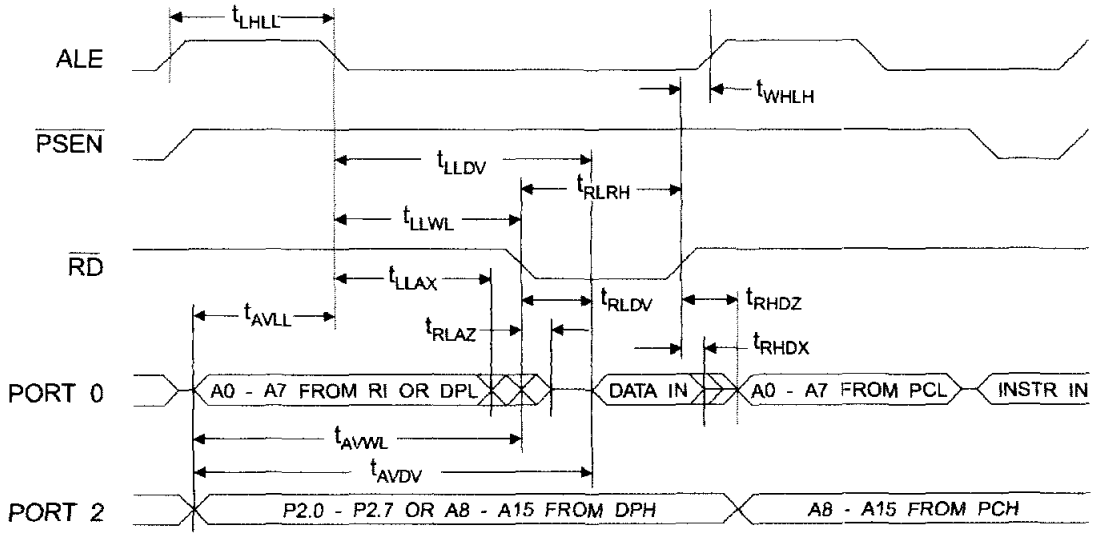
## External Program and Data Memory Characteristics

| Symbol | Parameter | 12 MHz Oscillator | | 16 to 24 MHz Oscillator | | Units |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| $1/t_{CLCL}$ | Oscillator Frequency | | | 0 | 24 | MHz |
| $t_{LHLL}$ | ALE Pulse Width | 127 | | $2t_{CLCL}$-40 | | ns |
| $t_{AVLL}$ | Address Valid to ALE Low | 28 | | tCLCL-13 | | ns |
| $t_{LLAX}$ | Address Hold After ALE Low | 48 | | tCLCL-20 | | ns |
| $t_{LLIV}$ | ALE Low to Valid Instruction In | | 233 | | 4tCLCL-65 | ns |
| $t_{LLPL}$ | ALE Low to $\overline{PSEN}$ Low | 43 | | $t_{CLCL}$-13 | | ns |
| $t_{PLPH}$ | $\overline{PSEN}$ Pulse Width | 205 | | $3t_{CLCL}$-20 | | ns |
| $t_{PLIV}$ | $\overline{PSEN}$ Low to Valid Instruction In | | 145 | | $3t_{CLCL}$-45 | ns |
| $t_{PXIX}$ | Input Instruction Hold After $\overline{PSEN}$ | 0 | | 0 | | ns |
| $t_{PXIZ}$ | Input Instruction Float After $\overline{PSEN}$ | | 59 | | $t_{CLCL}$-10 | ns |
| $t_{PXAV}$ | $\overline{PSEN}$ to Address Valid | 75 | | $t_{CLCL}$-8 | | ns |
| $t_{AVIV}$ | Address to Valid Instruction In | | 312 | | $5t_{CLCL}$-55 | ns |
| $t_{PLAZ}$ | $\overline{PSEN}$ Low to Address Float | | 10 | | 10 | ns |
| $t_{RLRH}$ | $\overline{RD}$ Pulse Width | 400 | | $6t_{CLCL}$-100 | | ns |
| $t_{WLWH}$ | $\overline{WR}$ Pulse Width | 400 | | $6t_{CLCL}$-100 | | ns |
| $t_{RLDV}$ | $\overline{RD}$ Low to Valid Data In | | 252 | | $5t_{CLCL}$-90 | ns |
| $t_{RHDX}$ | Data Hold After $\overline{RD}$ | 0 | | 0 | | ns |
| $t_{RHDZ}$ | Data Float After $\overline{RD}$ | | 97 | | $2t_{CLCL}$-28 | ns |
| $t_{LLDV}$ | ALE Low to Valid Data In | | 517 | | 8tCLCL-150 | ns |
| $t_{AVDV}$ | Address to Valid Data In | | 585 | | 9tCLCL-165 | ns |
| $t_{LLWL}$ | ALE Low to $\overline{RD}$ or $\overline{WR}$ Low | 200 | 300 | $3t_{CLCL}$-50 | $3t_{CLCL}$+50 | ns |
| $t_{AVWL}$ | Address to $\overline{RD}$ or $\overline{WR}$ Low | 203 | | $4t_{CLCL}$-75 | | ns |
| $t_{QVWX}$ | Data Valid to $\overline{WR}$ Transition | 23 | | $t_{CLCL}$-20 | | ns |
| $t_{QVWH}$ | Data Valid to $\overline{WR}$ High | 433 | | $7t_{CLCL}$-120 | | ns |
| $t_{WHQX}$ | Data Hold After $\overline{WR}$ | 33 | | $t_{CLCL}$-20 | | ns |
| $t_{RLAZ}$ | $\overline{RD}$ Low to Address Float | | 0 | | 0 | ns |
| $t_{WHLH}$ | $\overline{RD}$ or $\overline{WR}$ High to ALE High | 43 | 123 | $t_{CLCL}$-20 | $t_{CLCL}$+25 | ns |

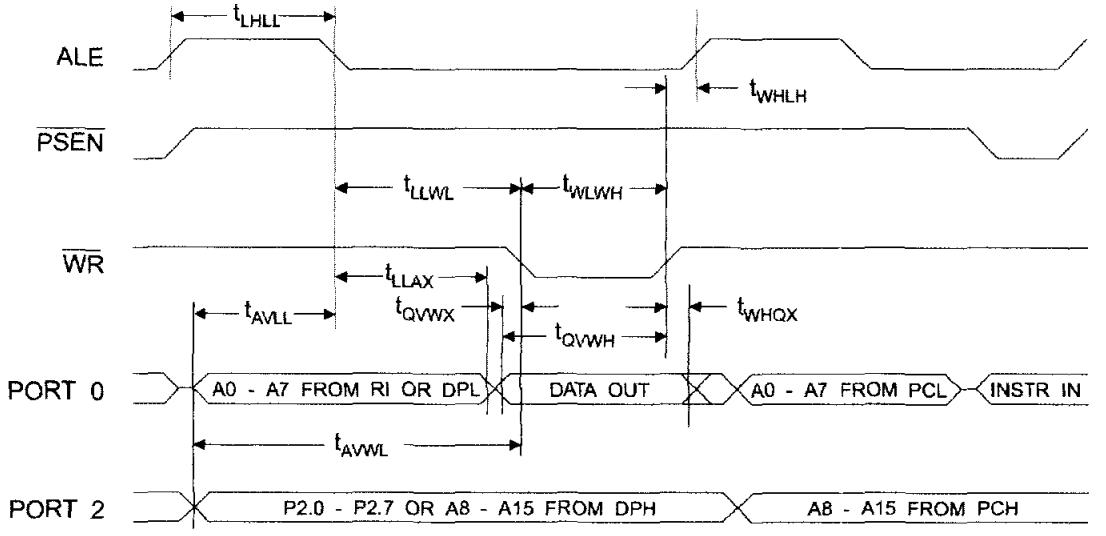
## External Program Memory Read Cycle



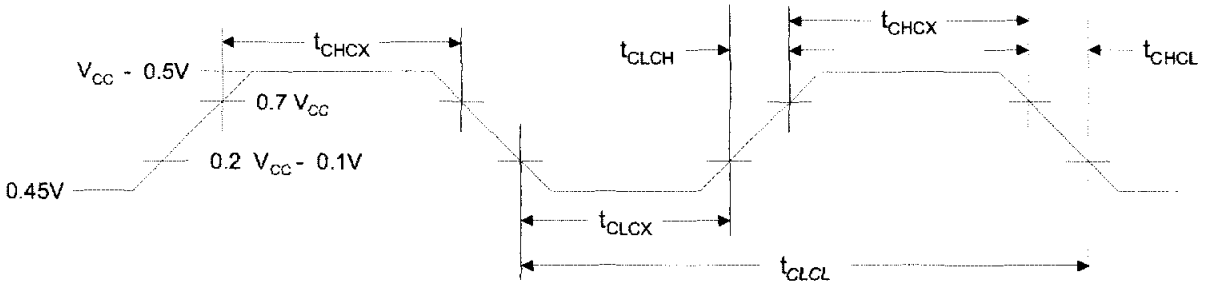

## External Data Memory Read Cycle



## External Data Memory Cycle




## External Clock Drive Waveforms




## External Clock Drive

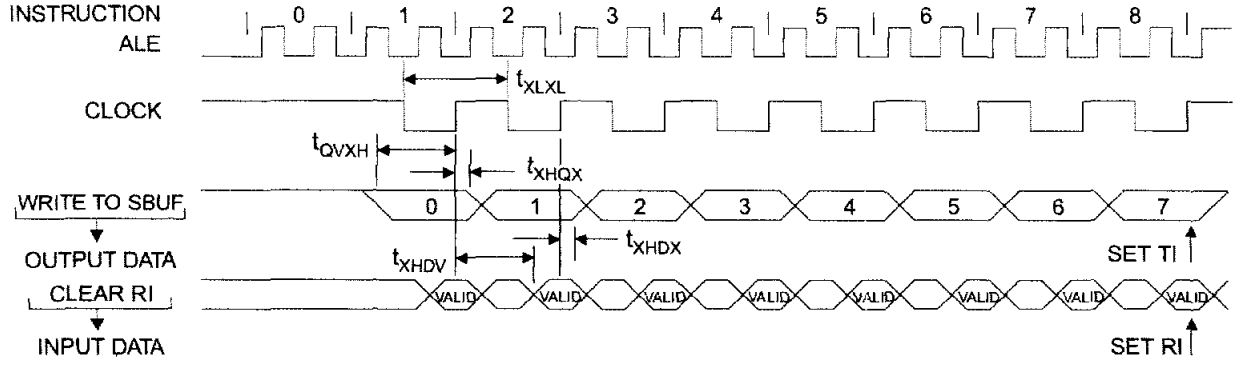
| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| 1/$t_{CLCL}$ | Oscillator Frequency | 0 | 24 | MHz |
| $t_{CLCL}$ | Clock Period | 41.6 | | ns |
| $t_{CHCX}$ | High Time | 15 | | ns |
| $t_{CLCX}$ | Low Time | 15 | | ns |
| $t_{CLCH}$ | Rise Time | | 20 | ns |
| $t_{CHCL}$ | Fall Time | | 20 | ns |

## Serial Port Timing: Shift Register Mode Test Conditions

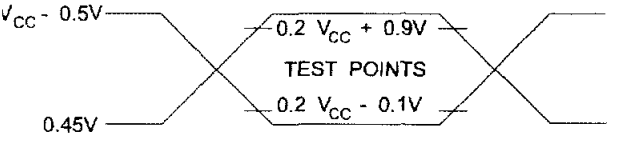
($V_{CC}$ = 5.0 V ± 20%; Load Capacitance = 80 pF)

| Symbol | Parameter | 12 MHz Osc | | Variable Oscillator | | Units |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| $t_{XLXL}$ | Serial Port Clock Cycle Time | 1.0 | | $12t_{CLCL}$ | | µs |
| $t_{QVXH}$ | Output Data Setup to Clock Rising Edge | 700 | | $10t_{CLCL}$-133 | | ns |
| $t_{XHQX}$ | Output Data Hold After Clock Rising Edge | 50 | | $2t_{CLCL}$-33 | | ns |
| $t_{XHDX}$ | Input Data Hold After Clock Rising Edge | 0 | | 0 | | ns |
| $t_{XHDV}$ | Clock Rising Edge to Input Data Valid | | 700 | | 10tCLCL-133 | ns |

## Shift Register Mode Timing Waveforms

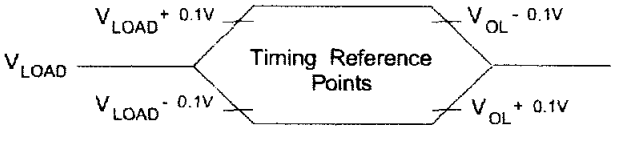



## AC Testing Input/Output Waveforms[1]




Note: 1. AC Inputs during testing are driven at $V_{CC}$ - 0.5 V for a logic 1 and 0.45 V for a logic 0. Timing measurements are made at $V_{IH}$ min. for a logic 1 and $V_{IL}$ max. for a logic 0.

## Float Waveforms[1]




Note: 1. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when a 100 mV change from the loaded $V_{OH}/V_{OL}$ level occurs.

# BIODATA

| | |
|---|---|
| Nama | : Christopher Denny |
| NRP | : 5103095019 |
| NIRM | : 96.7.003.31073.54422 |
| Tempat, Tanggal Lahir | : Surabaya, 10 Desember 1976 |
| Agama | : Katolik |
| Alamat | : Jl. Sawahan Templek IV/21, Sby |

**Riwayat Pendidikan:**

- Tahun 1989 Lulus SDK Don Bosco Surabaya.
- Tahun 1992 Lulus SMPK St. Vincentius Surabaya.
- Tahun 1995 Lulus SMAK St. Louis I Surabaya.
- Tahun 2000 Lulus Sarjana Fakultas Teknik Jurusan Teknik Elektro Universitas Katolik Widya Mandala Surabaya.

**Selama kuliah, aktif sebagai :**

- Anggota Senat Mahasiswa Fakultas Teknik.
- Anggota Unit Kegiatan Mahasiswa Bidang Kerohanian.
- Ketua dan anggota Paduan Suara Mahasiswa Cantate Domino.
- Asisten Praktikum Pengukuran Besaran Listrik di Laboratorium Pengukuran.
- Asisten Praktikum Sistem Intrumentasi Elektronika di Laboratorium Pengukuran.