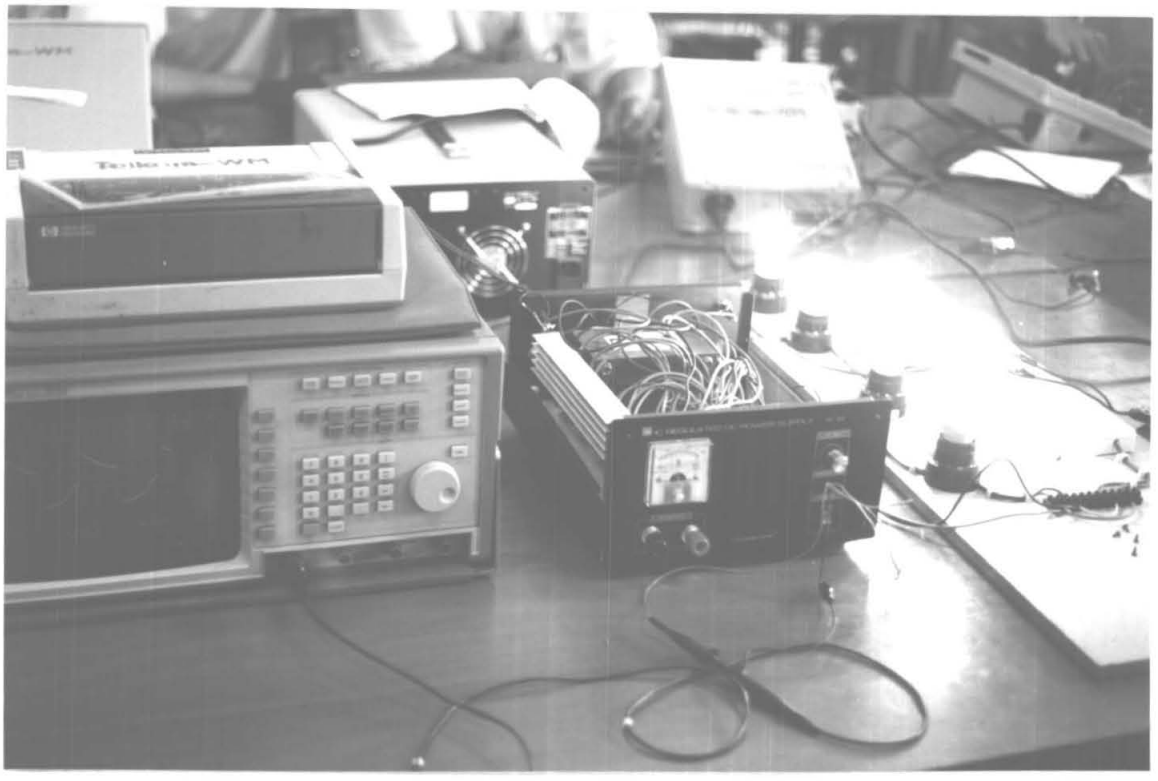
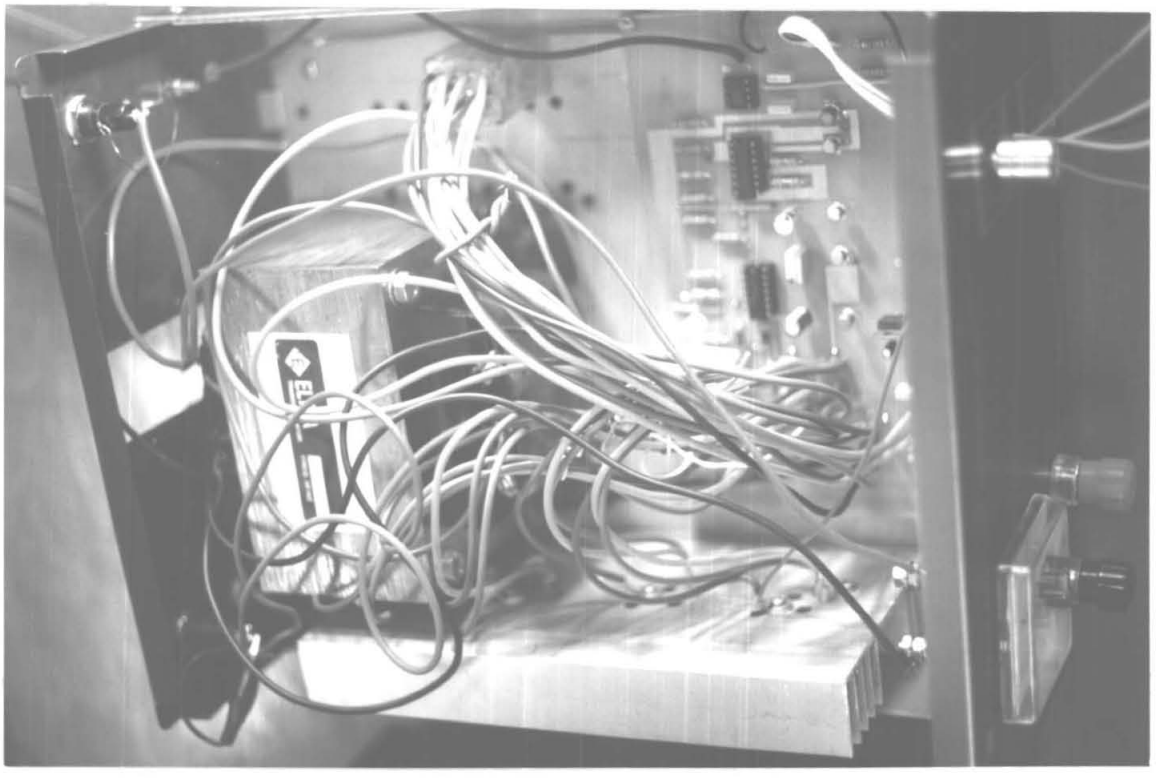
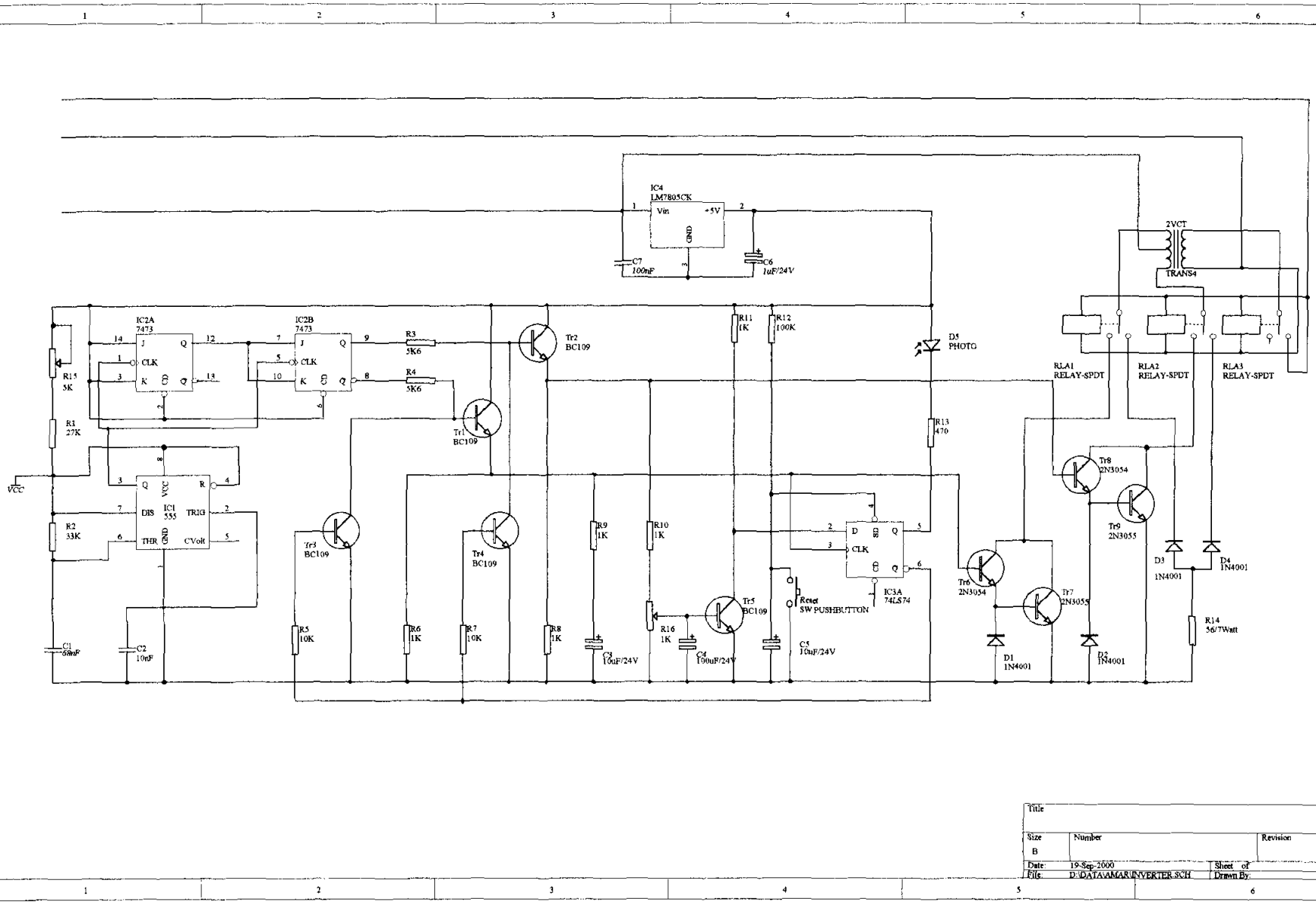
# LAMPIRAN



Gambar 1. Foto Hasil Percobaan Alat dengan Beban Lampu.

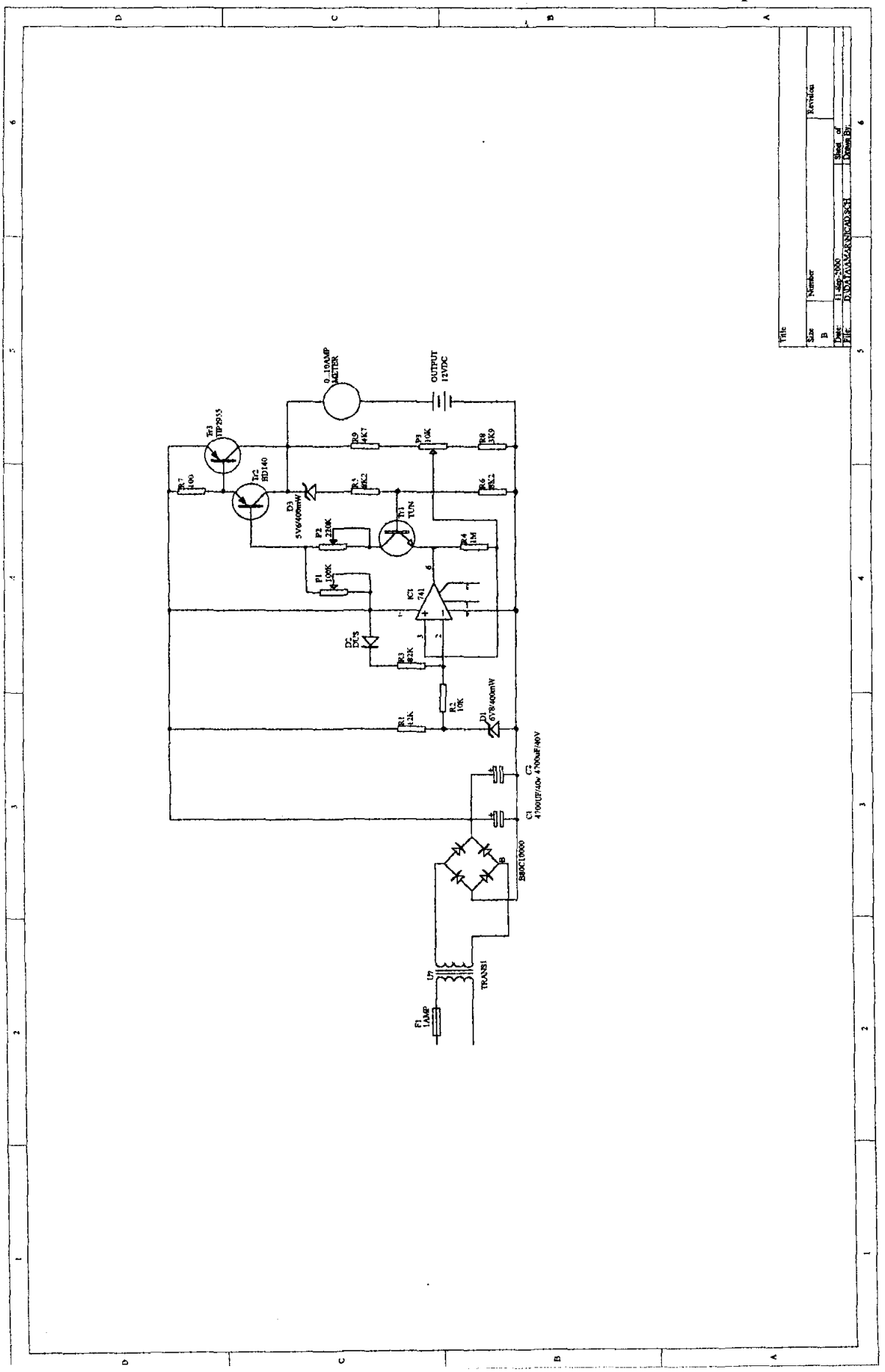


Gambar 2. Foto Desain Alat Pengubah Tegangan DC ke AC


IC4
LM7805CK
Vin
+5V
GND
C7
100nF
C6
1uF/24V
2VCT
TRANS4
IC2A
7473
IC2B
7473
R3
5K6
R4
5K6
Tr2
BC109
Tr1
BC109
R11
1K
R12
100K
D5
PHOTO
RLA1
RELAY-SPDT
RLA2
RELAY-SPDT
RLA3
RELAY-SPDT
R15
5K
R1
27K
R2
33K
IC1
555
VCC
DIS
TRIG
THR
GND
CVolt
R13
470
Tr8
2N3054
Tr9
2N3055
Tr3
BC109
Tr4
BC109
R9
1K
R10
1K
IC3A
74LS74
Reset
SW PUSHBUTTON
Tr5
BC109
Tr6
2N3054
Tr7
2N3055
D3
1N4001
D4
1N4001
R5
10K
R6
1K
R7
10K
R8
1K
R16
1K
C3
10uF/24V
C4
100uF/24V
C5
10uF/24V
C1
58nF
C2
10nF
D1
1N4001
D2
1N4001
R14
56/7Watt
Title
Size
B
Number
Revision
Date:
19-Sep-2000
File:
D:\DATAVAMAR\INVERTER.SCH
Sheet of
Drawn By:

Lampiran 2

**Lampiran 3**


0..10AMP METER
OUTPUT 12VDC
Tr3 TIP3055
Tr2 BD140
D3 5V6/400mW
Tr1 TUN
IC1 741
D2 DUS
D1 6V8/400mW
C2 4700uF/40v
C1 4700UF/40v
BR1 B40C10000
TRANS1
F1 1AMP
Title
Size B
Number
Revision
Date: 11-Sep-2000
File: D:\DOKUMEN\MAKALAH\CAD\SKH
Sheet of
Drawn By:

MOTOROLA

**Lampiran 4**

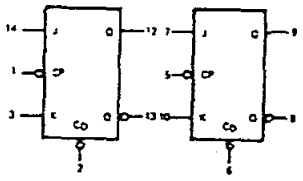
# SN54/74LS73A

## DUAL JK NEGATIVE EDGE-TRIGGERED FLIP-FLOP

LOW POWER SCHOTTKY

**DESCRIPTION** — The SN54LS/74LS73A offers individual J, K, clear, and clock inputs. These dual flip-flops are designed so that when the clock goes HIGH, the inputs are enabled and data will be accepted. The logic level of the J and K inputs may be allowed to change when the clock pulse is HIGH and the bistable will perform according to the truth table as long as minimum set-up times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

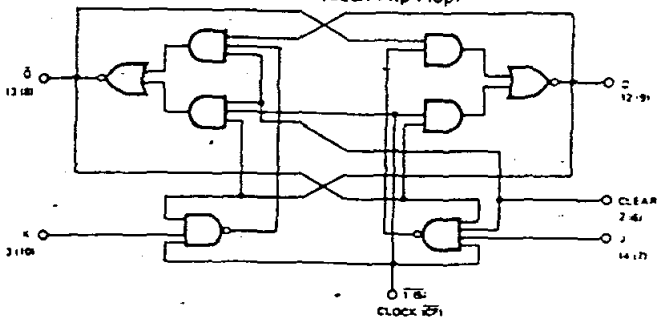
**LOGIC SYMBOL**



$V_{CC}$ = Pin 4
GND = Pin 11

J Suffix — Case 632-08 (Ceramic)
N Suffix — Case 646-06 (Plastic)

**LOGIC DIAGRAM** (Each Flip-Flop)



**DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE** (unless otherwise specified)

| SYMBOL | PARAMETER | | LIMITS MIN | LIMITS TYP | LIMITS MAX | UNITS | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Voltage | | 2.0 | | | V | Guaranteed Input HIGH Voltage for All Inputs |
| $V_{IL}$ | Input LOW Voltage | 54 | | | 0.7 | V | Guaranteed Input LOW Voltage for All Inputs |
| | | 74 | | | 0.8 | | |
| $V_{IK}$ | Input Clamp Diode Voltage | | | −0.65 | −1.5 | V | $V_{CC}$ = MIN, $I_{IN}$ = −18 mA |
| $V_{OH}$ | Output HIGH Voltage | 54 | 2.5 | 3.5 | | V | $V_{CC}$ = MIN, $I_{OH}$ = MAX, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ per Truth Table |
| | | 74 | 2.7 | 3.5 | | V | |
| $V_{OL}$ | Output LOW Voltage | 54,74 | | 0.25 | 0.4 | V | $I_{OL}$ = 4.0 mA; $V_{CC}$ = $V_{CC}$ MIN, $V_{IN}$ = $V_{IL}$ or $V_{IH}$ per Truth Table |
| | | 74 | | 0.35 | 0.5 | V | $I_{OL}$ = 8.0 mA |
| $I_{IH}$ | Input HIGH Current | J, K<br>Clear<br>Clock | | | 20<br>60<br>80 | μA | $V_{CC}$ = MAX, $V_{IN}$ = 2.7 V |
| | | J, K<br>Clear<br>Clock | | | 0.1<br>0.3<br>0.4 | mA | $V_{CC}$ = MAX, $V_{IN}$ = 7.0 V |
| $I_{IL}$ | Input LOW Current | J, K<br>Clear, Clock | | | −0.4<br>−0.8 | mA | $V_{CC}$ = MAX, $V_{IN}$ = 0.4 V |
| $I_{OS}$ | Short Circuit Current | | −20 | | −100 | mA | $V_{CC}$ = MAX |
| $I_{CC}$ | Power Supply Current | | | | 6.0 | mA | $V_{CC}$ = MAX |

## MODE SELECT – TRUTH TABLE

| OPERATING MODE | INPUTS | | | OUTPUTS | |
|---|---|---|---|---|---|
| | $\overline{C}_D$ | J | K | Q | $\overline{Q}$ |
| Reset (Clear) | L | X | X | L | H |
| Toggle | H | h | h | $\overline{q}$ | q |
| Load "0" (Reset) | H | l | h | L | H |
| Load "1" (Set) | H | h | l | H | L |
| Hold | H | l | l | q | $\overline{q}$ |

H, h = HIGH Voltage Level
L, l = LOW Voltage Level
X = Don't Care
l, h (q) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the HIGH to LOW clock transition.

## GUARANTEED OPERATING RANGES

| SYMBOL | PARAMETER | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | 54<br>74 | 4.5<br>4.75 | 5.0<br>5.0 | 5.5<br>5.25 | V |
| $T_A$ | Operating Ambient Temperature Range | 54<br>74 | −55<br>0 | 25<br>25 | 125<br>70 | °C |
| $I_{OH}$ | Output Current — High | 54, 74 | | | −0.4 | mA |
| $I_{OL}$ | Output Current — Low | 54<br>74 | | | 4.0<br>8.0 | mA |

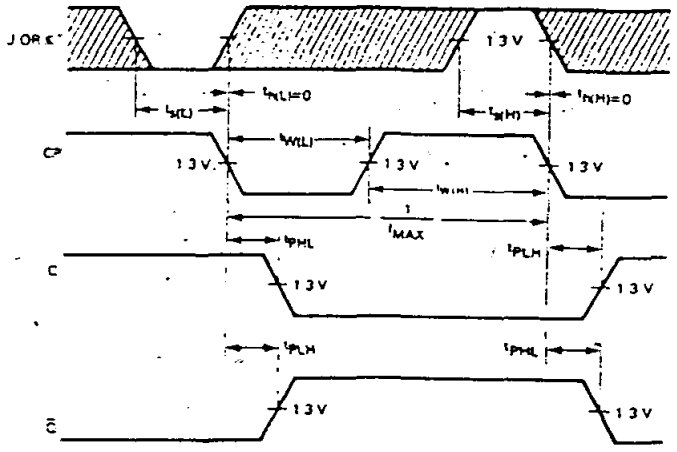
## AC CHARACTERISTICS: $T_A = 25°C$, $V_{CC} = 5.0\ V$

| SYMBOL | PARAMETER | LIMITS | | | UNITS | TEST CONDITIONS | |
|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | | | |
| $f_{MAX}$ | Maximum Clock Frequency | 30 | 45 | | MHz | Fig. 1 | $V_{CC} = 5.0\ V$<br>$C_L = 15\ pF$ |
| $t_{PLH}$ | Propagation Delay, | | 15 | 20 | ns | Fig. 1 | |
| $t_{PHL}$ | Clock to Output | | 15 | 20 | ns | | |

## AC SETUP REQUIREMENTS: $T_A = 25°C$

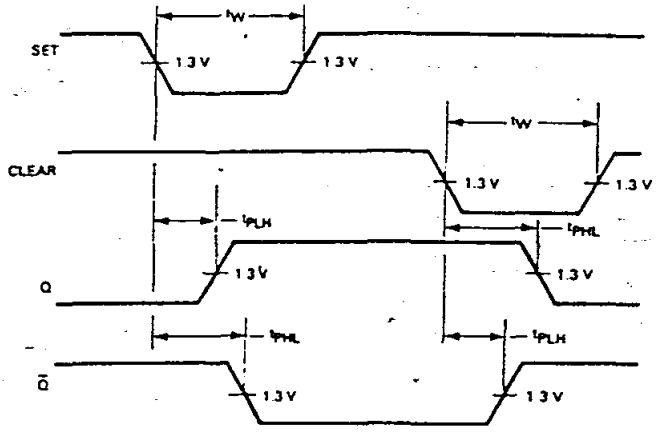
| SYMBOL | PARAMETER | LIMITS | | | UNITS | TEST CONDITIONS | |
|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | | | |
| $t_W$ | Clock Pulse Width High | 20 | | | ns | Fig. 1 | $V_{CC} = 5.0\ V$ |
| $t_W$ | Clear Pulse Width | 25 | | | ns | Fig. 2 | |
| $t_s$ | Setup Time | 20 | | | ns | Fig. 1 | |
| $t_h$ | Hold Time | 0 | | | ns | | |

Fig. 1 CLOCK TO OUTPUT DELAYS, DATA SET-UP AND HOLD TIMES, CLOCK PULSE WIDTH




*The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig. 2 SET AND CLEAR TO OUTPUT DELAYS, SET AND CLEAR PULSE WIDTHS



MOTOROLA

# SN54/74LS74A

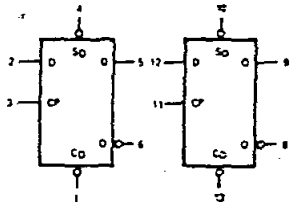
DESCRIPTION - The SN54LS/74LS74A dual edge-triggered flip-flop utilizes Schottky TTL circuitry to produce high speed D-type flip-flops. Each flip-flop has individual clear and set inputs, and also complementary Q and $\overline{Q}$ outputs.

Information at input D is transferred to the Q output on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the HIGH or the LOW level, the D input signal has no effect.

## DUAL D-TYPE POSITIVE EDGE-TRIGGERED FLIP-FLOP

LOW POWER SCHOTTKY

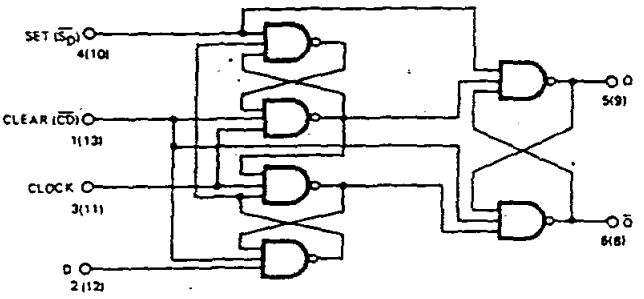
LOGIC SYMBOL



$V_{CC}$ = Pin 14
GND = Pin 7

J Suffix — Case 632-08 (Ceramic)
N Suffix — Case 646-06 (Plastic)

LOGIC DIAGRAM
(EACH FLIP-FLOP)




**DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE** (unless otherwise specified)

| SYMBOL | PARAMETER | | LIMITS MIN | LIMITS TYP | LIMITS MAX | UNITS | TEST CONDITIONS |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Voltage | | 2.0 | | | V | Guaranteed Input HIGH Voltage for All Inputs |
| $V_{IL}$ | Input LOW Voltage | 54 | | | 0.7 | V | Guaranteed Input LOW Voltage for All Inputs |
| | | 74 | | | 0.8 | | |
| $V_{IK}$ | Input Clamp Diode Voltage | | | −0.65 | −1.5 | V | $V_{CC}$ = MIN, $I_{IN}$ = −18 mA |
| $V_{OH}$ | Output HIGH Voltage | 54 | 2.5 | 3.5 | | V | $V_{CC}$ = MIN, $I_{OH}$ = MAX, $V_{IN}$ = $V_{IH}$ or $V_{IL}$ per Truth Table |
| | | 74 | 2.7 | 3.5 | | V | |
| $V_{OL}$ | Output LOW Voltage | 54,74 | | 0.25 | 0.4 | V | $I_{OL}$ = 4.0 mA; $V_{CC}$ = $V_{CC}$ MIN, $V_{IN}$ = $V_{IL}$ or $V_{IH}$ per Truth Table |
| | | 74 | | 0.35 | 0.5 | V | $I_{OL}$ = 8.0 mA |
| $I_{IH}$ | Input High Current<br>Data, Clock<br>Set, Clear | | | | 20<br>40 | μA | $V_{CC}$ = MAX, $V_{IN}$ = 2.7 V |
| | Data, Clock<br>Set, Clear | | | | 0.1<br>0.2 | mA | $V_{CC}$ = MAX, $V_{IN}$ = 7.0 V |
| $I_{IL}$ | Input LOW Current<br>Data, Clock<br>Set, Clear | | | | −0.4<br>−0.8 | mA | $V_{CC}$ = MAX, $V_{IN}$ = 0.4 V |
| $I_{OS}$ | Output Short Circuit Current | | −20 | | −100 | mA | $V_{CC}$ = MAX |
| $I_{CC}$ | Power Supply Current | | | | 8.0 | mA | $V_{CC}$ = MAX |

## MODE SELECT — TRUTH TABLE

| OPERATING MODE | INPUTS | | | OUTPUTS | |
|---|---|---|---|---|---|
| | $\overline{S}_D$ | $\overline{C}_D$ | D | Q | $\overline{Q}$ |
| Set | L | H | X | H | L |
| Reset (Clear) | H | L | X | L | H |
| *Undetermined | L | L | X | H | H |
| Load "1" (Set) | H | H | h | H | L |
| Load "0" (Reset) | H | H | l | L | H |

*Both outputs will be HIGH while both $\overline{S}_D$ AND $\overline{C}_D$ are LOW, but the output states are unpredictable if $\overline{S}_D$ and $\overline{C}_D$ go HIGH simultaneously. If the levels at the set and clear are near $V_{IL}$ maximum then we cannot guarantee to meet the minimum level for $V_{OH}$.

H, h = HIGH Voltage Level
L, l = LOW Voltage Level
X = Don't Care
i, h (q) = Lower case letters indicate the state of the referenced input (or output) one set-up time prior to the LOW to HIGH clock transition.

## GUARANTEED OPERATING RANGES

| SYMBOL | PARAMETER | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | 54<br>74 | 4.5<br>4.75 | 5.0<br>5.0 | 5.5<br>5.25 | V |
| $T_A$ | Operating Ambient Temperature Range | 54<br>74 | −55<br>0 | 25<br>25 | 125<br>70 | °C |
| $I_{OH}$ | Output Current — High | 54, 74 | | | −0.4 | mA |
| $I_{OL}$ | Output Current — Low | 54<br>74 | | | 4.0<br>8.0 | mA |

## AC CHARACTERISTICS: $T_A = 25°C$, $V_{CC} = 5.0$ V

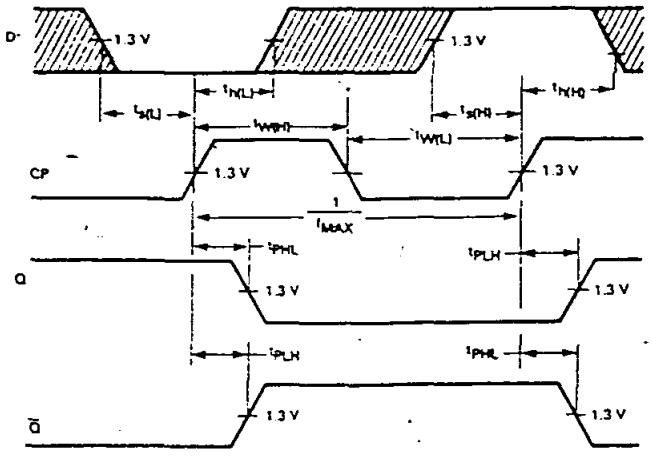
| SYMBOL | PARAMETER | LIMITS | | | UNITS | TEST CONDITIONS | |
|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | | | |
| $f_{MAX}$ | Maximum Clock Frequency | 25 | 33 | | MHz | Fig. 1 | $V_{CC} = 5.0$ V, $C_L = 15$ pF |
| $t_{PLH}$ | Clock, Clear, Set to Output | | 13 | 25 | ns | Fig. 1 | |
| $t_{PHL}$ | | | 25 | 40 | ns | | |

## AC SETUP REQUIREMENTS: $T_A = 25°C$, $V_{CC} = 5.0$ V

| SYMBOL | PARAMETER | LIMITS | | | UNITS | TEST CONDITIONS | |
|---|---|---|---|---|---|---|---|
| | | MIN | TYP | MAX | | | |
| $t_{W(H)}$ | Clock | 25 | | | ns | Fig. 1 | $V_{CC} = 5.0$ V |
| $t_{W(L)}$ | Clear, Set | 25 | | | ns | Fig. 2 | |
| $t_s$ | Data Setup Time — HIGH | 20 | | | ns | Fig. 1 | |
| | LOW | 20 | | | ns | | |
| $t_h$ | Hold Time | 5.0 | | | ns | Fig. 1 | |

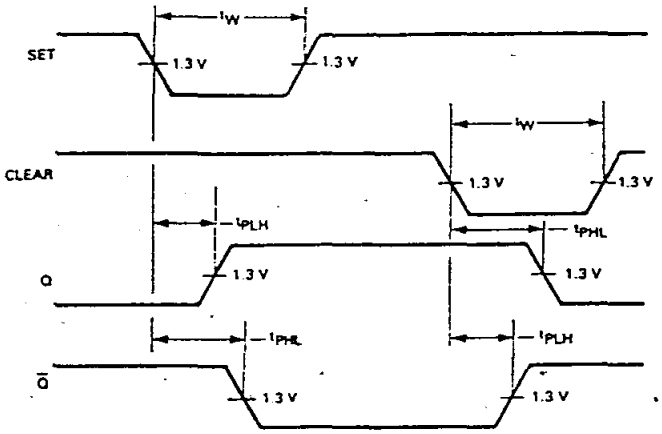
## AC WAVEFORMS

**Fig. 1 CLOCK TO OUTPUT DELAYS, DATA SET-UP AND HOLD TIMES, CLOCK PULSE WIDTH**




*The shaded areas indicate when the input is permitted to change for predictable output performance.

**Fig. 2 SET AND CLEAR TO OUTPUT DELAYS, SET AND CLEAR PULSE WIDTHS**



# BIODATA

# BIODATA

| | |
|---|---|
| Nama Lengkap | : **AMAR DIYANTO** |
| Nrp | : 94.7.003.31073.06070 |
| Tempat, Tanggal Lahir | : Surabaya, 24 Maret 1974 |
| Agama | : Islam |
| Alamat Rumah | : Dupak Masigit IX / 35 Surabaya |

**Riwayat Pendidikan :**

- SDN Kemayoran I Surabaya, lulus tahun 1987
- SMP Kemala Bhayangkari Surabaya, lulus tahun 1990
- STM Negeri 2 Surabaya, lulus tahun 1993
- Universitas Katolik Widya Mandala Fakultas Teknik Jurusan Teknik Elektro, Surabaya, angkatan 1994.