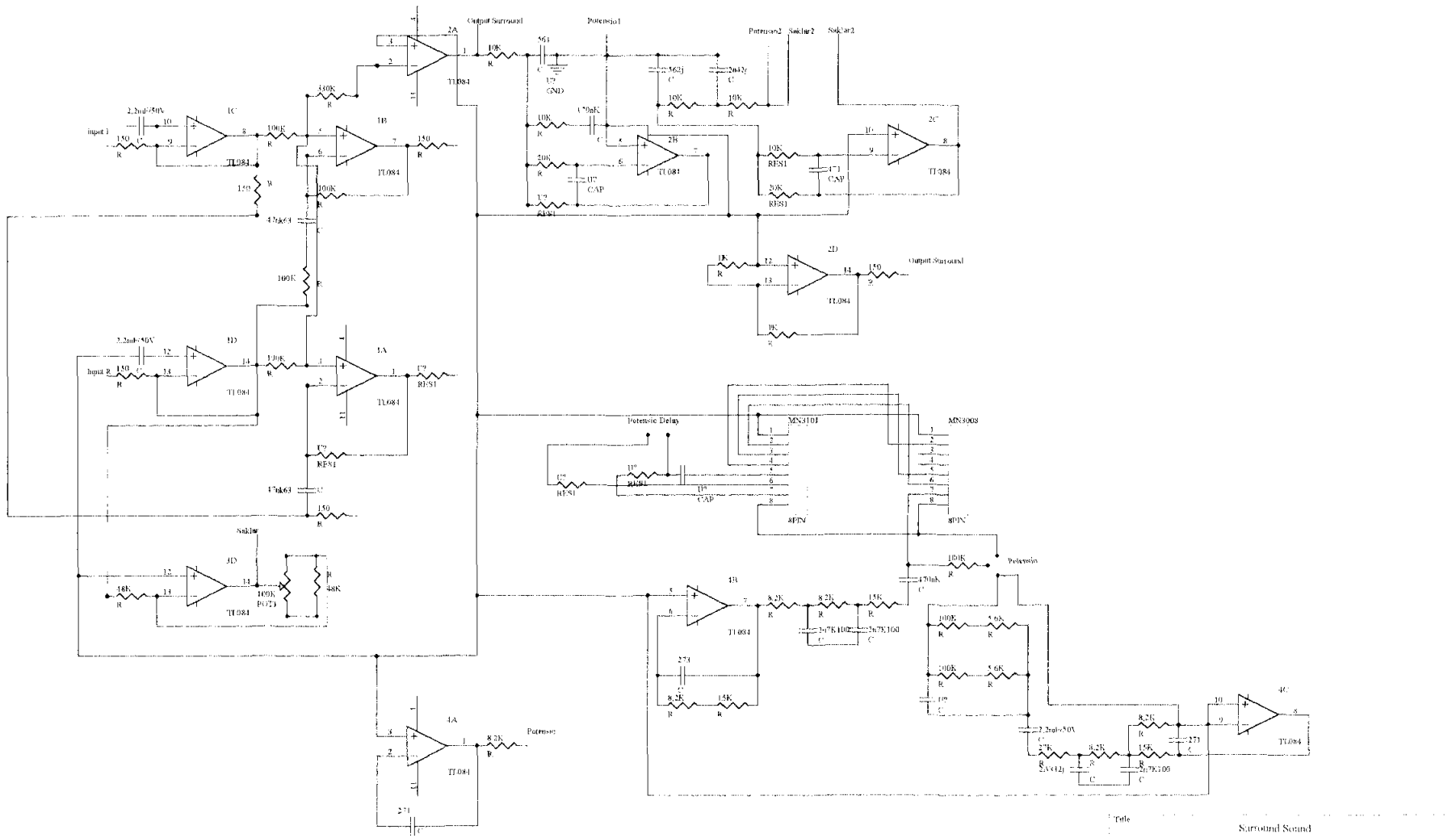
LAMPIRAN


Output Surround
Potensio1
Potensio2
Saklar2
Saklar2
input L
input R
TL084
MN3101
MN3008
Potensio Delay
Potensio
Saklar
Output Surround
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MN3008

2048-STAGE LOW NOISE BBD

■ General description

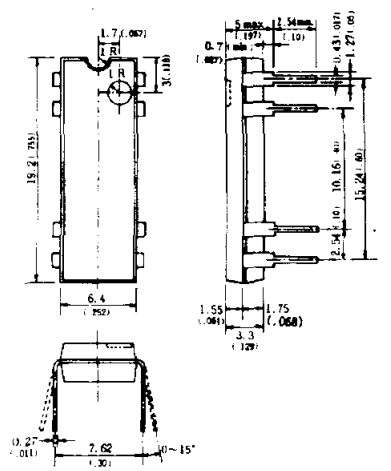
The MN3008 is a 2048-stage long delay low noise BBD that provides a signal delay of up to 102.4msec.

The MN3008 is particularly suitable for use as reverberation effect in electronic musical instruments such as stereo equipment due to its long delay time.

■ Features

- Variable delay time of audio signal: 10.24 ~ 102.4ms.
- Clock component cancellation capability.
- No insertion loss: L_i = 0dB typ.
- Wide dynamic range: S/N = 78dB typ.
- Wide frequency response: $f_i \leqq$ 10KHz.
- Low distortion: THD = 0.5% typ. (V_i = 0.78Vrms).
- Clock frequency range: 10 ~ 100KHz.
- P channel silicon gate process.
- Special 8-Lead Dual-In-Line Plastic Package.

Unit: mm (inch)

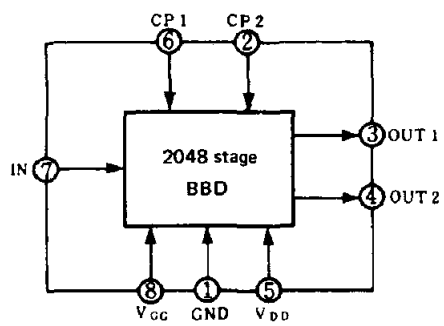


Special 8-Lead Dual-In-Line Plastic Package

■ Applications

- Reverberation effect of echo microphone and stereo equipments.
- Chorus effects in electronic musical instruments.
- Variable or fixed delay of analog signals.
- Telephone time compression and delay line for voice communication systems, etc.

■ Block Diagram



■ Quick Reference Data

Item	Symbol	Value	Unit
Supply Voltage	V_{DD}, V_{GG}	−15, V_{DD} + 1	V
Signal Delay Time	t_D	10.24~102.4	ms
Total Harmonic Distortion	THD	0.5	%
Signal to Noise Ratio	S/N	78	dB

■ Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Ratings	Unit
Terminal Voltage	V_{DD}, V_{GG}, V_{CP}, V_i	−18～+0.3	V
Output Voltage	V_O	−18～+0.3	V
Operating Temperature	Topr	−20～+60	℃
Storage Temperature	Tstg	−55～+125	℃

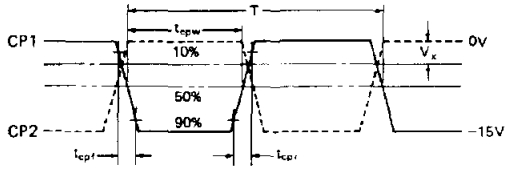
■ Operating Conditions (Ta = 25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Drain Supply Voltage	V_{DD}		−14	−15	−16	V
Gate Supply Voltage	V_{GG}			$V_{DD}+1$		V
Clock Voltage "H" Level	V_{CPH}		0		−1	V
Clock Voltage "L" Level	V_{CPL}			V_{DD}		V
Clock Input Capacitance	C_{CP}				1400	pF
Clock Frequency	f_{CP}		10		100	kHz
Clock Pulse Width *1	t_{cpw}				0.5T*2	
Clock Rise Time *1	t_{cpr}				500	ns
Clock Fall Time *1	t_{cpf}				500	ns
Clock Cross Point *1	V_X		0		−3	V
Input DC Bias	V_{Bias}		−5		−10	V

■ Electrical Characteristics (Ta = 25°C, $V_{DD} = V_{CPL} = -15V$, $V_{CPH} = 0V$, $V_{GG} = -14V$, $R_L = 100k\Omega$)

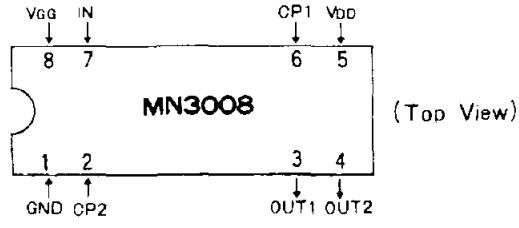
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Signal Delay Time	t_D		10.24		102.4	ms
Input Signal Frequency	f_i	f_{cp} = 40kHz, V_i = 1.7Vrms 3dB down (0dB at f_i = 1kHz)	10			kHz
Input Signal Swing	V_i	f_{CP}=40kHz, f_i = 1 kHz, THD=2.5%	1.2			Vrms
Insertion Loss	L_i	f_{CP}=40kHz, f_i = 1 kHz, V_i =1.2Vrms	−4	0	+4	dB
Total Harmonic Distortion	THD	f_{CP}=40kHz, f_i = 1 kHz, V_i =0.78Vrms		0.5	2.5	%
Noise	V_{no}	f_{cp} = 100kHz, weighted by "A" curve			0.4	mVrms
Signal to Noise Ratio	S/N			78		dB

*1 Clock Pulse Waveforms

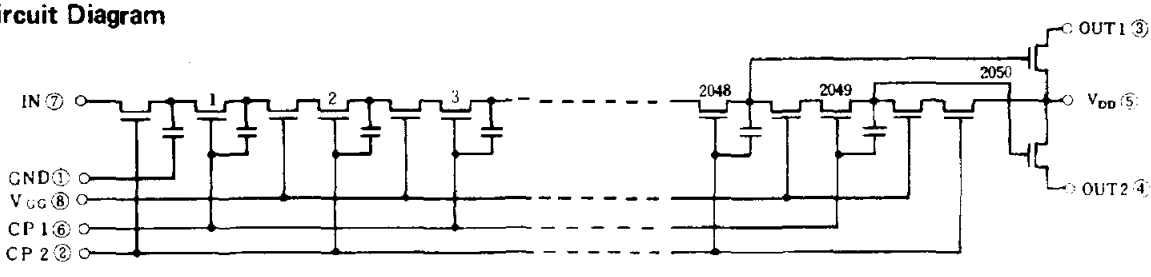


*2 T = $1/f_{CP}$ (Clock period)

■ Terminal Assignments

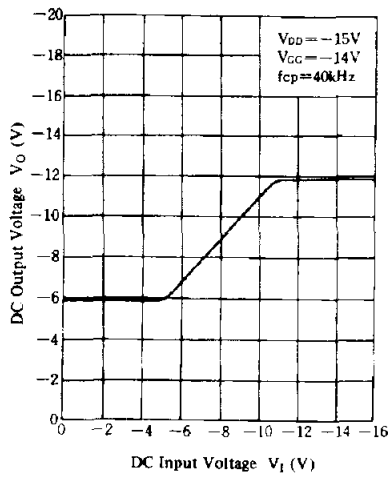


■ Circuit Diagram

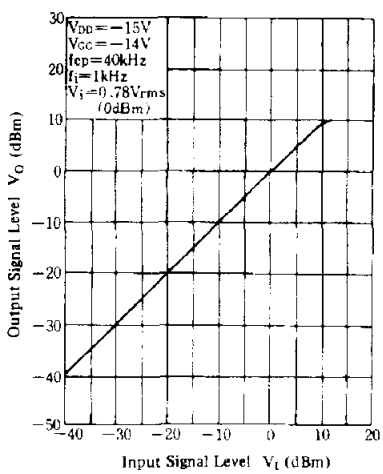


■ Typical Electrical Characteristic Curves

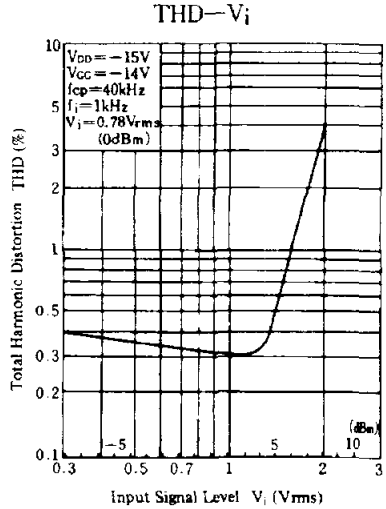
V_O—V_I



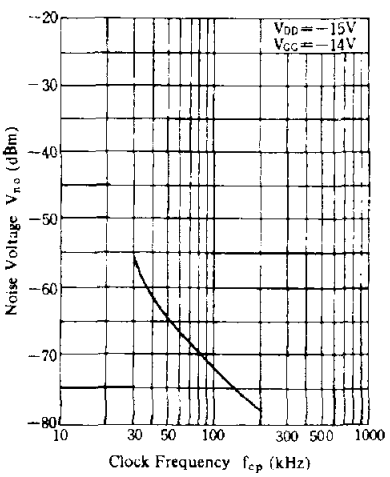
V_O—V_i



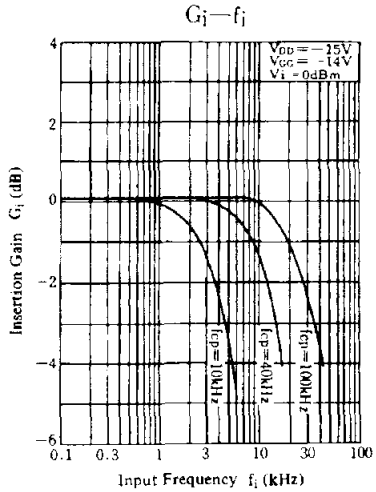
THD—V_i



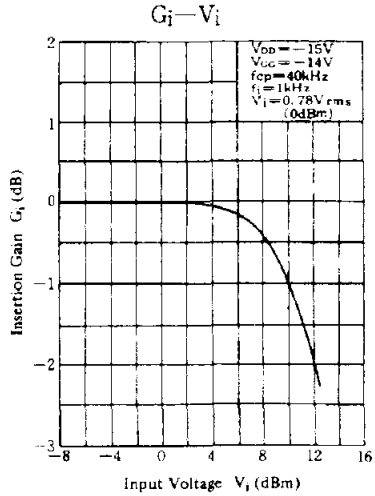
V_{no}—fcp



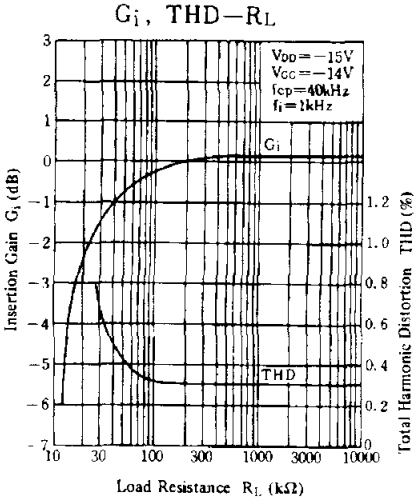
G_i—f_i



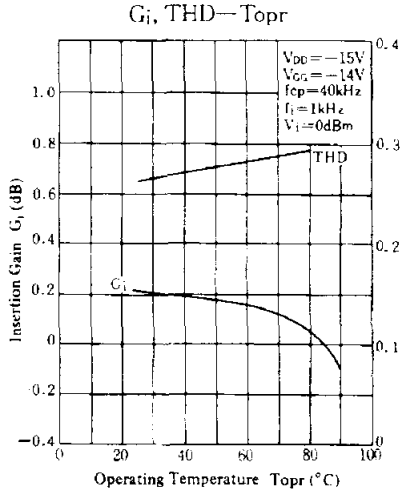
G_i—V_i



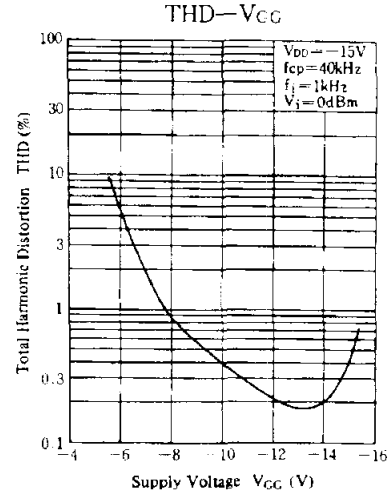
G_i, THD—R_L



G_i, THD—Topr

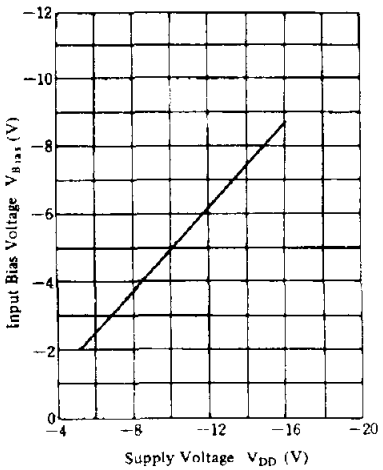


THD—V_{GG}

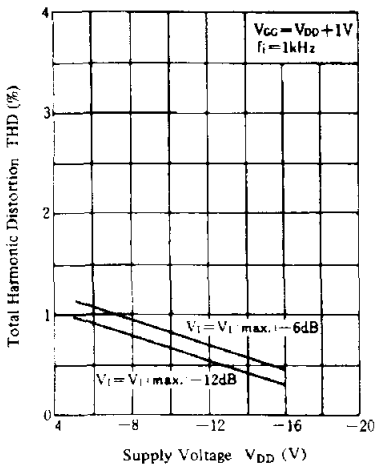


■ Supply Voltage Characteristics

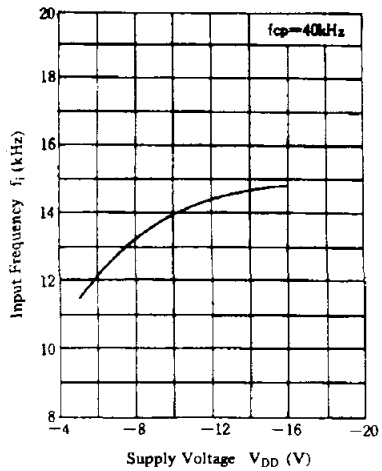
V_{Bias}—V_{DD}



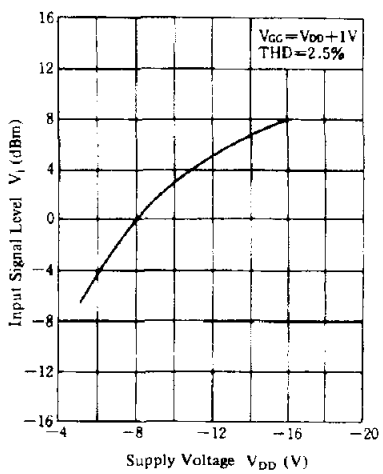
THD—V_{DD}



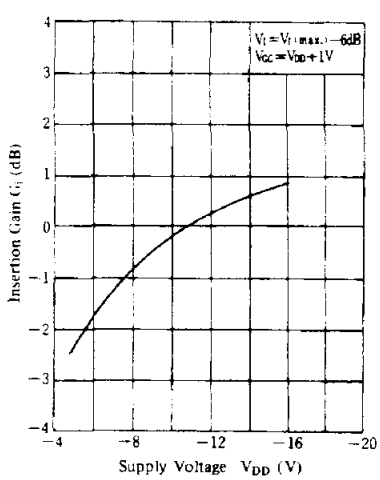
f_i—V_{DD}



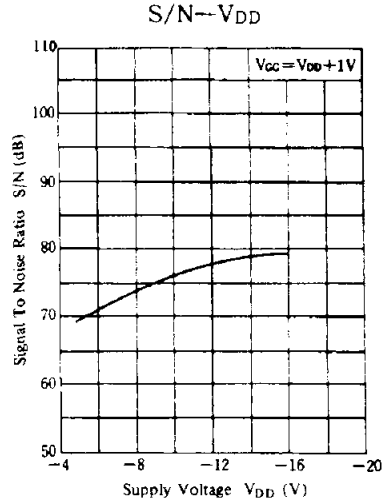
V_i—V_{DD}



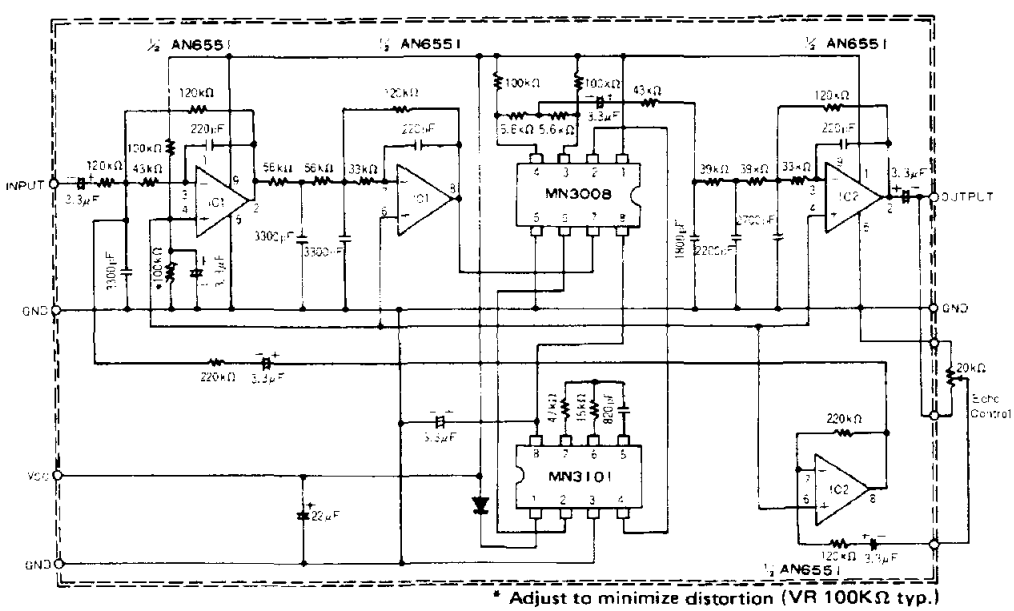
G_i—V_{DD}



S/N—V_{DD}



■ Application Circuit



* Adjust to minimize distortion (VR 100KΩ typ.)

Reverberation Effect Generation Circuit (Signal Delay Over 100msec.)

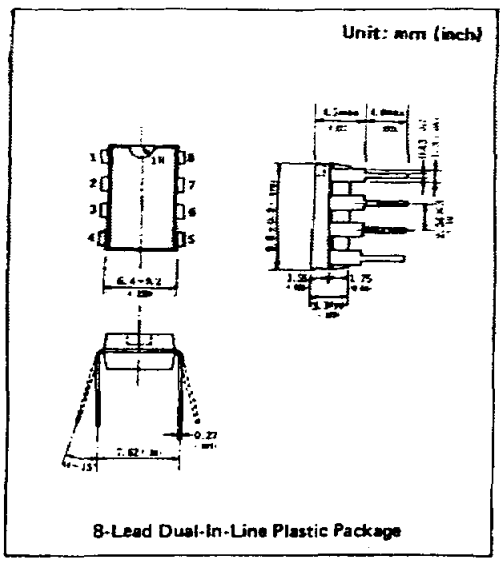
MN3101

CLOCK GENERATOR/DRIVER CMOS LSI FOR BBD

■ Description

The MN3101 is a CMOS LSI generating two phase clock signal of low output impedance to drive MN3000 series BBD. Built-in V_{GG} power supply circuit for the MN3000 series BBD* provides most suitable V_{GG} voltage for the BBD when the MN3101 is used with the same power source as BBD. Oscillation is abled by external resistors and capacitors, and also oscillation drive is possible by the separate excitation oscillation.
Clock signal frequency is 1/2 of oscillation frequency.

* MN3000 series BBDs
MN3001, MN3002, MN3003, MN3004, MN3005, MN3006 MN3007, MN3008, MN3009, MN3010, MN3011, MN3012.
Note) Clock signal generator is built-in the MN3003 and MN3012.



8-Lead Dual-In-Line Plastic Package

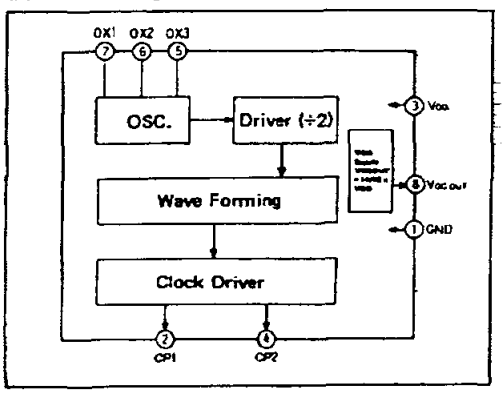
■ Features

- BBD direct driving capability of up to two MN3005s (equivalent to 8192-stages).
- Self and separate oscillations.
- Two phase clock output (Duty: 1/2).
- V_{GG} voltage generator is built-in for the BBD.
- Single power supply: −8 ~ −16V.
- 8-Lead Dual-In-Line Plastic Package.

■ Applications

- BBD clock generator/driver.

■ Block Diagram



■ Absolute Maximum Ratings (Ta = 25°C)

Item	Symbol	Rating	Unit	Remarks
Drain Supply Voltage	V_{DD}	−18~+0.3	V	GND=0V
Input Terminal Voltage	V_I	V_{DD}−0.3~+0.3	V	GND=0V
Output Terminal Voltage	V_O	V_{DD}−0.3~+0.3	V	GND=0V
Power Dissipation	P_D	200	mW	
Operating Ambient Temperature	Topr	−10~+70	℃	
Storage Temperature	Tstg	−30~+125	℃	

■ Operating Condition (Ta = 25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Drain Supply Voltage	V_{DD}	GND= 0 V	−8	−15	−16	V

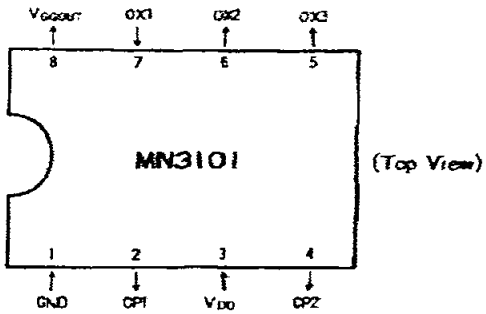
■ Electrical Characteristics (Ta = 25°C, V_{DD} = −15V, GND = 0V)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Input drain current	I_{DD}	No loard		3		mA
Total Power Dissipation	P_{tot}	Clock output 40kHz		45		mW
OX1 Input Terminal						
Voltage "H" Level	V_{IH}		0		−1	V
Voltage "L" Level	V_{IL}		V_{DD}+1		V_{DD}	V
Input Leakage Current	I_{LK}	V_I= 0 ~−15V			30	μA
OX2 Output Terminal						
Output Current "H" Level	I_{OH1}	V_O=− 1 V	0.6			mA
Output Current "L" Level	I_{OL1}	V_O=−14V	0.5			mA
Output Leakage Current	I_{LOL1}	V_O=V_{DD}			30	μA
Output Leakage Current	I_{LOH1}	V_O=GND			30	μA
OX3 Output Temrinal						
Output Current "H" Level	I_{OH2}	V_O=− 1 V	1.5			mA
Output Current "L" Level	I_{OL2}	V_O=−14V	2			mA
Output Leakage Current	I_{LOL2}	V_O=V_{DD}			30	μA
Output Leakage Current	I_{LOH2}	V_O=GND			30	μA
CP1, CP2 Output Terminal						
Output Current "H" Level	I_{OH3}	V_O=− 1 V	10			mA
Output Current "L" Level	I_{OL3}	V_O=−14V	10			mA
Output Leakage Current	I_{LOL3}	V_O=V_{DD}			30	μA
Output Leakage Current	I_{LOH3}	V_O=GND			30	μA
$V_{GG\ OUT}$ Output Terminal (*)						
Output Voltage	$V_{GG\ OUT}$			−14		V

(*) This terminal generates V_{GG} voltage exclusively applied for BBD manufactured by Matsushita Electronics Corporation, therefore, some times it might not be applicable for the device other than the V_{GG} voltage of MEC's BBD. $V_{GG\ OUT}$ changes by following formula depending on the value of V_{DD}.

$$V_{GG\ OUT} \fallingdotseq \frac{14}{15} V_{DD}$$

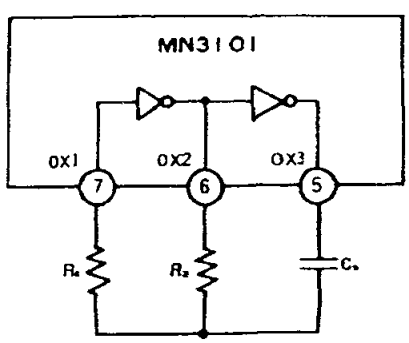
■ Terminal Assignments



■ Terminal Description

Terminal No.	Symbol	I/O	Terminal Name	Description	
1	GND	Power supply	Ground	Connected to GND of the circuit.	
2	CP1	0	Clock output 1	This terminal outputs clock signal that is a revers phase of CP2 with Duty 1/2, 1/2 frequency of oscillation frequency	
3	V_{DD}	Power supply	V_{DD} apply	−15V is applied.	
4	CP 2	0	Clock output 2	This terminal outputs clock signal that is a reverse phase of CP 1.	
5	OX 3	0	C and R is connected.	C, R are connected in case of selfoscillation. (Refer to oscillation circuit).	In case of separate excitation, OX3 and OX2 are opened and OX1 is set to OSC input.
6	OX 2	0			
7	OX 1	1			
8	$V_{GG\ OUT}$	0	V_{GG} voltage output.	−14V is output. (V_{DD} = −15V) $V_{GG\ OUT}$ = 14/15V_{DD}.	

■ Example of Oscillation Generation Circuit



Oscillation circuit of the MN3101 is composed of 2-stage inverter and oscillation frequency is defined by the time constant of C1 and R2 shown left.

Following is an example of C1, R1 and R2.
Figure 1 shows f_{cp}* −R2 characteristics.

Example \ Constant	R_1 (Ω)	R_2 (Ω)	C_1 (pF)	f_{esc}** (kHz)	f_{cp}* (kHz)
Example ①	0	5k~1M	33	15~1500	7.5~750
Example ②	22k	5k~1M	100	5.2~440	2.6~220
Example ③	22k	5k~1M	200	1.4~280	0.7~140

* Clock output frequency of CP1 or CP2 terminals.
** Oscillation frequency of OX1, OX2 and OX3.

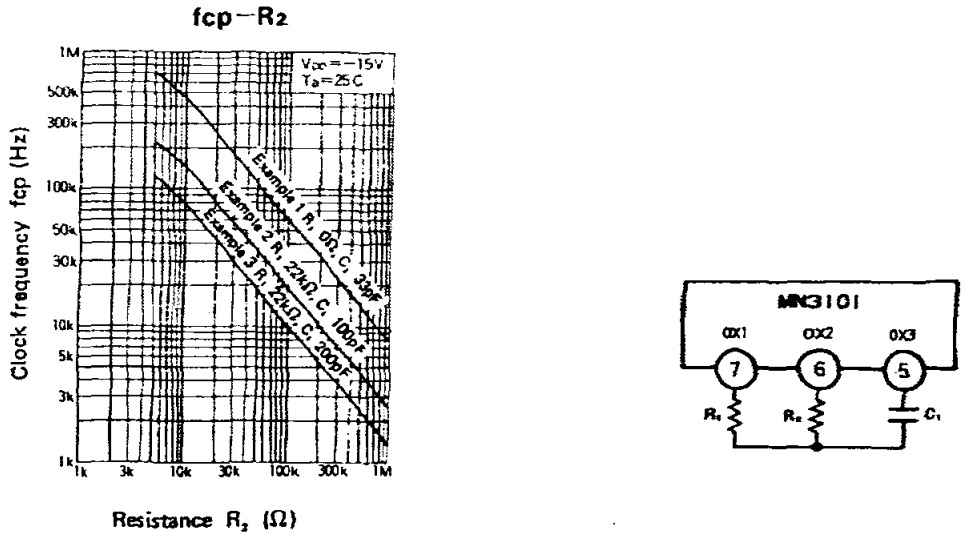


Figure 1 Example of characteristics of clock oscillation frequency.

■ The maximum clock frequency

The upper limit of the value of clock frequency is determined depending on the load capacitance and power consumption.
The permissible dissipation for this LSI is = P_D = 200mW.
If the clock frequency on the load capacitance is increased, the power consumption will be increased. (Refer to Figure 2.)
Accordingly, in order to utilize the MN3101 with dissipation less than the permissible value, it is necessary to select adequate values for the clock frequency and load capacitance.
Figure 3 shows an example of the dependence of the maximum clock frequency on the load capacitance in P_D = 150mW.
By connecting a resistance to the clock output terminal, it is made possible to increase the value of the maximum clock frequency without increasing dissipation. (Refer to Figures 2 and 3.)
It is because the dissipation on the LSI side is lessened, as a part of the power consumption required for driving the load capacitance is consumed by the series resistance.

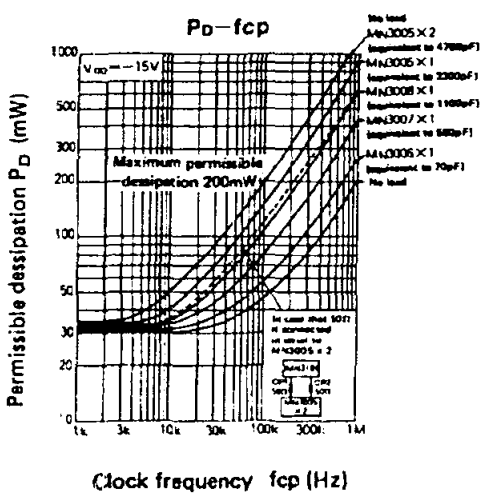


Figure 2 Example of the dependence of power consumption on the clock frequency.

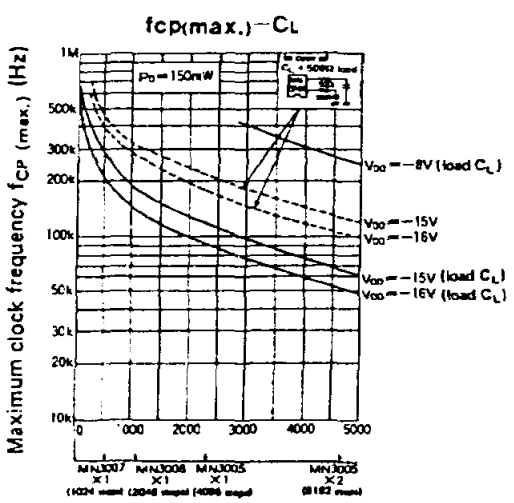


Figure 3 Example of the load capacitance characteristic of the maximum clock frequency in the power consumption of 150mW.

TL084
TL084A - TL084B

GENERAL PURPOSE J-FET QUAD OPERATIONAL AMPLIFIERS

- WIDE COMMON-MODE (UP TO V_{CC}^+) AND DIFFERENTIAL VOLTAGE RANGE
- LOW INPUT BIAS AND OFFSET CURRENT
- OUTPUT SHORT-CIRCUIT PROTECTION
- HIGH INPUT IMPEDANCE J–FET INPUT STAGE
- INTERNAL FREQUENCY COMPENSATION
- LATCH UP FREE OPERATION
- HIGH SLEW RATE : 16V/µs (typ)

N
DIP14
(Plastic Package)

D
SO14
(Plastic Micropackage)

P
TSSOP14
(Thin Shrink Small Outline Package)

ORDER CODE

Part Number	Temperature Range	Package		
		N	D	P
TL084M/AM/BM	-55°C, +125°C	•	•	•
TL084I/AI/BI	-40°C, +105°C	•	•	•
TL084C/AC/BC	0°C, +70°C	•	•	•
Example : TL084CN, TL084CD				

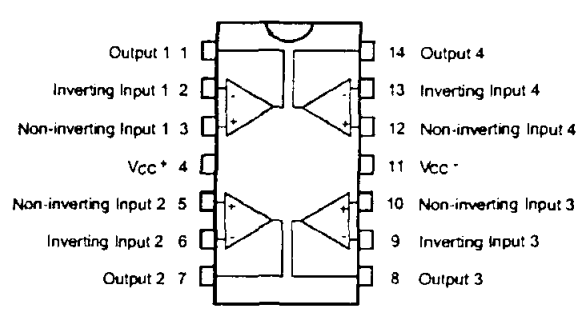
N = Dual in Line Package (DIP)
D = Small Outline Package (SO) - also available in Tape & Reel (DT)
P = Thin Shrink Small Outline Package (TSSOP) - only available in Tape & Reel (PT)

DESCRIPTION

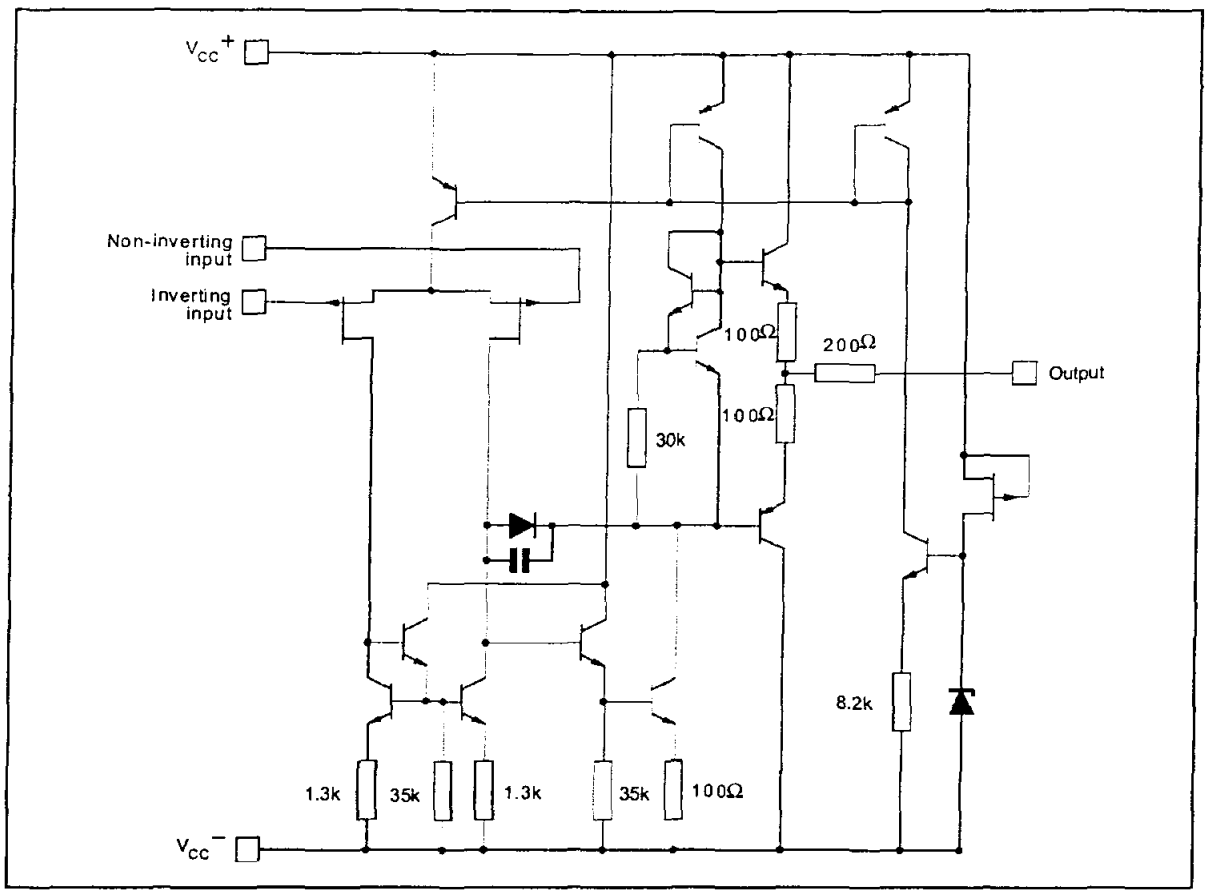
The TL084, TL084A and TL084B are high speed J–FET input quad operational amplifiers incorporating well matched, high voltage J–FET and bipolar transistors in a monolithic integrated circuit.

The devices feature high slew rates, low input bias and offset currents, and low offset voltage temperature coefficient.

PIN CONNECTIONS (top view)



SCHEMATIC DIAGRAM (each amplifier)



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	TL084M, AM, BM	TL084I, AI, BI	TL084C, AC, BC	Unit
V_{CC}	Supply voltage - note 1)	±18			V
V_i	Input Voltage - note 2)	±15			V
V_{id}	Differential Input Voltage - note 3)	±30			V
P_{tot}	Power Dissipation	680			mW
	Output Short-circuit Duration - note 4)	Infinite			
T_{oper}	Operating Free-air Temperature Range	-55 to +125	-40 to +105	0 to +70	°C
T_{stg}	Storage Temperature Range	-65 to +150			°C

1. All voltage values, except differential voltage, are with respect to the zero reference level (ground) of the supply voltages where the zero reference level is the midpoint between V_{CC}^+ and V_{CC}^-.
2. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or 15 volts, whichever is less.
3. Differential voltages are the non-inverting input terminal with respect to the inverting input terminal.
4. The output may be shorted to ground or to either supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded

ELECTRICAL CHARACTERISTICS

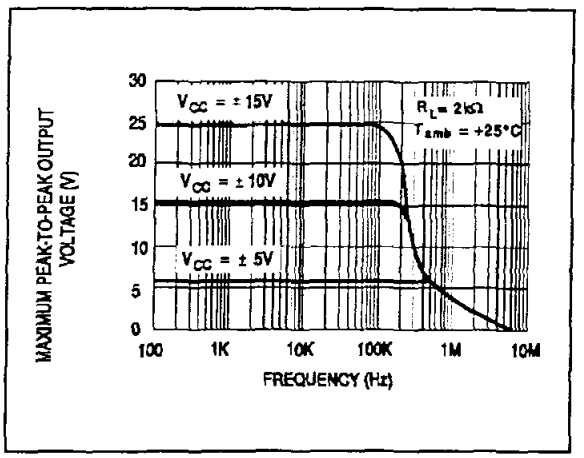
V_{CC} = ±15V, T_{amb} = +25°C (unless otherwise specified)

Symbol	Parameter		TL084I,M,AC,AI,AM, BC,BI,BM			TL084C			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage (R_s = 50Ω)								mV
	T_{amb} = +25°C	TL084		3	10		3	10	
		TL084A		3	6				
		TL084B		1	3				
	$T_{min} \le T_{amb} \le T_{max}$	TL084			13			13	
		TL084A			7				
		TL084B			5				
DV_{io}	Input Offset Voltage Drift			10			10		µV/°C
I_{io}	Input Offset Current - note [1]								
	T_{amb} = +25°C			5	100		5	100	pA
	$T_{min} \le T_{amb} \le T_{max}$				4			4	nA
I_{ib}	Input Bias Current -note 1								
	T_{amb} = +25°C			20	200		20	400	pA
	$T_{min} \le T_{amb} \le T_{max}$				20			20	nA
A_{vd}	Large Signal Voltage Gain (R_L = 2kΩ, V_o = ±10V)								V/mV
	T_{amb} = +25°C		50	200		25	200		
	$T_{min} \le T_{amb} \le T_{max}$		25			15			
SVR	Supply Voltage Rejection Ratio (R_S = 50Ω)								dB
	T_{amb} = +25°C		80	86		70	86		
	$T_{min} \le T_{amb} \le T_{max}$		80			70			
I_{CC}	Supply Current, no load, per amplifier								mA
	T_{amb} = +25°C			1.4	2.5		1.4	2.5	
	$T_{min} \le T_{amb} \le T_{max}$				2.5			2.5	
V_{icm}	Input Common Mode Voltage Range		±11	+15 -12		±11	+15 -12		V
CMR	Common Mode Rejection Ratio (R_S = 50Ω)								dB
	T_{amb} = +25°C		80	86		70	86		
	$T_{min} \le T_{amb} \le T_{max}$		80			70			
I_{os}	Output Short-circuit Current								mA
	T_{amb} = +25°C		10	40	60	10	40	60	
	$T_{min} \le T_{amb} \le T_{max}$		10		60	10		60	
$\pm V_{opp}$	Output Voltage Swing								V
	T_{amb} = +25°C	RL = 2kΩ	10	12		10	12		
		RL = 10kΩ	12	13.5		12	13.5		
	$T_{min} \le T_{amb} \le T_{max}$	RL = 2kΩ	10			10			
		RL = 10kΩ	12			12			
SR	Slew Rate (T_{amb} = +25°C)								V/µs
	V_{in} = 10V, R_L = 2kΩ, C_L = 100pF, unity gain		8	16		8	16		
t_r	Rise Time (T_{amb} = +25°C)								µs
	V_{in} = 20mV, R_L = 2kΩ, C_L = 100pF, unity gain			0.1			0.1		
K_{ov}	Overshoot (T_{amb} = +25°C)								%
	V_{in} = 20mV, R_L = 2kΩ, C_L = 100pF, unity gain			10			10		
GBP	Gain Bandwidth Product (T_{amb} = +25°C)								MHz
	V_{in} = 10mV, R_L = 2kΩ, C_L = 100pF, f= 100kHz		2.5	4		2.5	4		
R_i	Input Resistance			10^{12}			10^{12}		Ω

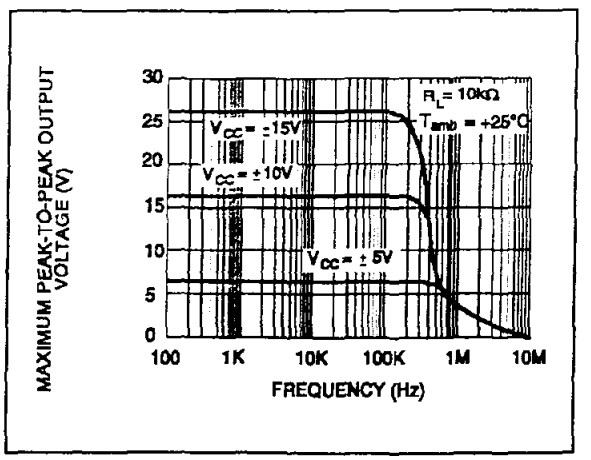
Symbol	Parameter	TL084I,M,AC,AI,AM, BC,BI,BM			TL084C			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
THD	Total Harmonic Distortion (T_{amb} = +25°C), f= 1kHz, R_L = 2kΩ,C_L = 100pF, A_v = 20dB, V_o = $2V_{pp}$		0.01			0.01		%
e_n	Equivalent Input Noise Voltage R_S = 100Ω, f = 1KHz		15			15		$\frac{nV}{\sqrt{Hz}}$
Øm	Phase Margin		45			45		degrees
V_{o1}/V_{o2}	Channel Separation A_v = 100		120			120		dB

1. The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature.

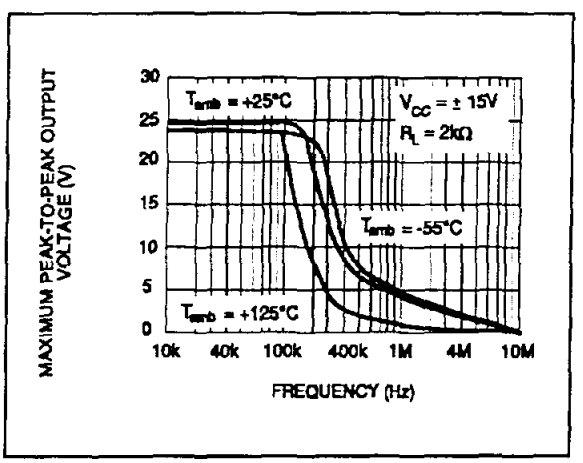
MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE versus FREQUENCY



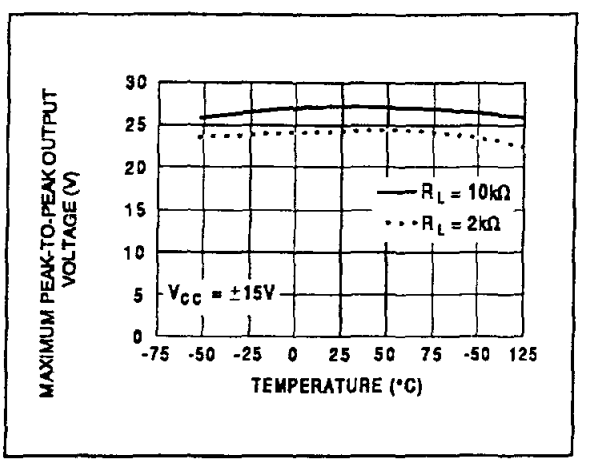
MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE versus FREQUENCY



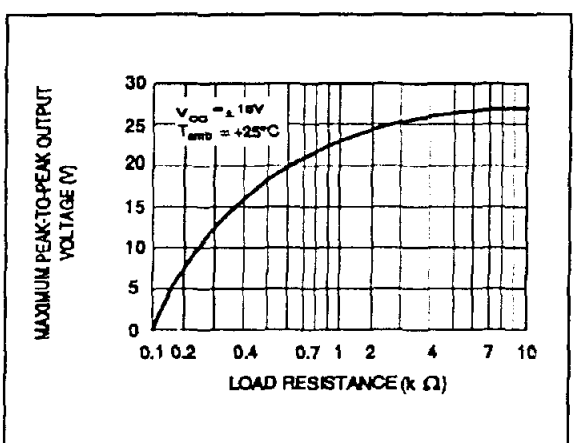
MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE versus FREQUENCY



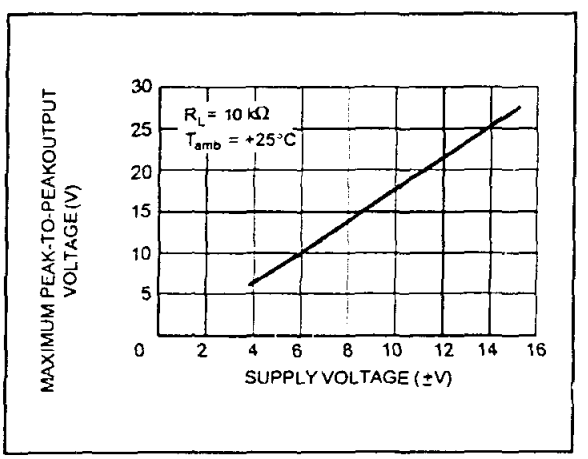
MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE versus FREE AIR TEMP.



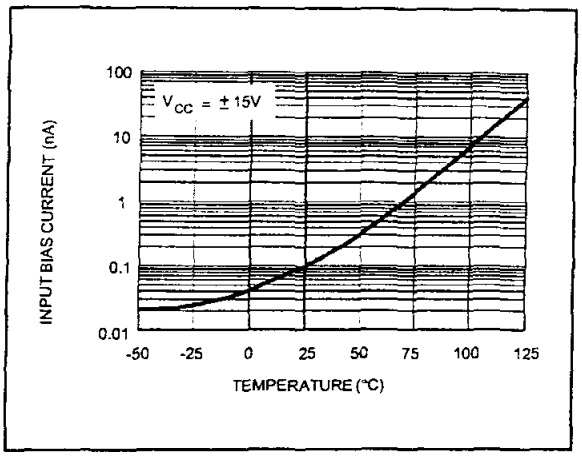
MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE versus LOAD RESISTANCE



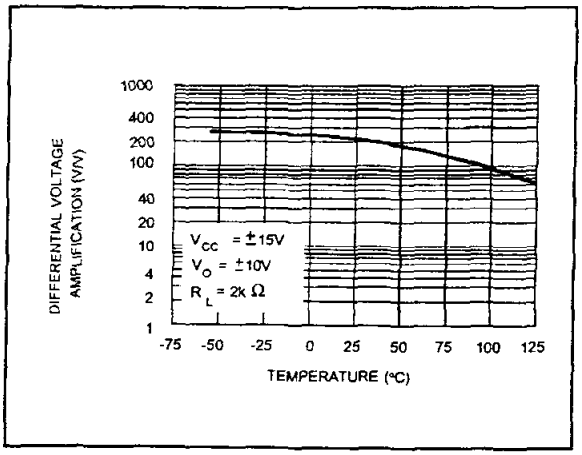
MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE versus SUPPLY VOLTAGE



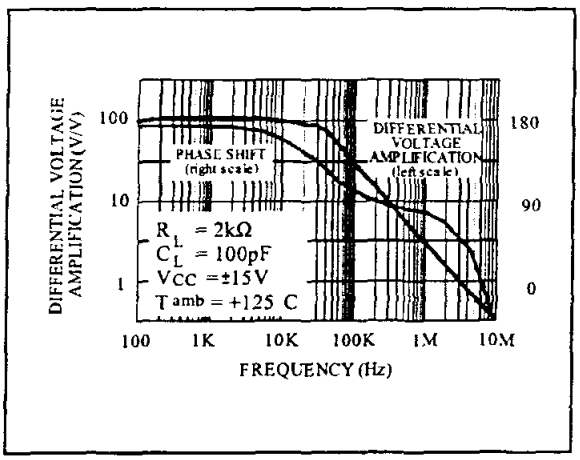
INPUT BIAS CURRENT versus FREE AIR TEMPERATURE



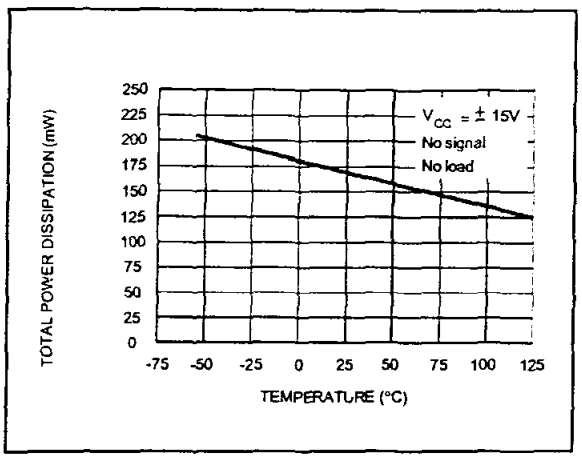
LARGE SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION versus FREE AIR TEMP.



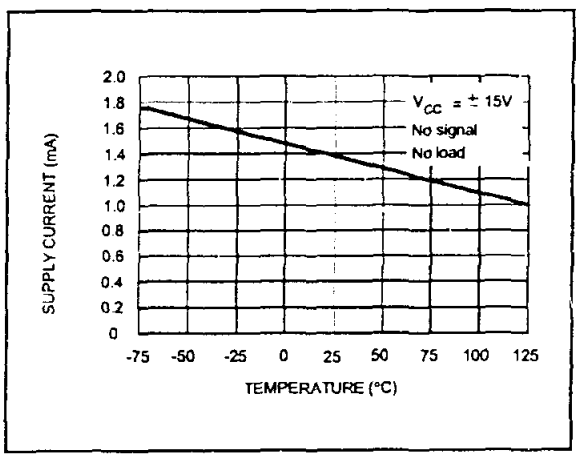
LARGE SIGNAL DIFFERENTIAL VOLTAGE AMPLIFICATION AND PHASE SHIFT versus FREQUENCY



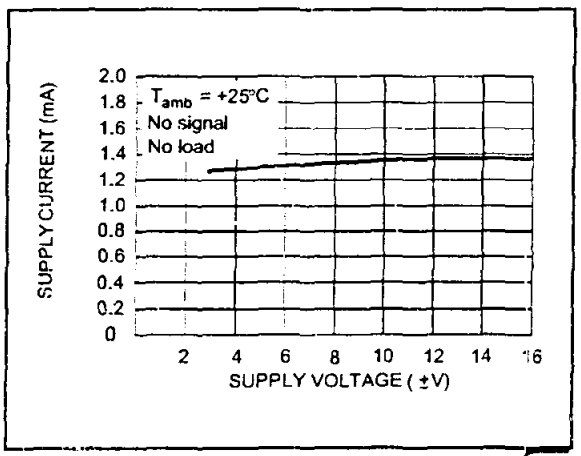
TOTAL POWER DISSIPATION versus FREE AIR TEMPERATURE



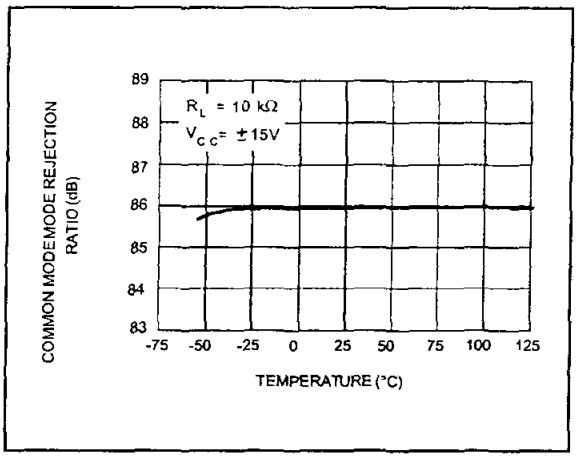
SUPPLY CURRENT PER AMPLIFIER versus FREE AIR TEMPERATURE



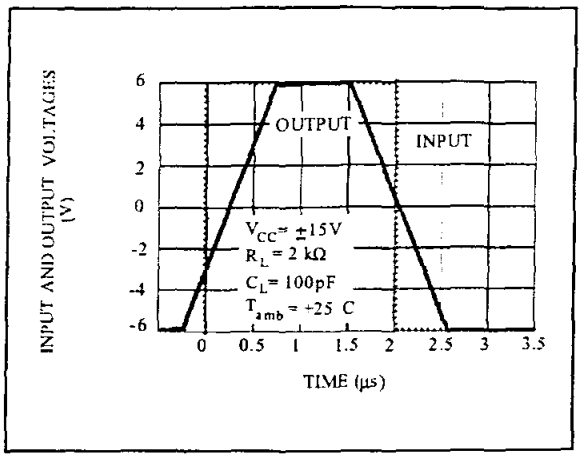
SUPPLY CURRENT PER AMPLIFIER versus SUPPLY VOLTAGE



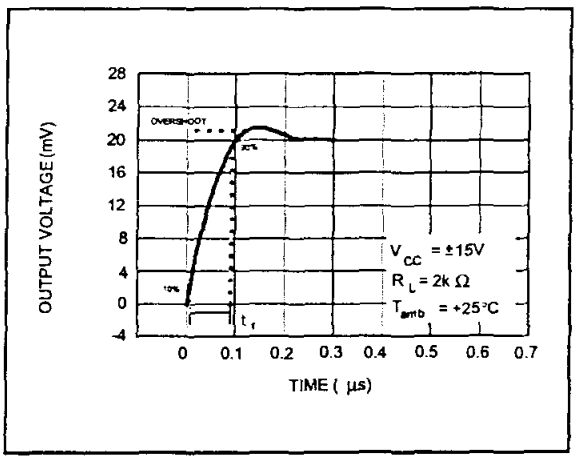
COMMON MODE REJECTION RATIO versus FREE AIR TEMPERATURE



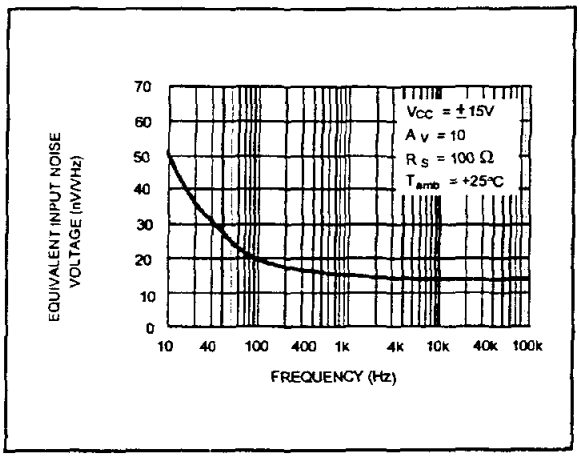
VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE



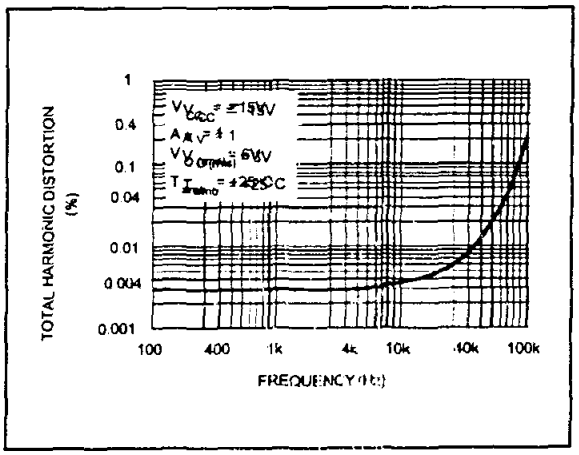
OUTPUT VOLTAGE versus ELAPSED TIME



EQUIVALENT INPUT NOISE VOLTAGE versus FREQUENCY



TOTAL HARMONIC DISTORTION versus FREQUENCY



PARAMETER MEASUREMENT INFORMATION

Figure 1 : Voltage Follower

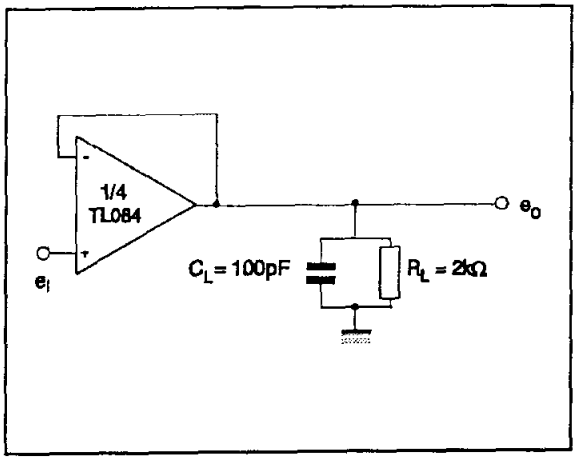
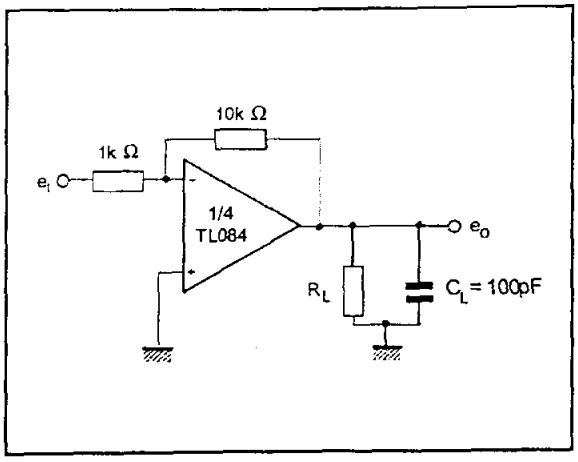
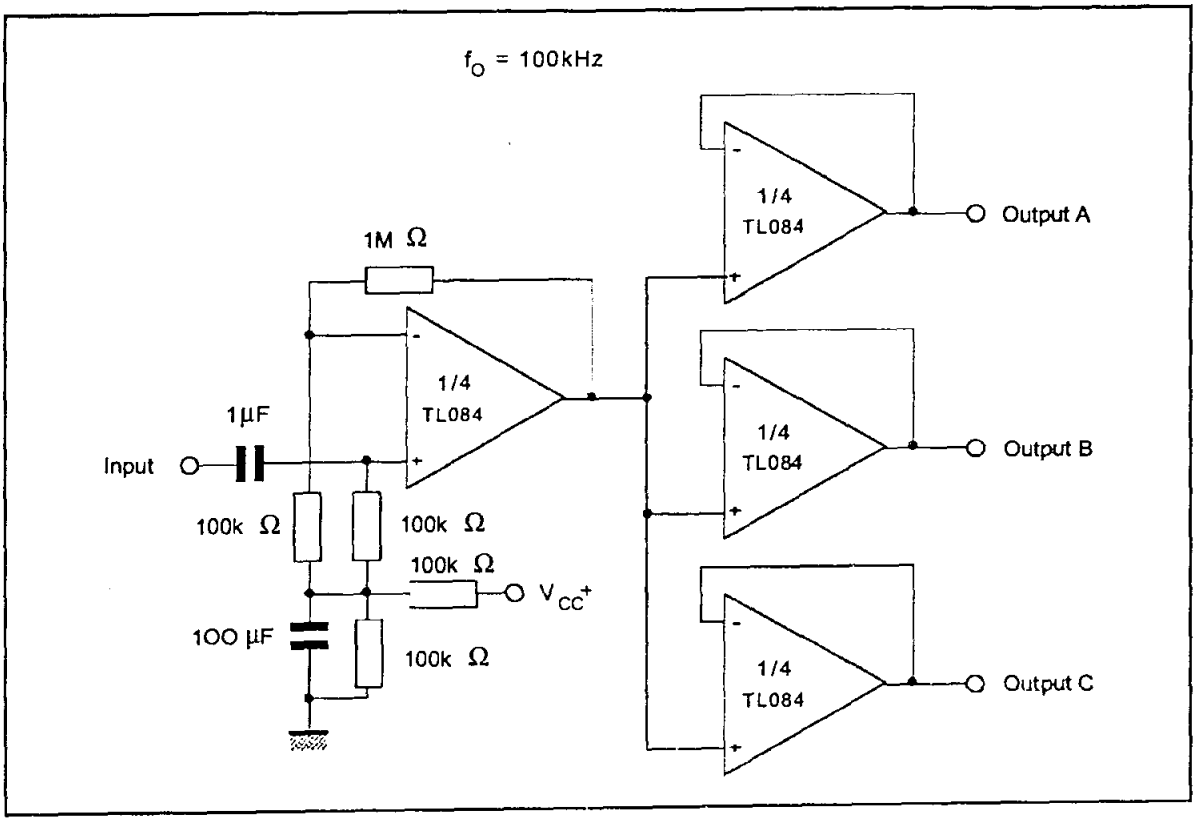


Figure 2 : Gain-of-10 Inverting Amplifier



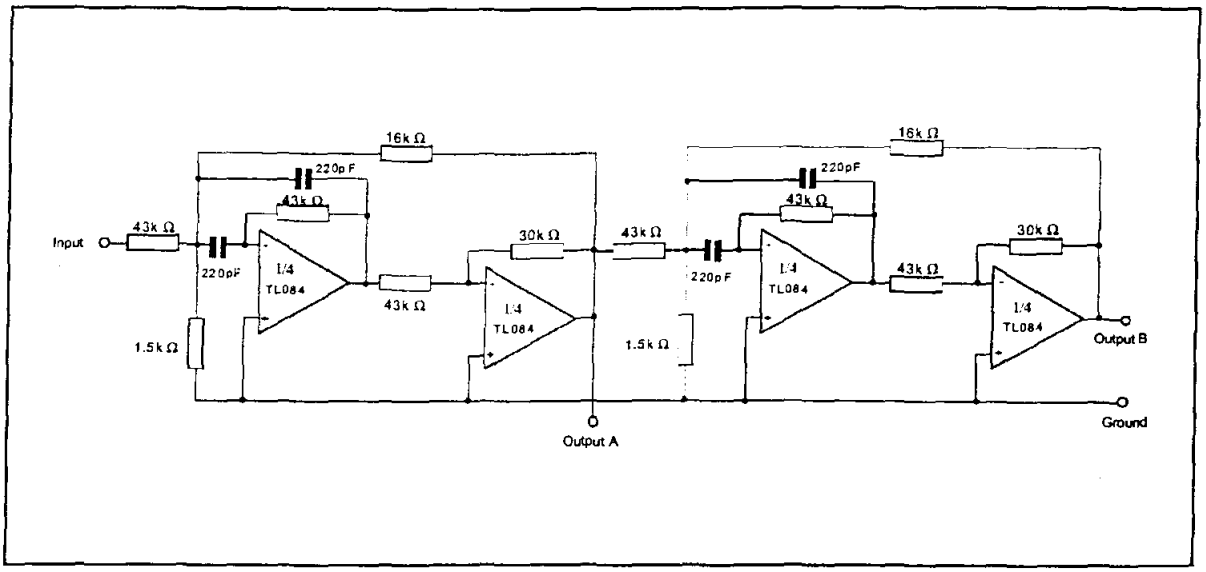
TYPICAL APPLICATIONS

AUDIO DISTRIBUTION AMPLIFIER

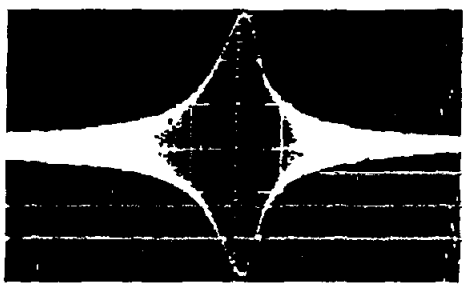


TYPICAL APPLICATIONS (continued)

POSITIVE FEEDBACK BANDPASS FILTER

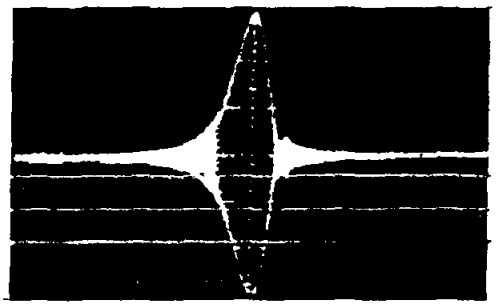


OUTPUT A



SECOND ORDER BANDPASS FILTER
fo = 100kHz; Q = 30; Gain = 4

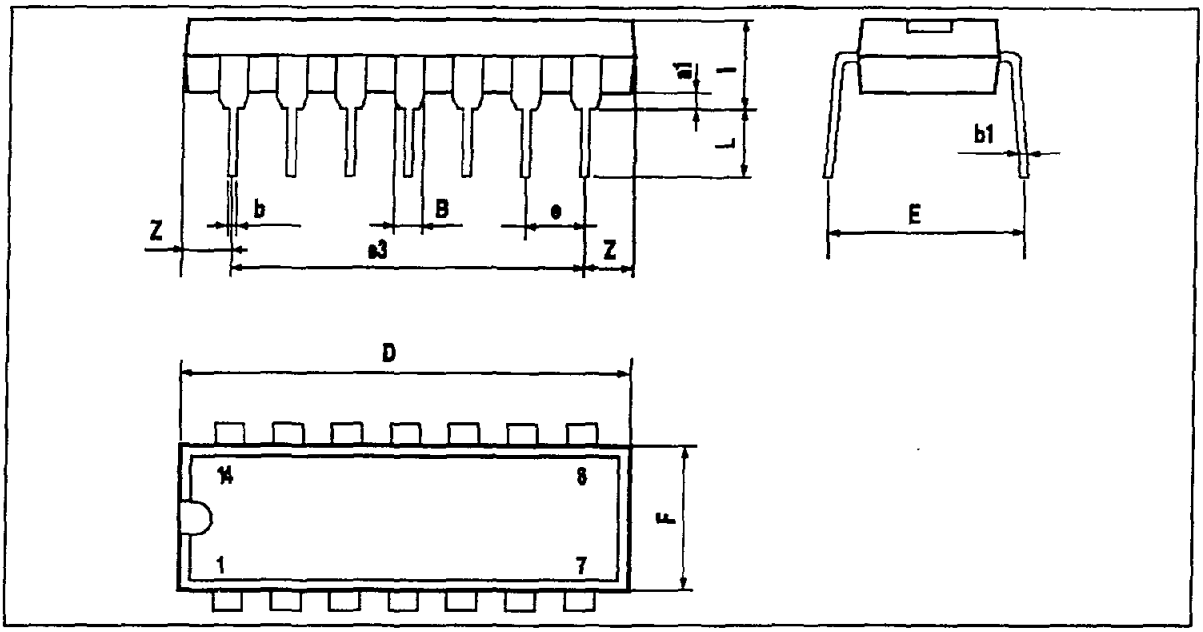
OUTPUT B



CASCADED BANDPASS FILTER
fo = 100kHz; Q = 69; Gain = 16

PACKAGE MECHANICAL DATA

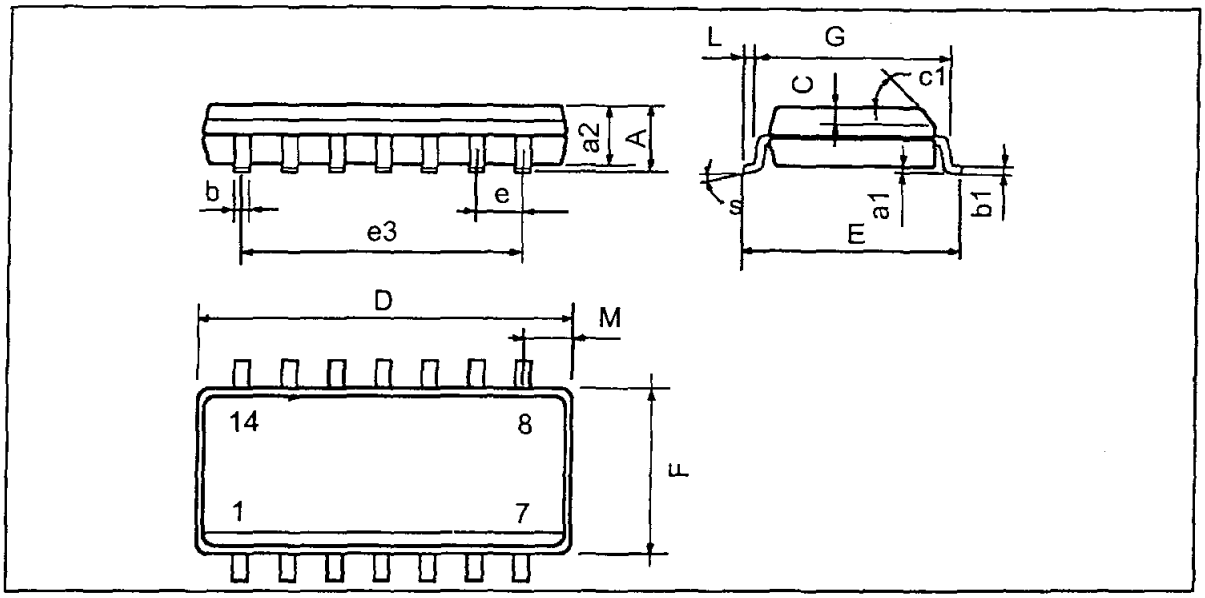
14 PINS - PLASTIC DIP



Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
a1	0.51			0.020		
B	1.39		1.65	0.055		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		15.24			0.600	
F			7.1			0.280
i			5.1			0.201
L		3.3			0.130	
Z	1.27		2.54	0.050		0.100

PACKAGE MECHANICAL DATA

14 PINS - PLASTIC MICROPACKAGE (SO)

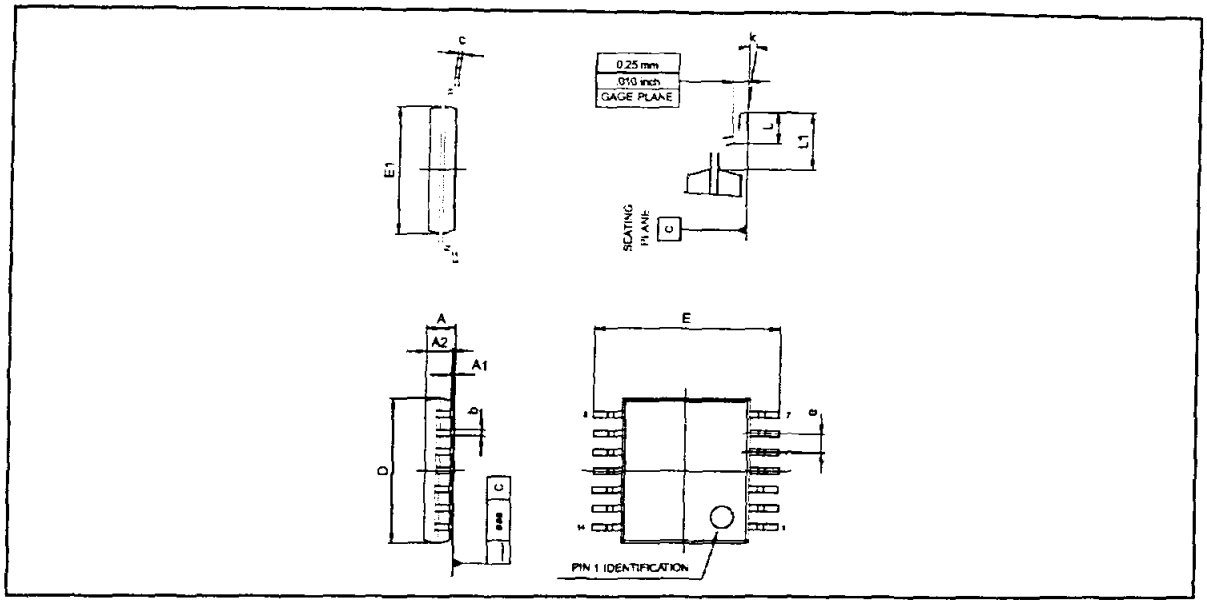


Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
a1	0.1		0.2	0.004		0.008
a2			1.6			0.063
b	0.35		0.46	0.014		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.020	
c1	45° (typ.)					
D (1)	8.55		8.75	0.336		0.344
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		7.62			0.300	
F (1)	3.8		4.0	0.150		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.020		0.050
M			0.68			0.027
S	8° (max.)					

Note : (1) D and F do not include mold flash or protrusions - Mold flash or protrusions shall not exceed 0.15mm (.066 inc) ONLY FOR DATA BOOK.

PACKAGE MECHANICAL DATA

14 PINS - THIN SHRINK SMALL OUTLINE PACKAGE



Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.20			0.05
A1	0.05		0.15	0.01		0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.15
c	0.09		0.20	0.003		0.012
D	4.90	5.00	5.10	0.192	0.196	0.20
E		6.40			0.252	
E1	4.30	4.40	4.50	0.169	0.173	0.177
e		0.65			0.025	
k	0°		8°	0°		8°
l	0.50	0.60	0.75	0.09	0.0236	0.030