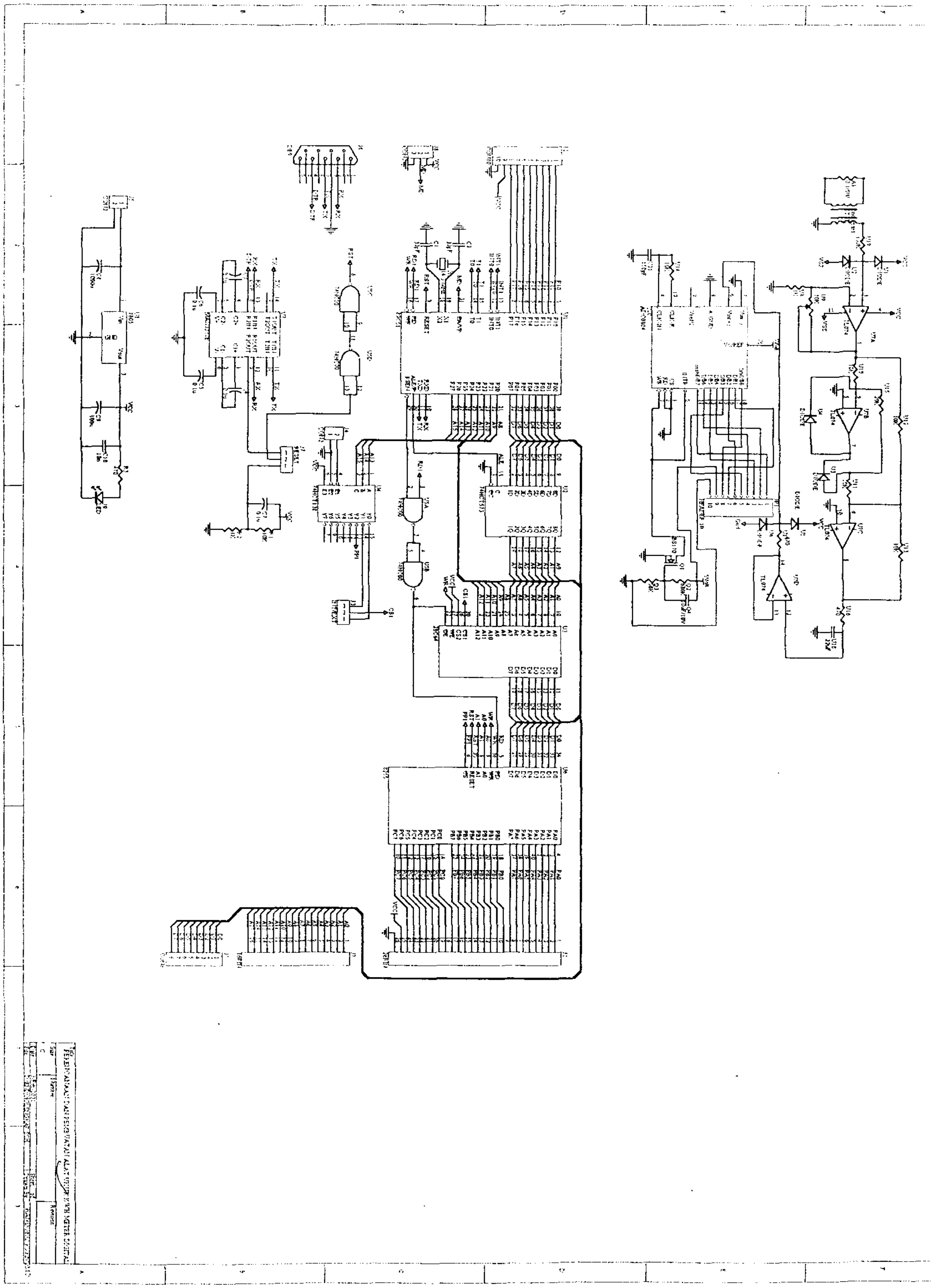
LAMPIRAN 1



```
;-------------------------------------------------------------------------------
                 PERENCANAAN DAN PEMBUATAN ALAT UKUR
                         KWH METER DIGITAL
                      UNIKA WIDYA MANDALA
                            SURABAYA
;-------------------------------------------------------------------------------
PA        EQU   4000H
PB        EQU   4001H
PC        EQU   4002H
PCW       EQU   4003H
CW        EQU   80H

COUNT       EQU   08H
TEMP1       EQU   09H
TEMP2       EQU   0AH
TEMP3       EQU   0BH
TEMP4       EQU   0CH
IN1       EQU   0DH
IN2       EQU   0EH
IN3       EQU   0FH
IN4       EQU   10H
VAR6      EQU   11H          ;VARIABEL 64 BIT
VAR7      EQU   12H
VAR8      EQU   13H
VAR9      EQU   14H
VAR10     EQU   15H
VAR11     EQU   16H
VAR12     EQU   17H          ;MSB 64 BIT
VAR1      EQU   18H          ;LSB 32 BIT
VAR2      EQU   19H
VAR3      EQU   1AH
VAR4      EQU   1BH          ;MSB 32 BIT
VAR5      DATA  21H          ;LSB 64 BIT
WATT1     EQU   1CH
WATT2     EQU   1DH
WATT3     EQU   1EH
WATT4     EQU   1FH
KWH1      EQU   30H
KWH2      EQU   31H
KWH3      EQU   32H
KWH4      EQU   33H
UANG1     EQU   34H
UANG2     EQU   35H
UANG3     EQU   36H
UANG4     EQU   37H
WAKTU1    EQU   38H
```

```
WAKTU2    EQU   39H
CURSOR    EQU   3AH

ORG       2000H

START               AJMP   MULAI

                    ORG    200BH
;--------------------------------
;      INTERUPT TIMER0
;--------------------------------
                    AJMP   TIMER0

                    ORG    2100H
;--------------------------------
;      ROUTINE TIMER0
;--------------------------------
TIMER0              DJNZ   R4,ESCTR0
                    MOV    R4,#48
                    DJNZ   R5,ESCTR0
                    MOV    R5,#100
                    INC    WAKTU1
ESCTR0              RETI

;--------------------------------
;         DELAY
;--------------------------------
DELAY               MOV    R7,#0FFH
DEL1                MOV    R6,#0FFH
                    DJNZ   R6,$
                    DJNZ   R7,DEL1
                    RET

;--------------------------------
;        DELAY LCD
;--------------------------------
DEL_LCD             MOV    R7,#1
DEL2                MOV    R6,#250
                    DJNZ   R6,$
                    DJNZ   R7,DEL2
                    RET

;--------------------------------
;        INISIALISASI
;--------------------------------
INIT                MOV    WATT1,#0
```

```
                MOV   WATT2,#0
                MOV   WATT3,#0
                MOV   WATT4,#0
                MOV   KWH1,#0
                MOV   KWH2,#0
                MOV   KWH3,#0
                MOV   KWH4,#0
                MOV   UANG1,#0
                MOV   UANG2,#0
                MOV   UANG3,#0
                MOV   UANG4,#0
                MOV   R4,#48
                MOV   R5,#40
                MOV   IE,#82H          ;INTERUPT TIMER0
ENABLE
                MOV   TMOD,#02H          ;TIMER0 MODE 2
                MOV   TL0,#64
                MOV   TH0,#64
                MOV   WAKTU2,#0
                MOV   WAKTU1,#0

                MOV   TMOD,#00100010B       ;T1 mode2, T0
mode2
                MOV   TL1,#0FAH             ;T1 mode2 generate
BR=9600 Bps
                MOV   TH1,#0FAH
                MOV   TCON,#01000000B       ;T1 on,T0 off
                MOV   SCON,#01010000B      ;Mode1,REN
                MOV   PCON,#80H            ;SMOD=0

                SETB  TR0
                RET

;--------------------------------
;       SUBROUTINE LCD
;--------------------------------
SUB_LCD         MOV   DPTR,#PA
                MOVX  @DPTR,A
                MOV   A,#02H       ;ENABLE HIGH
                MOV   DPTR,#PC
                MOVX  @DPTR,A
                ACALL DEL_LCD
                MOV   A,#0         ;ENABLE LOW
                MOVX  @DPTR,A
                RET
```

```
;---------------------------------
;          LCD
;---------------------------------
LCD             MOV    A,#3FH       ;RESETLCD
                ACALL  SUB_LCD
                MOV    A,#0CH       ;DISPLAY ON/OFF
                ACALL  SUB_LCD
                MOV    A,#06H       ;DATA ENTRY
                ACALL  SUB_LCD
                MOV    A,#01H       ;DISPLAY CLEAR
                ACALL  SUB_LCD
                MOV    A,#80H       ;DISPLAY LINE1 (LINE2=C0);
                ACALL  SUB_LCD
                RET

;---------------------------------
;          PEMBAGIAN
;---------------------------------
BAGI            MOV    A,R0
                PUSH   A
                MOV    A,R1
                PUSH   A
                MOV    A,R2
                PUSH   A
                MOV    IN1,VAR1
                MOV    IN2,VAR2
                MOV    IN3,VAR3
                MOV    IN4,VAR4
                MOV    VAR1,#0
                MOV    VAR2,#0
                MOV    VAR3,#0
                MOV    VAR4,#0
                MOV    COUNT,#64
BAGI1           CLR    C
                MOV    A,VAR5           ;GESER LSB 64 BIT
                RLC    A
                MOV    VAR5,A
                MOV    R0,#11H          ;ALAMAT VAR6
                MOV    R2,#11
SHIFT           MOV    A,@R0            ;GESER KIRI
                RLC    A
                MOV    @R0,A
                INC    R0
                DJNZ   R2,SHIFT
                MOV    TEMP1,VAR1
                MOV    TEMP2,VAR2
```

```
                MOV   TEMP3,VAR3
                MOV   TEMP4,VAR4
                CLR   C              ;PENGURANGAN
                MOV   R0,#18H
                MOV   R1,#0DH
                MOV   R2,#4
KURANG          MOV   A,@R0
                SUBB  A,@R1
                MOV   @R0,A
                INC   R0
                INC   R1
                DJNZ  R2,KURANG
                JC    CLEAR_VARBIT0        ;CEK APAKAH RESULT
NEGATIVE
                SETB  VAR5.0
                AJMP  CEKCOUNTER
CLEAR_VARBIT0   MOV   VAR1,TEMP1
                MOV   VAR2,TEMP2
                MOV   VAR3,TEMP3
                MOV   VAR4,TEMP4
CEKCOUNTER      DJNZ  COUNT,BAGI1
                POP   A
                MOV   R2,A
                POP   A
                MOV   R1,A
                POP   A
                MOV   R0,A
                RET

;------------------------------
;       PERKALIAN
;------------------------------
KALI        MOV   IN1,VAR1
            MOV   IN2,VAR2
            MOV   IN3,VAR3
            MOV   IN4,VAR4
            MOV   VAR9,#0
            MOV   VAR10,#0
            MOV   VAR11,#0
            MOV   VAR12,#0
            MOV   VAR1,#0
            MOV   VAR2,#0
            MOV   VAR3,#0
            MOV   VAR4,#0
            MOV   COUNT,#32
KALI1       CLR   C
```

```
            JNB    VAR5.0,PASS2         ;APAKAH Q0 = 0 ?
            MOV    R0,#18H
            MOV    R1,#0DH
            MOV    R2,#4
TAMBAH      MOV    A,@R0
            ADDC   A,@R1
            MOV    @R0,A
            INC    R0
            INC    R1
            DJNZ   R2,TAMBAH
PASS2       MOV    R0,#1BH              ;ALAMAT VAR6
            MOV    R2,#4
SHIFTR1     MOV    A,@R0                ;GESER KANAN
            RRC    A
            MOV    @R0,A
            DEC    R0
            DJNZ   R2,SHIFTR1
            MOV    R0,#13H
            MOV    R2,#3
SHIFTR2     MOV    A,@R0
            RRC    A
            MOV    @R0,A
            DEC    R0
            DJNZ   R2,SHIFTR2
            MOV    A,VAR5               ;GESER LSB 64 BIT
            RRC    A
            MOV    VAR5,A
            DJNZ   COUNT,KALI1          ;APAKAH COUNTER = 0 ?
            MOV    VAR12,VAR4
            MOV    VAR11,VAR3
            MOV    VAR10,VAR2
            MOV    VAR9,VAR1
            RET

;----------------------------------------
;          PENJUMLAHAN
;----------------------------------------
SUM         CLR    C                    ;PENJUMLAHAN
            MOV    A,VAR5
            ADDC   A,VAR1
            MOV    VAR5,A
            MOV    R0,#11H
            MOV    R1,#19H
            MOV    R2,#3
JUMLAH      MOV    A,@R0
            ADDC   A,@R1
```

```
            MOV    @R0,A
            INC    R0
            INC    R1
            DJNZ   R2,JUMLAH
            JNC    ESC_SUM
            INC    VAR9
ESC_SUM     RET

;--------------------------------------
;           PENGURANGAN
;--------------------------------------
SUB         CLR    C              ;PENGURANGAN
            MOV    A,VAR5
            SUBB   A,VAR1
            MOV    VAR5,A
            MOV    R0,#11H
            MOV    R1,#19H
            MOV    R2,#3
POTONG      MOV    A,@R0
            SUBB   A,@R1
            MOV    @R0,A
            INC    R0
            INC    R1
            DJNZ   R2,POTONG
            JNC    ESC_SUB
            DEC    VAR9
ESC_SUB     RET

;--------------------------------------
;           ENABLE DISPLAY
;--------------------------------------
ENA_DIS     MOV    DPTR,#PA
            MOVX   @DPTR,A
            MOV    A,#03H
            MOV    DPTR,#PC
            MOVX   @DPTR,A
            ACALL  DEL_LCD
            MOV    A,#0
            MOV    DPTR,#PC
            MOVX   @DPTR,A
            RET
```

```
;----------------------------------
;        DISPLAY KWH
;----------------------------------
DISP_KWH   MOV    R3,#9          ;9 CHAR
           MOV    CURSOR,#15
DISP1      MOV    R2,CURSOR      ;POINTER CURSOR
           DEC    CURSOR
           MOV    A,#80H         ;POINTER MULA-MULA BARIS1
           ACALL  SUB_LCD
           ACALL  SUB_LCD
DISP2      MOV    A,#14H         ;CURSOR BERGESER
           ACALL  SUB_LCD
           DJNZ   R2,DISP2
           CJNE   R3,#6,DISP3
           MOV    A,#2EH
           AJMP   DISP4
DISP3      MOV    VAR1,#10
           MOV    VAR2,#0
           MOV    VAR3,#0
           MOV    VAR4,#0
           ACALL  BAGI
           MOV    A,#30H
           ORL    A,VAR1         ;TAMPILKAN SISA DIV 10
DISP4      ACALL  ENA_DIS
           DJNZ   R3,DISP1
           RET

;----------------------------------
;        DISPLAY BIAYA
;----------------------------------
DISP_BIAYA MOV    R3,#9          ;9 KARAKTER
           MOV    CURSOR,#15
DISP5      MOV    R2,CURSOR      ;POINTER CURSOR
           DEC    CURSOR
           MOV    A,#0C0H        ;POINTER MULA-MULA BARIS 2
           ACALL  SUB_LCD
           ACALL  SUB_LCD
DISP6      MOV    A,#14H         ;CURSOR BERGESER
           ACALL  SUB_LCD
           DJNZ   R2,DISP6
           CJNE   R3,#7,DISP7
           MOV    A,#2EH
           AJMP   DISP8
DISP7      MOV    VAR1,#10
           MOV    VAR2,#0
           MOV    VAR3,#0
```

```
                MOV    VAR4,#0
                ACALL  BAGI
                MOV    A,#30H
                ORL    A,VAR1              ;TAMPILKAN SISA DIV 10
DISP8           ACALL  ENA_DIS
                DJNZ   R3,DISP5
                RET

;--------------------------------
;      SUBROUTINE STRING
;--------------------------------
SUB_STR                 MOV    A,#03       ;R/S OFF
                MOV    DPTR,#PC
                MOVX   @DPTR,A
                MOV    A,@R0
                MOV    DPTR,#PA
                MOVX   @DPTR,A
                ACALL  DEL_LCD
                MOV    A,#0H        ;R/S ON
                MOV    DPTR,#PC
                MOVX   @DPTR,A
                ACALL  DEL_LCD
                INC    R0
                DJNZ   R2,SUB_STR
                RET

;--------------------------------
; TULISAN 'KWH  : ' & 'BIAYA : '
;--------------------------------
STRING          MOV    A,#0         ;CONTROL LCD = 0
                MOV    DPTR,#PC
                MOVX   @DPTR,A
                ACALL  DEL_LCD
                MOV    VAR6,#4BH     ;{K}
                MOV    VAR7,#57H     ;{W}
                MOV    VAR8,#48H     ;{H}
                MOV    VAR9,#20H     ;{ }
                MOV    VAR10,#20H    ;{ }
                MOV    VAR11,#3AH    ;{:}
                MOV    R0,#11H
                MOV    R2,#6
                ACALL  SUB_STR
                MOV    A,#0C0H       ;DISPLAY BARIS 2
                ACALL  SUB_LCD
                MOV    VAR6,#43H     ;{C}
                MOV    VAR7,#4FH     ;{O}
```

```
            MOV   VAR8,#53H     ;{S}
            MOV   VAR9,#54H     ;{T}
            MOV   VAR10,#20H    ;{ }
            MOV   VAR11,#3AH    ;{:}
            MOV   R0,#11H
            MOV   R2,#6
            ACALL SUB_STR
            RET

;--------------------------------
;     AKTIFKAN ALU 4 BYTE
;--------------------------------
ALU4BYTE    MOV   VAR9,#0
            MOV   VAR10,#0
            MOV   VAR11,#0
            MOV   VAR12,#0
            RET

;--------------------------------
;    PERHITUNGAN KWH METER
;--------------------------------
HITWATT     MOV   VAR5,P1
            MOV   VAR6,#0
            MOV   VAR7,#0
            MOV   VAR8,#0
            ACALL ALU4BYTE
            MOV   VAR1,#51
            MOV   VAR2,#0
            MOV   VAR3,#0
            MOV   VAR4,#0
            ACALL KALI
            MOV   VAR1,WATT1
            MOV   VAR2,WATT2
            MOV   VAR3,WATT3
            MOV   VAR4,WATT4
            ACALL SUM
            MOV   WATT1,VAR5
            MOV   WATT2,VAR6
            MOV   WATT3,VAR7
            MOV   WATT4,VAR8
ESCHIT      RET
```

```
;--------------------------------
; PERHITUNGAN KWH METER & UANG
;--------------------------------
HITKWH     MOV    VAR5,WATT1
           MOV    VAR6,WATT2
           MOV    VAR7,WATT3
           MOV    VAR8,WATT4
           MOV    VAR1,#36
           MOV    VAR2,#0
           MOV    VAR3,#0
           MOV    VAR4,#0
           ACALL  ALU4BYTE
           ACALL  BAGI            ;DIBAGI 36
           MOV    VAR1,#232
           MOV    VAR2,#3
           MOV    VAR3,#0
           MOV    VAR4,#0
           ACALL  ALU4BYTE
           ACALL  BAGI            ;DIBAGI 1000
           MOV    WATT1,VAR1
           MOV    WATT2,VAR2
           MOV    WATT3,VAR3
           MOV    WATT4,VAR4
           MOV    VAR1,KWH1
           MOV    VAR2,KWH2
           MOV    VAR3,KWH3
           MOV    VAR4,KWH4
           ACALL  SUM
           MOV    KWH1,VAR5
           MOV    KWH2,VAR6
           MOV    KWH3,VAR7
           MOV    KWH4,VAR8
           MOV    VAR1,#9
           MOV    VAR2,#0
           MOV    VAR3,#0
           MOV    VAR4,#0
           ACALL  KALI
           MOV    UANG1,VAR5
           MOV    UANG2,VAR6
           MOV    UANG3,VAR7
           MOV    UANG4,VAR8
           RET
```

```
;---------------------------------
;        TRANSMISI
;---------------------------------
TRANSMISI  MOV  R0,#30H
           MOV  R2,#8
           MOV  A,#128
           JNB  TI,$
           CLR  TI
TRANS1     MOV  A,@R0
           JNB  TI,$
           CLR  TI
           DJNZ R2,TRANS1
           RET

;---------------------------------
;        MAIN PROGRAM
;---------------------------------
MULAI      MOV    SP,#40H
           ACALL  DELAY
           MOV    DPTR,#PCW
           MOV    A,#CW
           MOVX   @DPTR,A
           ACALL  LCD
           ACALL  STRING
           ACALL  INIT
CEKDETIK   MOV    A,WAKTU1
           CJNE   A,WAKTU2,CEK          ;CEK PERUBAHAN DETIK
           AJMP   DISPLAY
CEK        ACALL  HITWATT
           MOV    WAKTU2,WAKTU1
           MOV    A,WAKTU1
           MOV    B,#36
           DIV    AB
           MOV    WAKTU1,B
           MOV    WAKTU2,WAKTU1
           JNB    ACC.0,DISPLAY         ;APAKAH WAKTU1 = 36 ?
           ACALL  HITKWH
DISPLAY    MOV    VAR5,KWH1
           MOV    VAR6,KWH2
           MOV    VAR7,KWH3
           MOV    VAR8,KWH4
           ACALL  DISP_KWH
           MOV    VAR5,UANG1
           MOV    VAR6,UANG2
           MOV    VAR7,UANG3
           MOV    VAR8,UANG4
```

```
MOV     A,#0C0H             ;BARIS 2
ACALL   SUB_LCD
ACALL   DISP_BIAYA
JB      P3.2,CEKDETIK
ACALL        TRANSMISI
AJMP    CEKDETIK
□
```

National Semiconductor Corporation

ADC0801, ADC0802, ADC0803, ADC0804, ADC0805 8-Bit μP Compatible A/D Converters

General Description

The ADC0801, ADC0802, ADC0803, ADC0804 and ADC0805 are CMOS 8-bit successive approximation A/D converters that use a differential potentiometric ladder—similar to the 256R products. These converters are designed to allow operation with the NSC800 and INS8080A derivative control bus with TRI-STATE® output latches directly driving the data bus. These A/Ds appear like memory locations or I/O ports to the microprocessor and no interfacing logic is needed.

Differential analog voltage inputs allow increasing the common-mode rejection and offsetting the analog zero input voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8 bits of resolution.

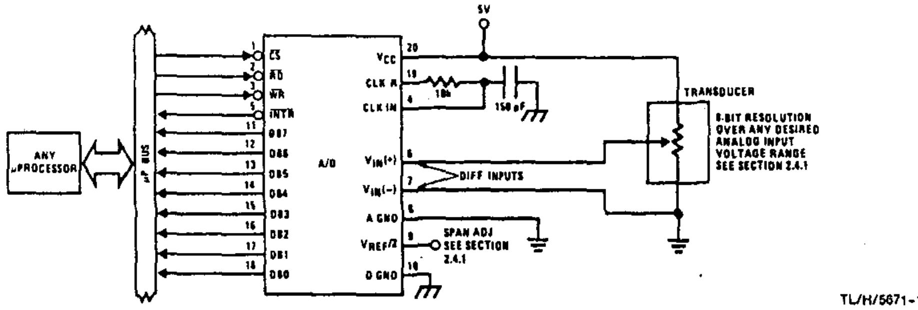
Features

- Compatible with 8080 μP derivatives—no interfacing logic needed - access time - 135 ns
- Easy interface to all microprocessors, or operates "stand alone"
- Differential analog voltage inputs
- Logic inputs and outputs meet both MOS and TTL voltage level specifications
- Works with 2.5V (LM336) voltage reference
- On-chip clock generator
- 0V to 5V analog input voltage range with single 5V supply
- No zero adjust required
- 0.3" standard width 20-pin DIP package
- 20-pin molded chip carrier or small outline package
- Operates ratiometrically or with 5 V_{DC}, 2.5 V_{DC}, or analog span adjusted voltage reference

Key Specifications

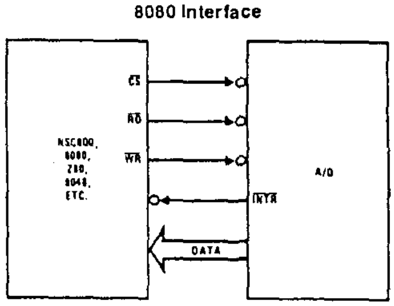
- Resolution: 8 bits
- Total error: ± ¼ LSB, ± ½ LSB and ± 1 LSB
- Conversion time: 100 μs

Typical Applications



TL/H/5671-1

8080 Interface



TL/H/5671-31

Error Specification (Includes Full-Scale, Zero Error, and Non-Linearity)			
Part Number	Full-Scale Adjusted	$V_{REF}/2 = 2.500\ V_{DC}$ (No Adjustments)	$V_{REF}/2$ = No Connection (No Adjustments)
ADC0801	± ¼ LSB		
ADC0802		± ½ LSB	
ADC0803	± ½ LSB		
ADC0804		± 1 LSB	
ADC0805			± 1 LSB

te Maximum Ratings (Notes 1 & 2)

Aerospace specified devices are required, e National Semiconductor Sales Office/ for availability and specifications.

ge (V_{CC}) (Note 3)	6.5V
trol Inputs	−0.3V to +18V
nput and Outputs	−0.3V to (V_{CC}+0.3V)
(Soldering, 10 seconds)	
ne Package (plastic)	260°C
ne Package (ceramic)	300°C
lount Package	
hase (60 seconds)	215°C
(15 seconds)	220°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation at T_A = 25°C	875 mW
ESD Susceptibility (Note 10)	800V

Operating Ratings (Notes 1 & 2)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
ADC0801/02LJ	−55°C ≤ T_A ≤ +125°C
ADC0801/02/03/04LCJ	−40°C ≤ T_A ≤ +85°C
ADC0801/02/03/05LCN	−40°C ≤ T_A ≤ +85°C
ADC0804LCN	0°C ≤ T_A ≤ +70°C
ADC0802/03/04LCV	0°C ≤ T_A ≤ +70°C
ADC0802/03/04LCWM	0°C ≤ T_A ≤ +70°C
Range of V_{CC}	4.5 V_{DC} to 6.3 V_{DC}

al Characteristics

g specifications apply for V_{CC} = 5 V_{DC}, $T_{MIN} \le T_A \le T_{MAX}$ and f_{CLK} = 640 kHz unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
otal Adjusted Error (Note 8)	With Full-Scale Adj. (See Section 2.5.2)			±¼	LSB
otal Unadjusted Error (Note 8)	$V_{REF}/2$ = 2.500 V_{DC}			±½	LSB
otal Adjusted Error (Note 8)	With Full-Scale Adj. (See Section 2.5.2)			±½	LSB
otal Unadjusted Error (Note 8)	$V_{REF}/2$ = 2.500 V_{DC}			±1	LSB
otal Unadjusted Error (Note 8)	$V_{REF}/2$-No Connection			±1	LSB
t Resistance (Pin 9)	ADC0801/02/03/05 ADC0804 (Note 9)	2.5 0.75	8.0 1.1		kΩ kΩ
Voltage Range	(Note 4) V(+) or V(−)	Gnd−0.05		V_{CC}+0.05	V_{DC}
-Mode Error	Over Analog Input Voltage Range		±1/16	±⅛	LSB
/ Sensitivity	V_{CC} = 5 V_{DC} ±10% Over Allowed $V_{IN}(+)$ and $V_{IN}(-)$ Voltage Range (Note 4)		±1/16	±⅛	LSB

trical Characteristics

g specifications apply for V_{CC} = 5 V_{DC} and T_A = 25°C unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Conversion Time	f_{CLK} = 640 kHz (Note 6)	103		114	μs
Conversion Time	(Note 5, 6)	66		73	$1/f_{CLK}$
Clock Frequency Clock Duty Cycle	V_{CC} = 5V, (Note 5) (Note 5)	100 40	640	1460 60	kHz %
Conversion Rate in Free-Running Mode	$\overline{INTR}$ tied to $\overline{WR}$ with $\overline{CS}$ = 0 V_{DC}, f_{CLK} = 640 kHz	8770		9708	conv/s
Width of $\overline{WR}$ Input (Start Pulse Width)	$\overline{CS}$ = 0 V_{DC} (Note 7)	100			ns
Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Data Valid)	C_L = 100 pF		135	200	ns
TRI-STATE Control (Delay from Rising Edge of $\overline{RD}$ to Hi-Z State)	C_L = 10 pF, R_L = 10k (See TRI-STATE Test Circuits)		125	200	ns
Delay from Falling Edge of $\overline{WR}$ or $\overline{RD}$ to Reset of $\overline{INTR}$			300	450	ns
Input Capacitance of Logic Control Inputs			5	7.5	pF
TRI-STATE Output Capacitance (Data Buffers)			5	7.5	pF
PUTS [Note: CLK IN (Pin 4) is the input of a Schmitt trigger circuit and is therefore specified separately]					
Logical "1" Input Voltage (Except Pin 4 CLK IN)	V_{CC} = 5.25 V_{DC}	2.0		15	V_{DC}

AC Electrical Characteristics (Continued)

The following specifications apply for $V_{CC} = 5V_{DC}$ and $T_{MIN} \leq T_A \leq T_{MAX}$, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CONTROL INPUTS [Note: CLK IN (Pin 4) is the input of a Schmitt trigger circuit and is therefore specified separately]						
V_{IN} (0)	Logical "0" Input Voltage (Except Pin 4 CLK IN)	$V_{CC} = 4.75\ V_{DC}$			0.8	V_{DC}
I_{IN} (1)	Logical "1" Input Current (All Inputs)	$V_{IN} = 5\ V_{DC}$		0.005	1	μA_{DC}
I_{IN} (0)	Logical "0" Input Current (All Inputs)	$V_{IN} = 0\ V_{DC}$	−1	−0.005		μA_{DC}
CLOCK IN AND CLOCK R						
V_T+	CLK IN (Pin 4) Positive Going Threshold Voltage		2.7	3.1	3.5	V_{DC}
V_T-	CLK IN (Pin 4) Negative Going Threshold Voltage		1.5	1.8	2.1	V_{DC}
V_H	CLK IN (Pin 4) Hysteresis $(V_T+)-(V_T-)$		0.6	1.3	2.0	V_{DC}
V_{OUT} (0)	Logical "0" CLK R Output Voltage	$I_O = 360\ \mu A$, $V_{CC} = 4.75\ V_{DC}$			0.4	V_{DC}
V_{OUT} (1)	Logical "1" CLK R Output Voltage	$I_O = -360\ \mu A$, $V_{CC} = 4.75\ V_{DC}$	2.4			V_{DC}
DATA OUTPUTS AND $\overline{INTR}$						
V_{OUT} (0)	Logical "0" Output Voltage Data Outputs $\overline{INTR}$ Output	 $I_{OUT} = 1.6$ mA, $V_{CC} = 4.75\ V_{DC}$ $I_{OUT} = 1.0$ mA, $V_{CC} = 4.75\ V_{DC}$			 0.4 0.4	 V_{DC} V_{DC}
V_{OUT} (1)	Logical "1" Output Voltage	$I_O = -360\ \mu A$, $V_{CC} = 4.75\ V_{DC}$	2.4			V_{DC}
V_{OUT} (1)	Logical "1" Output Voltage	$I_O = -10\ \mu A$, $V_{CC} = 4.75\ V_{DC}$	4.5			V_{DC}
I_{OUT}	TRI-STATE Disabled Output Leakage (All Data Buffers)	$V_{OUT} = 0\ V_{DC}$ $V_{OUT} = 5\ V_{DC}$	−3		 3	μA_{DC} μA_{DC}
I_{SOURCE}		V_{OUT} Short to Gnd, $T_A = 25°C$	4.5	6		mA_{DC}
I_{SINK}		V_{OUT} Short to V_{CC}, $T_A = 25°C$	9.0	16		mA_{DC}
POWER SUPPLY						
I_{CC}	Supply Current (Includes Ladder Current) ADC0801/02/03/04LCJ/05 ADC0804LCN/LCV/LCWM	$f_{CLK} = 640$ kHz, $V_{REF}/2 = $ NC, $T_A = 25°C$ and $\overline{CS} = 5V$		 1.1 1.9	 1.8 2.5	 mA mA

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions

Note 2: All voltages are measured with respect to Gnd, unless otherwise specified. The separate A Gnd point should always be wired to the D Gnd.

Note 3: A zener diode exists, internally, from V_{CC} to Gnd and has a typical breakdown voltage of 7 V_{DC}.

Note 4: For $V_{IN}(-) \geq V_{IN}(+)$ the digital output code will be 0000 0000. Two on-chip diodes are tied to each analog input (see block diagram) which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the V_{CC} supply. Be careful, during testing at low V_{CC} levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct—especially at elevated temperatures, and cause errors for analog inputs near full-scale. The spec allows 50 mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 50 mV, the output code will be correct. To achieve an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.950 V_{DC} over temperature variations, initial tolerance and loading.

Note 5: Accuracy is guaranteed at $f_{CLK} = 640$ kHz. At higher clock frequencies accuracy can degrade. For lower clock frequencies, the duty cycle limits can be extended so long as the minimum clock high time interval or minimum clock low time interval is no less than 275 ns.

Note 6: With an asynchronous start pulse, up to 8 clock periods may be required before the internal clock phases are proper to start the conversion process. The start request is internally latched, see *Figure 2* and section 2.0.

Note 7: The $\overline{CS}$ input is assumed to bracket the $\overline{WR}$ strobe input and therefore timing is dependent on the $\overline{WR}$ pulse width. An arbitrarily wide pulse width will hold the converter in a reset mode and the start of conversion is initiated by the low to high transition of the $\overline{WR}$ pulse (see timing diagrams).

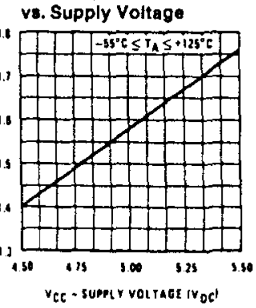
Note 8: None of these A/Ds requires a zero adjust (see section 2.5.1). To obtain zero code at other analog input voltages see section 2.5 and *Figure 5*.

Note 9: The $V_{REF}/2$ pin is the center point of a two resistor divider connected from V_{CC} to ground. Each resistor is 2.2k, except for the ADC0804LCJ where each resistor is 16k. Total ladder input resistance is the sum of the two equal resistors.

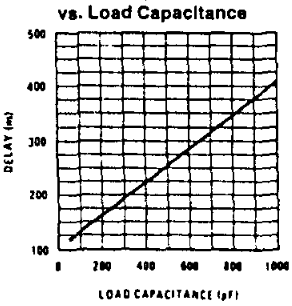
Note 10: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

pical Performance Characteristics

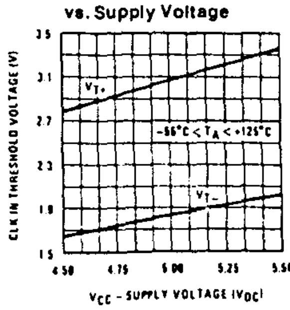
Logic Input Threshold Voltage vs. Supply Voltage



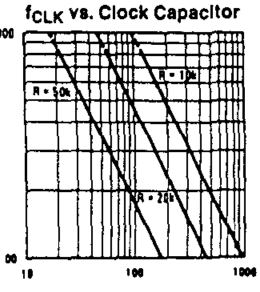
Delay From Falling Edge of $\overline{RD}$ to Output Data Valid vs. Load Capacitance



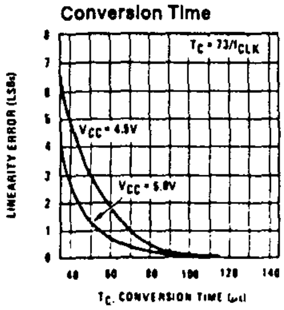
CLK IN Schmitt Trip Levels vs. Supply Voltage



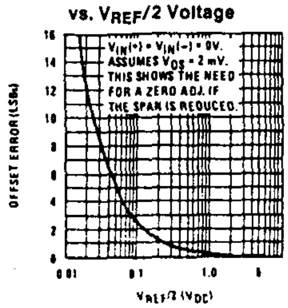
f_{CLK} vs. Clock Capacitor



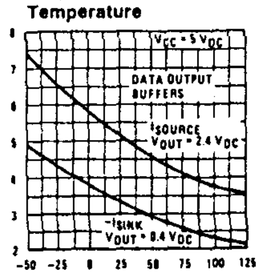
Full-Scale Error vs Conversion Time



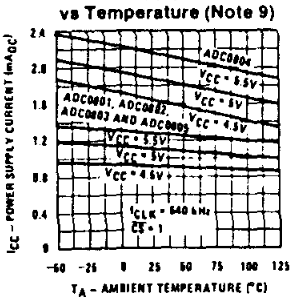
Effect of Unadjusted Offset Error vs. $V_{REF}/2$ Voltage



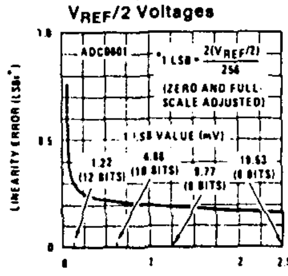
Output Current vs Temperature



Power Supply Current vs Temperature (Note 9)



Linearity Error at Low $V_{REF}/2$ Voltages



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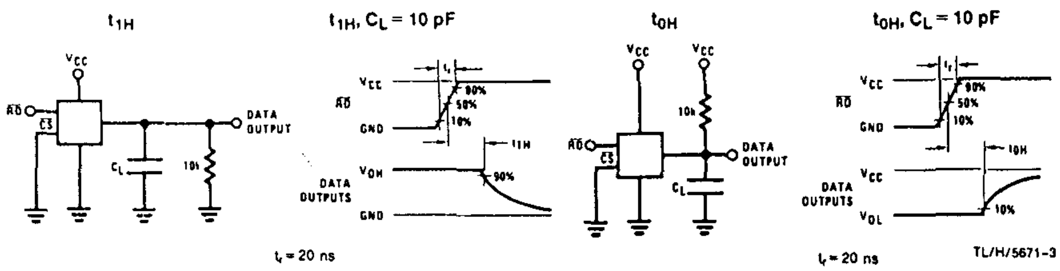
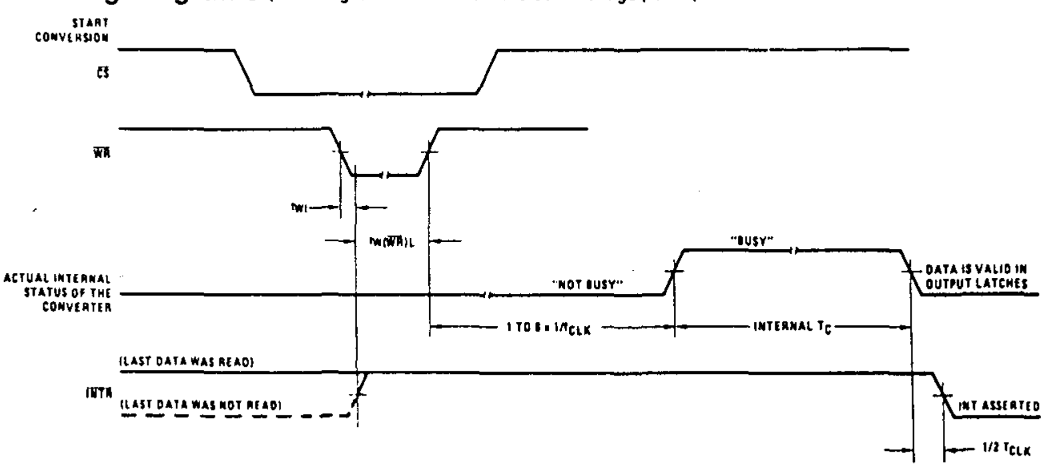
TRI-STATE Test Circuits and Waveforms

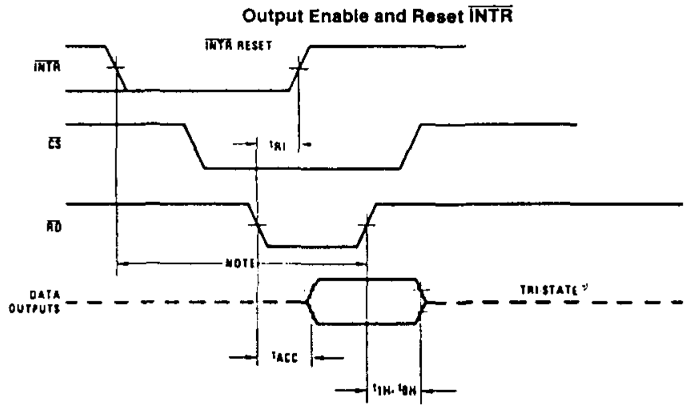


TL/H/5671-3

Timing Diagrams (All timing is measured from the 50% voltage points)



Output Enable and Reset $\overline{INTR}$



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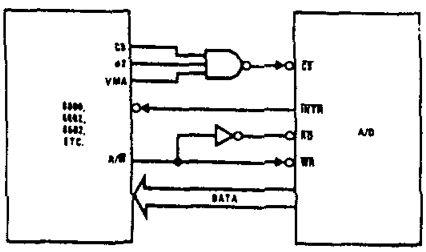
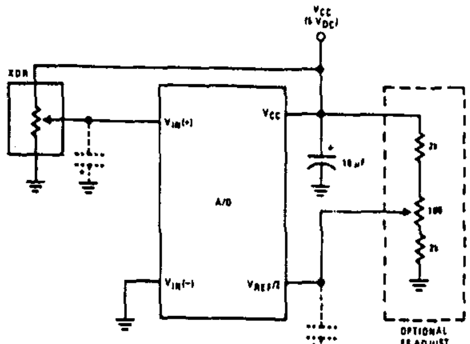
Note: Read strobe must occur 8 clock periods ($8/f_{CLK}$) after assertion of interrupt to guarantee reset of $\overline{INTR}$.

Typical Applications (Continued)

6800 Interface

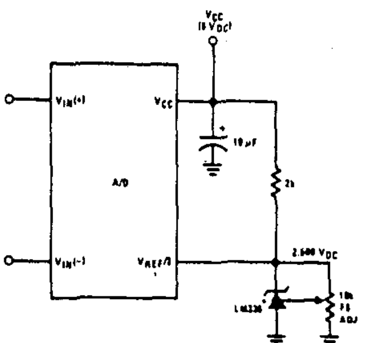


Ratiometric with Full-Scale Adjust



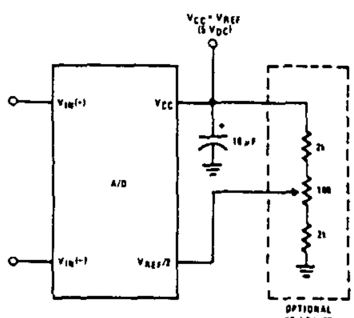
Note: before using caps at V_{IN} or $V_{REF}/2$, see section 2.3.2 Input Bypass Capacitors.

Absolute with a 2.500V Reference

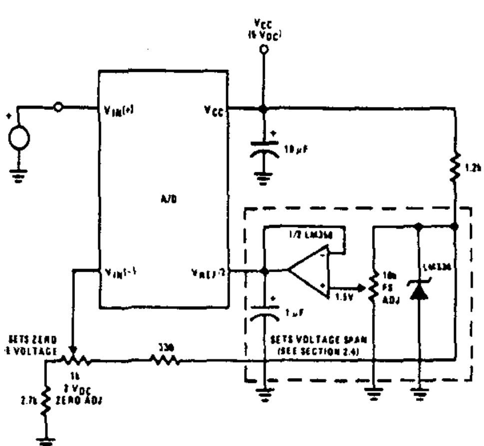


*For low power, see also LM385-2.5

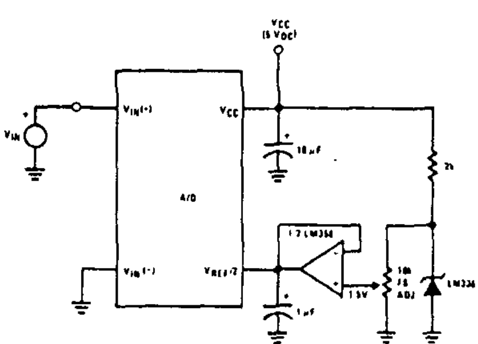
Absolute with a 5V Reference



Zero-Shift and Span Adjust: $2V \leq V_{IN} \leq 5V$



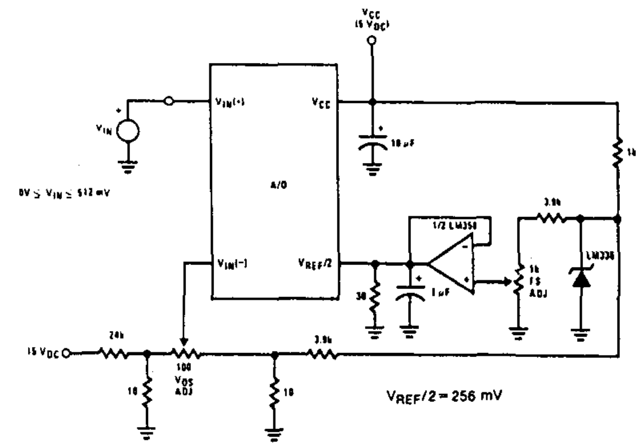
Span Adjust: $0V \leq V_{IN} \leq 3V$



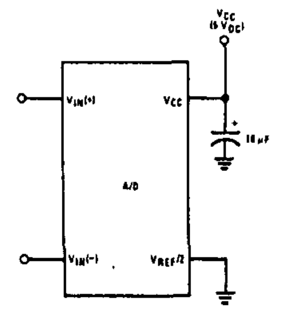
TL/H/5671-5

Typical Applications (Continued)

Directly Converting a Low-Level Signal



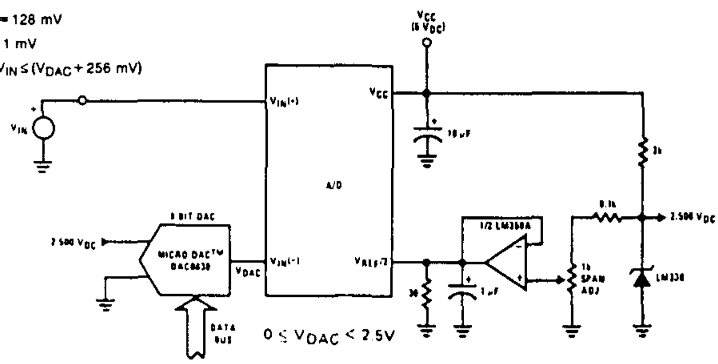
A μP Interfaced Comparator



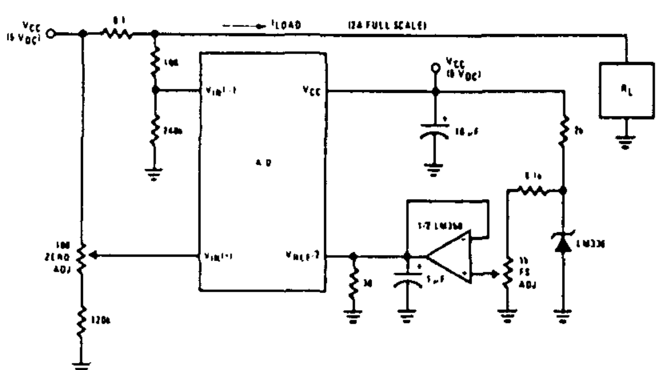
For: $V_{IN}(+) > V_{IN}(-)$
Output = FF_{HEX}
For: $V_{IN}(+) < V_{IN}(-)$
Output = 00_{HEX}

1 mV Resolution with μP Controlled Range

$V_{REF}/2 = 128$ mV
1 LSB = 1 mV
$V_{DAC} \le V_{IN} \le (V_{DAC} + 256 \text{ mV})$



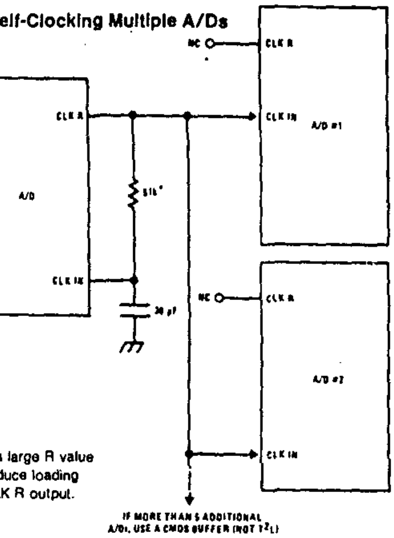
Digitizing a Current Flow



TL/H/5671-6

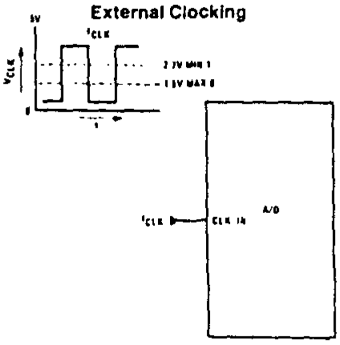
al Applications (Continued)

elf-Clocking Multiple A/Ds



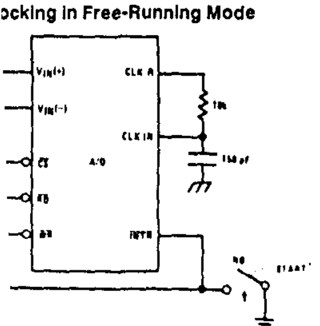
large R value
duce loading
K R output.

External Clocking



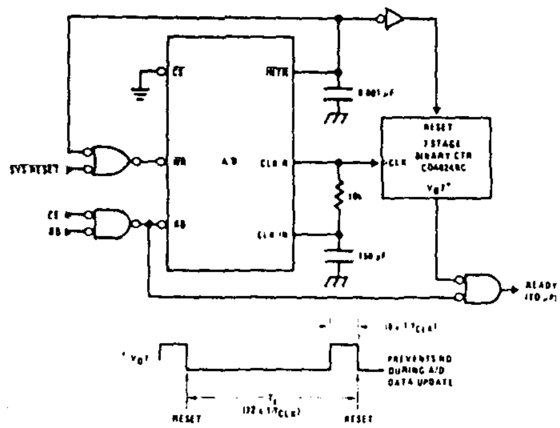
100 kHz ≤ f_{CLK} ≤ 1460 kHz

ocking in Free-Running Mode

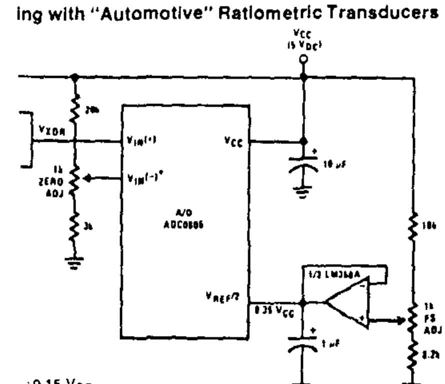


up, a momentary grounding
put is needed to guarantee operation.

µP Interface for Free-Running A/D

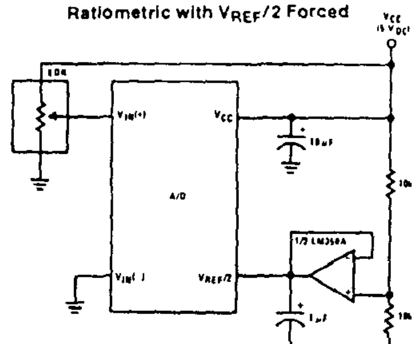


ing with "Automotive" Ratiometric Transducers



:0.15 V_{CC}
$V_{CC} \le V_{XDR} \le 85\%$ of V_{CC}

Ratiometric with $V_{REF}/2$ Forced



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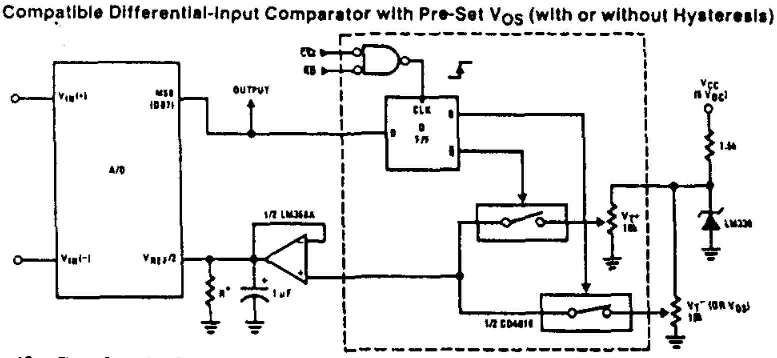
3

Typical Applications (Continued)

μP Compatible Differential-Input Comparator with Pre-Set V_{OS} (with or without Hysteresis)

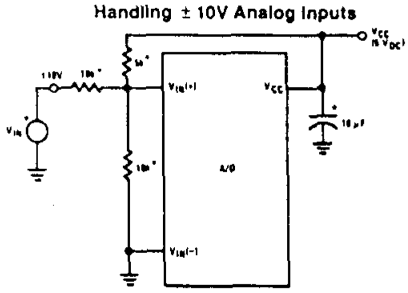


*See *Figure 5* to select R value

DB7 = "1" for $V_{IN}(+) > V_{IN}(-) + (V_{REF}/2)$

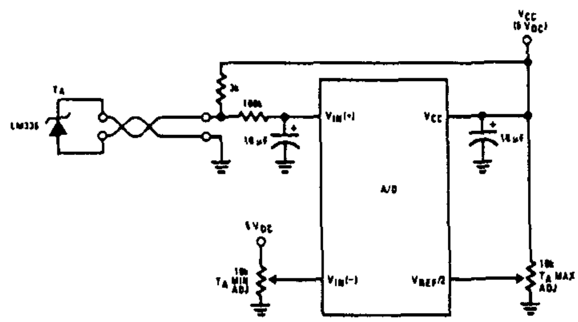
Omit circuitry within the dotted area if hysteresis is not needed

Handling ± 10V Analog Inputs

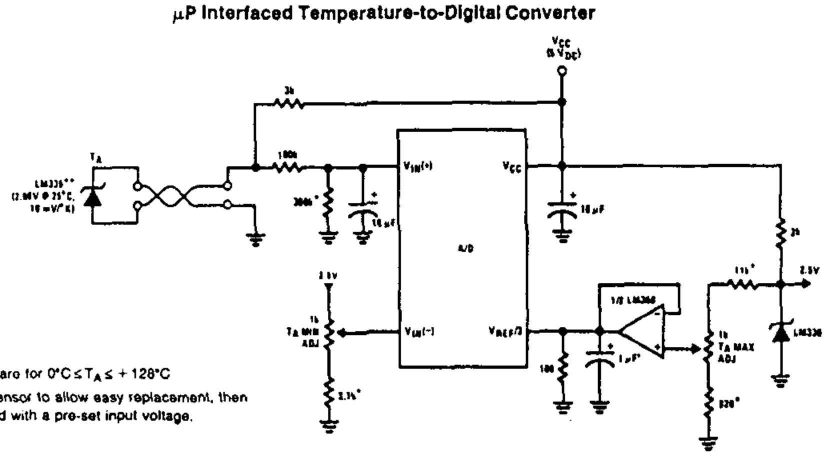


*Beckman Instruments #694-3-R10K resistor array

Low-Cost, μP Interfaced, Temperature-to-Digital Converter



μP Interfaced Temperature-to-Digital Converter



*Circuit values shown are for $0°C \le T_A \le +128°C$

**Can calibrate each sensor to allow easy replacement, then A/D can be calibrated with a pre-set input voltage.

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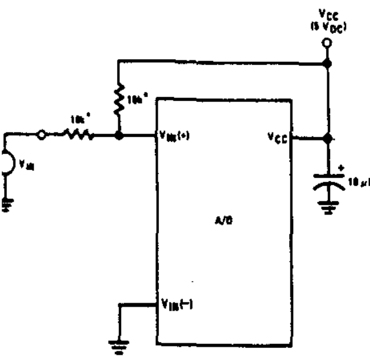
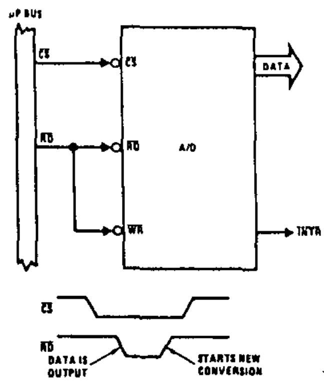
cal Applications (Continued)

Handling ±5V Analog Inputs

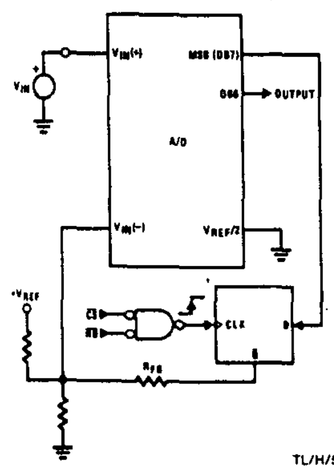


*Beckman Instruments #694-3-R10K resistor array

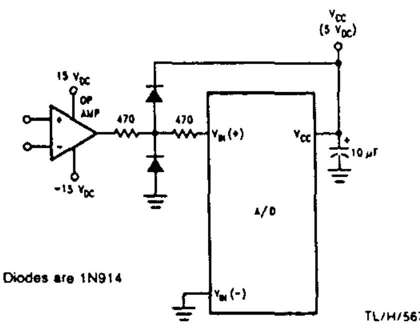
Read-Only Interface



µP Interfaced Comparator with Hysteresis

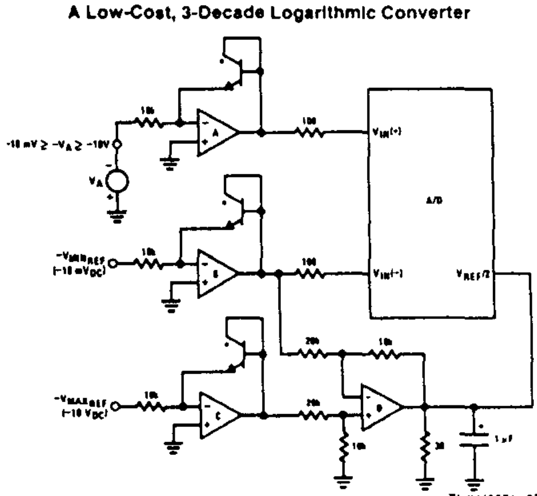


Protecting the Input



Diodes are 1N914

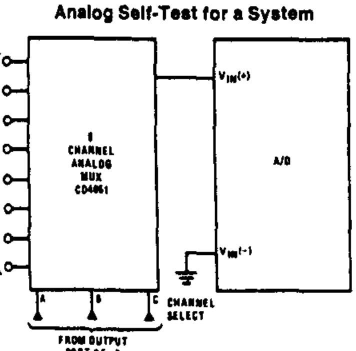
A Low-Cost, 3-Decade Logarithmic Converter



*LM389 transistors

A, B, C, D = LM324A quad op amp

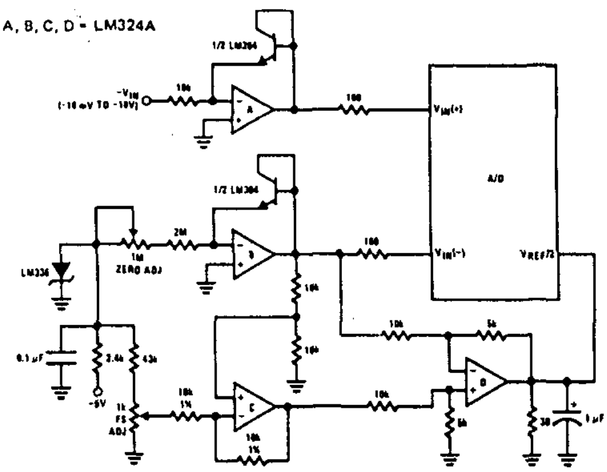
Analog Self-Test for a System



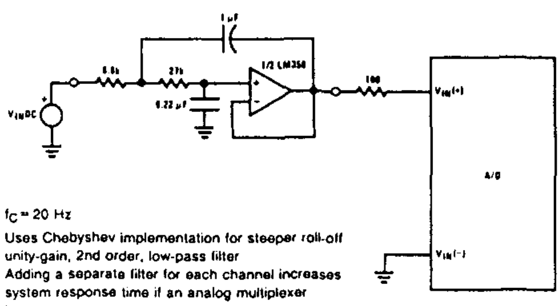
3

Typical Applications (Continued)

3-Decade Logarithmic A/D Converter

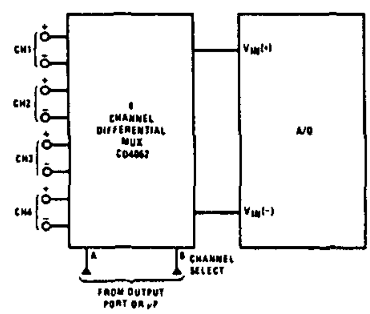


Noise Filtering the Analog Input

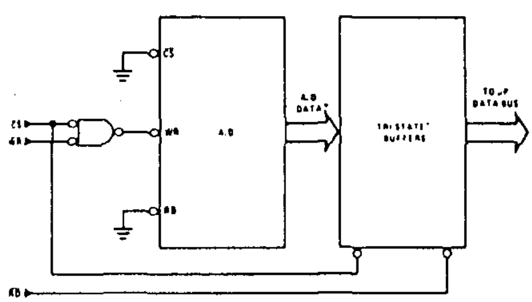


$f_C = 20$ Hz
Uses Chebyshev implementation for steeper roll-off unity-gain, 2nd order, low-pass filter
Adding a separate filter for each channel increases system response time if an analog multiplexer is used

Multiplexing Differential Inputs

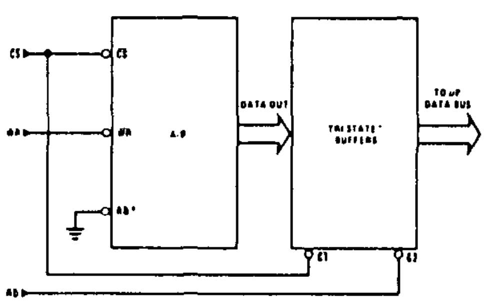


Output Buffers with A/D Data Enabled



*A/D output data is updated 1 CLK period prior to assertion of $\overline{INTR}$

Increasing Bus Drive and/or Reducing Time on Bus

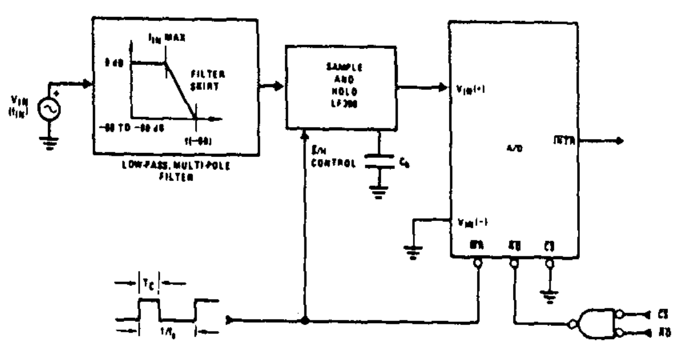


TL/H/5671-10

*Allows output data to set-up at falling edge of $\overline{CS}$

Typical Applications (Continued)

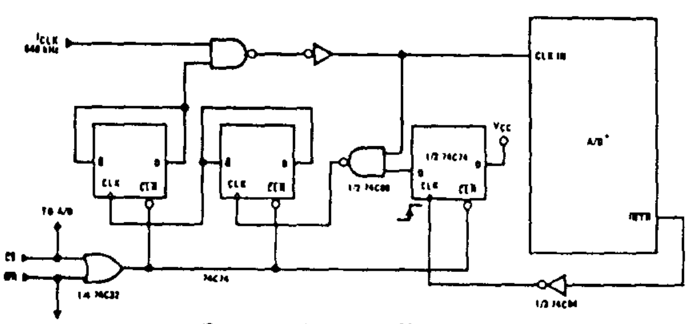
Sampling an AC Input Signal



Note 1: Oversample whenever possible [keep fs > 2f(−60)] to eliminate input frequency folding (aliasing) and to allow for the skirt response of the filter.

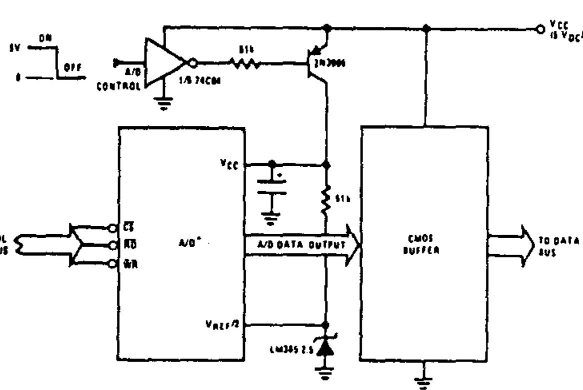
Note 2: Consider the amplitude errors which are introduced within the passband of the filter.

70% Power Savings by Clock Gating



(Complete shutdown takes ≈ 30 seconds.)

Power Savings by A/D and V_{REF} Shutdown



TL/H/5671–11

*Use ADC0801, 02, 03 or 05 for lowest power consumption.

Note: Logic inputs can be driven to V_{CC} with A/D supply at zero volts.

Buffer prevents data bus from overdriving output of A/D when in shutdown mode.

Functional Description

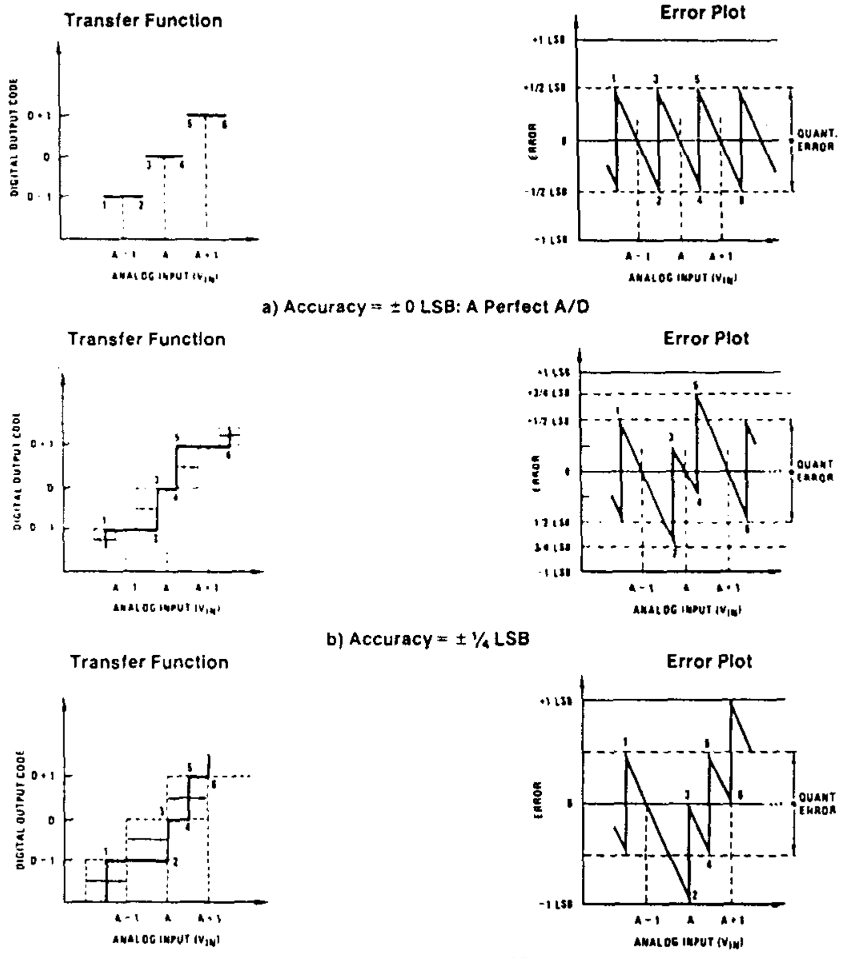
1.0 UNDERSTANDING A/D ERROR SPECS

A perfect A/D transfer characteristic (staircase waveform) is shown in *Figure 1a*. The horizontal scale is analog input voltage and the particular points labeled are in steps of 1 LSB (19.53 mV with 2.5V tied to the $V_{REF}/2$ pin). The digital output codes that correspond to these inputs are shown as D−1, D, and D+1. For the perfect A/D, not only will center-value (A−1, A, A+1, ...) analog inputs produce the correct output ditigal codes, but also each riser (the transitions between adjacent output codes) will be located ±½ LSB away from each center-value. As shown, the risers are ideal and have no width. Correct digital output codes will be provided for a range of analog input voltages that extend ±½ LSB from the ideal center-values. Each tread (the range of analog input voltage that provides the same digital output code) is therefore 1 LSB wide.

Figure 1b shows a worst case error plot for the ADC0801. All center-valued inputs are guaranteed to produce the correct output codes and the adjacent risers are guaranteed to be no closer to the center-value points than ±¼ LSB. In other words, if we apply an analog input equal to the center-value ±¼ LSB, *we guarantee* that the A/D will produce the correct digital code. The maximum range of the position of the code transition is indicated by the horizontal arrow and it is guaranteed to be no more than ½ LSB.

The error curve of *Figure 1c* shows a worst case error plot for the ADC0802. Here we guarantee that if we apply an analog input equal to the LSB analog voltage center-value the A/D will produce the correct digital code.

Next to each transfer function is shown the corresponding error plot. Many people may be more familiar with error plots than transfer functions. The analog input voltage to the A/D is provided by either a linear ramp or by the discrete output steps of a high resolution DAC. Notice that the error is continuously displayed and includes the quantization uncertainty of the A/D. For example the error at point 1 of *Figure 1a* is +½ LSB because the digital code appeared ½ LSB in advance of the center-value of the tread. The error plots always have a constant negative slope and the abrupt upside steps are always 1 LSB in magnitude.



a) Accuracy = ±0 LSB: A Perfect A/D

b) Accuracy = ±¼ LSB

c) Accuracy = ±½ LSB

TL/H/5671-12

FIGURE 1. Clarifying the Error Specs of an A/D Converter

Functional Description (Continued)

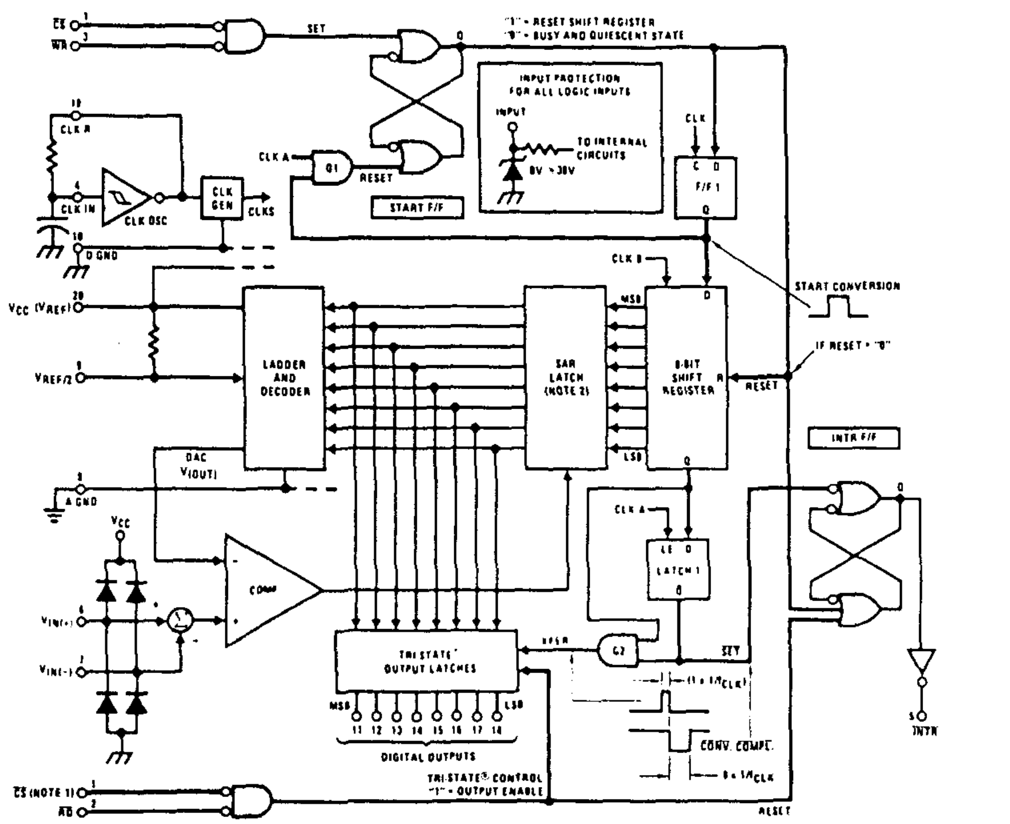
2.0 FUNCTIONAL DESCRIPTION

The ADC0801 series contains a circuit equivalent of the 256R network. Analog switches are sequenced by successive approximation logic to match the analog difference input voltage $[V_{IN}(+) - V_{IN}(-)]$ to a corresponding tap on the R network. The most significant bit is tested first and after 8 comparisons (64 clock cycles) a digital 8-bit binary code (1111 1111 = full-scale) is transferred to an output latch and then an interrupt is asserted ($\overline{INTR}$ makes a high-to-low transition). A conversion in process can be interrupted by issuing a second start command. The device may be operated in the free-running mode by connecting $\overline{INTR}$ to the $\overline{WR}$ input with $\overline{CS} = 0$. To ensure start-up under all possible conditions, an external $\overline{WR}$ pulse is required during the first power-up cycle.

On the high-to-low transition of the $\overline{WR}$ input the internal SAR latches and the shift register stages are reset. As long as the $\overline{CS}$ input and $\overline{WR}$ input remain low, the A/D will remain in a reset state. *Conversion will start from 1 to 8 clock periods after at least one of these inputs makes a low-to-high transition.*

A functional diagram of the A/D converter is shown in *Figure 2*. All of the package pinouts are shown and the major logic control paths are drawn in heavier weight lines.

The converter is started by having $\overline{CS}$ and $\overline{WR}$ simultaneously low. This sets the start flip-flop (F/F) and the resulting "1" level resets the 8-bit shift register, resets the Interrupt (INTR) F/F and inputs a "1" to the D flop, F/F1, which is at the input end of the 8-bit shift register. Internal clock signals then transfer this "1" to the Q output of F/F1. The AND gate, G1, combines this "1" output with a clock signal to provide a reset signal to the start F/F. If the set signal is no longer present (either $\overline{WR}$ or $\overline{CS}$ is a "1") the start F/F is reset and the 8-bit shift register then can have the "1" clocked in, which starts the conversion process. If the set signal were to still be present, this reset pulse would have no effect (both outputs of the start F/F would momentarily be at a "1" level) and the 8-bit shift register would continue to be held in the reset mode. This logic therefore allows for wide $\overline{CS}$ and $\overline{WR}$ signals and the converter will start after at least one of these signals returns high and the internal clocks again provide a reset signal for the start F/F.



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Note 1: $\overline{CS}$ shown twice for clarity.

Note 2: SAR = Successive Approximation Register.

FIGURE 2. Block Diagram

Functional Description (Continued)

After the "1" is clocked through the 8-bit shift register (which completes the SAR search) it appears as the input to the D-type latch, LATCH 1. As soon as this "1" is output from the shift register, the AND gate, G2, causes the new digital word to transfer to the TRI-STATE output latches. When LATCH 1 is subsequently enabled, the Q output makes a high-to-low transition which causes the INTR F/F to set. An inverting buffer then supplies the $\overline{\text{INTR}}$ input signal.

Note that this $\overline{\text{SET}}$ control of the INTR F/F remains low for 8 of the external clock periods (as the internal clocks run at ⅛ of the frequency of the external clock). If the data output is continuously enabled ($\overline{\text{CS}}$ and $\overline{\text{RD}}$ both held low), the $\overline{\text{INTR}}$ output will still signal the end of conversion (by a high-to-low transition), because the $\overline{\text{SET}}$ input can control the Q output of the INTR F/F even though the RESET input is constantly at a "1" level in this operating mode. This $\overline{\text{INTR}}$ output will therefore stay low for the duration of the $\overline{\text{SET}}$ signal, which is 8 periods of the external clock frequency (assuming the A/D is not started during this interval).

When operating in the free-running or continuous conversion mode ($\overline{\text{INTR}}$ pin tied to $\overline{\text{WR}}$ and $\overline{\text{CS}}$ wired low—see also section 2.8), the START F/F is SET by the high-to-low transition of the $\overline{\text{INTR}}$ signal. This resets the SHIFT REGISTER which causes the input to the D-type latch, LATCH 1, to go low. As the latch enable input is still present, the $\overline{\text{Q}}$ output will go high, which then allows the INTR F/F to be RESET. This reduces the width of the resulting $\overline{\text{INTR}}$ output pulse to only a few propagation delays (approximately 300 ns).

When data is to be read, the combination of both $\overline{\text{CS}}$ and $\overline{\text{RD}}$ being low will cause the INTR F/F to be reset and the TRI-STATE output latches will be enabled to provide the 8-bit digital outputs.

2.1 Digital Control Inputs

The digital control inputs ($\overline{\text{CS}}$, $\overline{\text{RD}}$, and $\overline{\text{WR}}$) meet standard T^2L logic voltage levels. These signals have been renamed when compared to the standard A/D Start and Output Enable labels. In addition, these inputs are active low to allow an easy interface to microprocessor control busses. For non-microprocessor based applications, the $\overline{\text{CS}}$ input (pin 1) can be grounded and the standard A/D Start function is obtained by an active low pulse applied at the $\overline{\text{WR}}$ input (pin 3) and the Output Enable function is caused by an active low pulse at the $\overline{\text{RD}}$ input (pin 2).

2.2 Analog Differential Voltage Inputs and Common-Mode Rejection

This A/D has additional applications flexibility due to the analog differential voltage input. The $V_{IN}(-)$ input (pin 7) can be used to automatically subtract a fixed voltage value from the input reading (tare correction). This is also useful in 4 mA–20 mA current loop conversion. In addition, common-mode noise can be reduced by use of the differential input.

The time interval between sampling $V_{IN}(+)$ and $V_{IN}(-)$ is 4-½ clock periods. The maximum error voltage due to this slight time difference between the input voltage samples is given by:

$$\Delta V_e(\text{MAX}) = (V_P)(2\pi f_{cm})\left(\frac{4.5}{f_{CLK}}\right),$$

where:

ΔV_e is the error voltage due to sampling delay

V_P is the peak value of the common-mode voltage

f_{cm} is the common-mode frequency

As an example, to keep this error to ¼ LSB (~5 mV) when operating with a 60 Hz common-mode frequency, f_{cm}, and using a 640 kHz A/D clock, f_{CLK}, would allow a peak value of the common-mode voltage, V_P, which is given by:

$$V_P = \frac{[\Delta V_{e(MAX)}(f_{CLK})]}{(2\pi f_{cm})(4.5)}$$

or

$$V_P = \frac{(5\times 10^{-3})(640\times 10^3)}{(6.28)(60)(4.5)}$$

which gives

$V_P \cong 1.9V.$

The allowed range of analog input voltages usually places more severe restrictions on input common-mode noise levels.

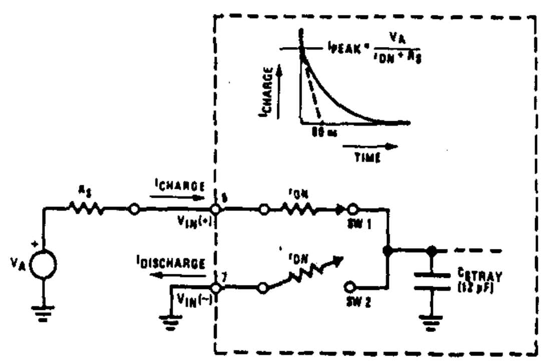
An analog input voltage with a reduced span and a relatively large zero offset can be handled easily by making use of the differential input (see section 2.4 Reference Voltage).

2.3 Analog Inputs

2.3.1 Input Current

Normal Mode

Due to the internal switching action, displacement currents will flow at the analog inputs. This is due to on-chip stray capacitance to ground as shown in *Figure 3*.



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r_{ON} of SW 1 and SW 2 ≅ 5 kΩ

$\tau = r_{ON}\,C_{STRAY} \cong 5\ k\Omega \times 12\ pF = 60\ ns$

FIGURE 3. Analog Input Impedance

tional Description (Continued)

ge on this capacitance is switched and will result in entering the $V_{IN}(+)$ input pin and leaving the nput which will depend on the analog differential tage levels. These current transients occur at the dge of the internal clocks. They rapidly decay and *ause errors* as the on-chip comparator is strobed at of the clock period.

de

ltage source applied to the $V_{IN}(+)$ or $V_{IN}(-)$ pin the allowed operating range of $V_{CC}+50$ mV, large rents can flow through a parasitic diode to the V_{CC} ese currents can exceed the 1 mA max allowed external diode (1N914) should be added to bypass ent to the V_{CC} pin (with the current bypassed with e, the voltage at the $V_{IN}(+)$ pin can exceed the age by the forward voltage of this diode).

ut Bypass Capacitors

capacitors at the inputs will average these charges se a DC current to flow through the output resist- the analog signal sources. This charge pumping worse for continuous conversions with the $V_{IN}(+)$ tage at full-scale. For continuous conversions with Hz clock frequency with the $V_{IN}(+)$ input at 5V, this ent is at a maximum of approximately 5 µA. There- *oass capacitors should not be used at the analog r the $V_{REF}/2$ pin* for high resistance sources (> 1 put bypass capacitors are necessary for noise filter- high source resistance is desirable to minimize ca- size, the detrimental effects of the voltage drop his input resistance, which is due to the average the input current, can be eliminated with a full-scale ent while the given source resistor and input bypass r are both in place. This is possible because the value of the input current is a precise linear func- he differential input voltage.

ut Source Resistance

alues of source resistance where an input bypass r is not used, *will not cause errors* as the input cur- ttle out prior to the comparison time. If a low pass equired in the system, use a low valued series resis- kΩ) for a passive RC section or add an op amp RC ow pass filter. For low source resistance applica- : 1 kΩ), a 0.1 µF bypass capacitor at the inputs will noise pickup due to series lead inductance of a long 100Ω series resistor can be used to isolate this ca- -both the R and C are placed outside the feedback om the output of an op amp, if used.

ise

ds to the analog inputs (pin 6 and 7) should be kept as possible to minimize input noise coupling. Both nd undesired digital clock coupling to these inputs se system errors. The source resistance for these hould, in general, be kept below 5 kΩ. Larger values ce resistance can cause undesired system noise Input bypass capacitors, placed from the analog in- ground, will eliminate system noise pickup but can nalog scale errors as these capacitors will average sient input switching currents of the A/D (see sec- 1.). This scale error depends on both a large source resistance and the use of an input bypass capacitor. This error can be eliminated by doing a full-scale adjustment of the A/D (adjust $V_{REF}/2$ for a proper full-scale reading—see section 2.5.2 on Full-Scale Adjustment) with the source re- sistance and input bypass capacitor in place.

2.4 Reference Voltage

2.4.1 Span Adjust

For maximum applications flexibility, these A/Ds have been designed to accommodate a 5 V_{DC}, 2.5 V_{DC} or an adjusted voltage reference. This has been achieved in the design of the IC as shown in *Figure 4*.

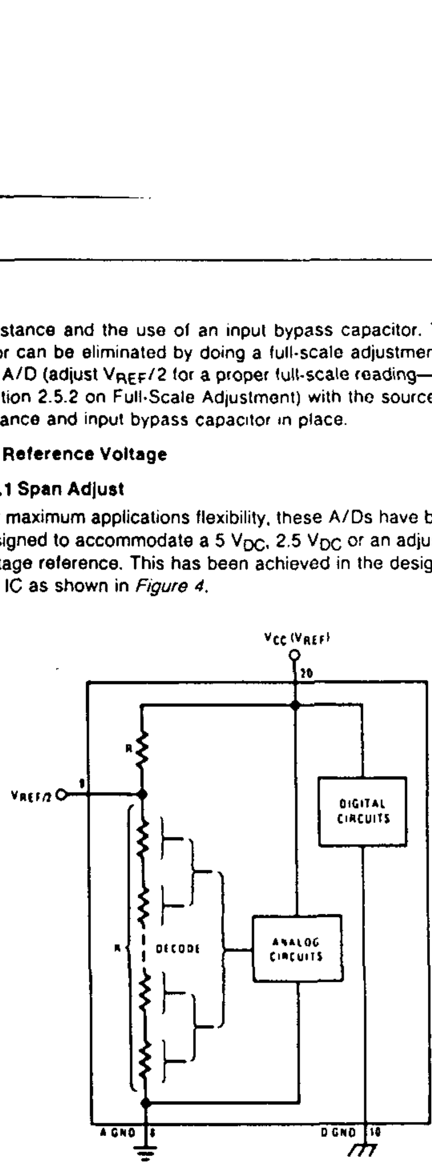

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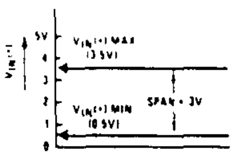
FIGURE 4. The $V_{REFERENCE}$ Design on the IC

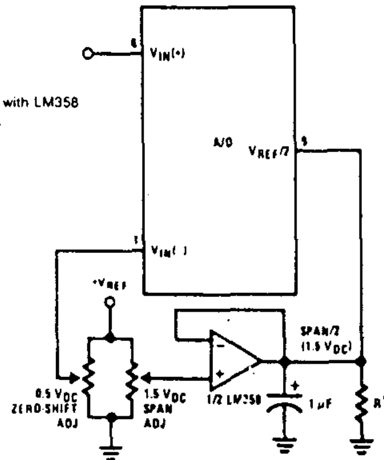
Notice that the reference voltage for the IC is either ½ of the voltage applied to the V_{CC} supply pin, or is equal to the voltage that is externally forced at the $V_{REF}/2$ pin. This al- lows for a ratiometric voltage reference using the V_{CC} sup- ply, a 5 V_{DC} reference voltage can be used for the V_{CC} supply or a voltage less than 2.5 V_{DC} can be applied to the $V_{REF}/2$ input for increased application flexibility. The inter- nal gain to the $V_{REF}/2$ input is 2, making the full-scale differ- ential input voltage twice the voltage at pin 9.

An example of the use of an adjusted reference voltage is to accommodate a reduced span—or dynamic voltage range of the analog input voltage. If the analog input voltage were to range from 0.5 V_{DC} to 3.5 V_{DC}, instead of 0V to 5 V_{DC}, the span would be 3V as shown in *Figure 5*. With 0.5 V_{DC} applied to the $V_{IN}(-)$ pin to absorb the offset, the reference voltage can be made equal to ½ of the 3V span or 1.5 V_{DC}. The A/D now will encode the $V_{IN}(+)$ signal from 0.5V to 3.5 V with the 0.5V input corresponding to zero and the 3.5 V_{DC} input corresponding to full-scale. The full 8 bits of resolution are therefore applied over this reduced analog input voltage range.

Functional Description (Continued)



a) Analog Input Signal Example



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b) Accommodating an Analog Input from 0.5V (Digital Out = = 00_{HEX}) to 3.5V (Digital Out = FF_{HEX})

FIGURE 5. Adapting the A/D Analog Input Voltages to Match an Arbitrary Input Signal Range

2.4.2 Reference Accuracy Requirements

The converter can be operated in a ratiometric mode or an absolute mode. In ratiometric converter applications, the magnitude of the reference voltage is a factor in both the output of the source transducer and the output of the A/D converter and therefore cancels out in the final digital output code. The ADC0805 is specified particularly for use in ratiometric applications with no adjustments required. In absolute conversion applications, both the initial value and the temperature stability of the reference voltage are important factors in the accuracy of the A/D converter. For $V_{REF}/2$ voltages of 2.4 V_{DC} nominal value, initial errors of ± 10 mV_{DC} will cause conversion errors of ± 1 LSB due to the gain of 2 of the $V_{REF}/2$ input. In reduced span applications, the initial value and the stability of the $V_{REF}/2$ input voltage become even more important. For example, if the span is reduced to 2.5V, the analog input LSB voltage value is correspondingly reduced from 20 mV (5V span) to 10 mV and 1 LSB at the $V_{REF}/2$ input becomes 5 mV. As can be seen, this reduces the allowed initial tolerance of the reference voltage and requires correspondingly less absolute change with temperature variations. Note that spans smaller than 2.5V place even tighter requirements on the initial accuracy and stability of the reference source.

In general, the magnitude of the reference voltage will require an initial adjustment. Errors due to an improper value of reference voltage appear as full-scale errors in the A/D transfer function. IC voltage regulators may be used for references if the ambient temperature changes are not excessive. The LM336B 2.5V IC reference diode (from National Semiconductor) has a temperature stability of 1.8 mV typ (6 mV max) over $0°C \le T_A \le +70°C$. Other temperature range parts are also available.

2.5 Errors and Reference Voltage Adjustments

2.5.1 Zero Error

The zero of the A/D does not require adjustment. If the minimum analog input voltage value, $V_{IN(MIN)}$, is not ground, a zero offset can be done. The converter can be made to output 0000 0000 digital code for this minimum input voltage by biasing the A/D $V_{IN}(-)$ input at this $V_{IN(MIN)}$ value (see Applications section). This utilizes the differential mode operation of the A/D.

The zero error of the A/D converter relates to the location of the first riser of the transfer function and can be measured by grounding the $V_{IN}(-)$ input and applying a small magnitude positive voltage to the $V_{IN}(+)$ input. Zero error is the difference between the actual DC input voltage that is necessary to just cause an output digital code transition from 0000 0000 to 0000 0001 and the ideal ½ LSB value (½ LSB = 9.8 mV for $V_{REF}/2 = 2.500\ V_{DC}$).

2.5.2 Full-Scale

The full-scale adjustment can be made by applying a differential input voltage that is 1½ LSB less than the desired analog full-scale voltage range and then adjusting the magnitude of the $V_{REF}/2$ input (pin 9 or the V_{CC} supply if pin 9 is not used) for a digital output code that is just changing from 1111 1110 to 1111 1111.

'unctional Description (Continued)

.5.3 Adjusting for an Arbitrary Analog Input Voltage Range

the analog zero voltage of the A/D is shifted away from round (for example, to accommodate an analog input sig- al that does not go to ground) this new zero reference hould be properly adjusted first. A $V_{IN}(+)$ voltage that quals this desired zero reference plus ½ LSB (where the SB is calculated for the desired analog span, 1 LSB = ana- g span/256) is applied to pin 6 and the zero reference oltage at pin 7 should then be adjusted to just obtain the 0_{HEX} to 01_{HEX} code transition.

he full-scale adjustment should then be made (with the roper $V_{IN}(-)$ voltage applied) by forcing a voltage to the $_{IN}(+)$ input which is given by:

$$V_{IN}(+)\text{ fs adj} = V_{MAX} - 1.5\left[\frac{(V_{MAX} - V_{MIN})}{256}\right],$$

here:

V_{MAX} = The high end of the analog input range

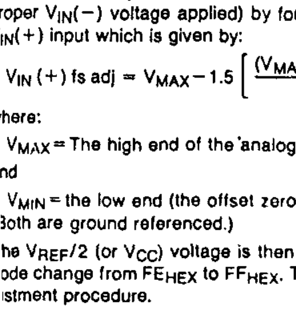
nd

V_{MIN} = the low end (the offset zero) of the analog range. 3oth are ground referenced.)

he $V_{REF}/2$ (or V_{CC}) voltage is then adjusted to provide a ode change from FE_{HEX} to FF_{HEX}. This completes the ad- istment procedure.

.6 Clocking Option

he clock for the A/D can be derived from the CPU clock or n external RC can be added to provide self-clocking. The LK IN (pin 4) makes use of a Schmitt trigger as shown in *igure 6.*



$$f_{CLK} \approx \frac{1}{1.1\,RC}$$

$R \approx 10\ k\Omega$

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FIGURE 6. Self-Clocking the A/D

eavy capacitive or DC loading of the clock R pin should be 'oided as this will disturb normal converter operation. ads less than 50 pF, such as driving up to 7 A/D convert- clock inputs from a single clock R pin of 1 converter, are owed. For larger clock line loading, a CMOS or low power 'L buffer or PNP input logic should be used to minimize e loading on the clock R pin (do not use a standard TTL Iffer).

7 Restart During a Conversion

the A/D is restarted ($\overline{CS}$ and $\overline{WR}$ go low and return high) ıring a conversion, the converter is reset and a new con- rsion is started. The output data latch is not updated if the conversion in process is not allowed to be completed, there- fore the data of the previous conversion remains in this latch. The $\overline{INTR}$ output simply remains at the "1" level.

2.8 Continuous Conversions

For operation in the free-running mode an initializing pulse should be used, following power-up, to ensure circuit opera- tion. In this application, the $\overline{CS}$ input is grounded and the $\overline{WR}$ input is tied to the $\overline{INTR}$ output. This $\overline{WR}$ and $\overline{INTR}$ node should be momentarily forced to logic low following a power-up cycle to guarantee operation.

2.9 Driving the Data Bus

This MOS A/D, like MOS microprocessors and memories, will require a bus driver when the total capacitance of the data bus gets large. Other circuitry, which is tied to the data bus, will add to the total capacitive loading, even in TRI-STATE (high impedance mode). Backplane bussing also greatly adds to the stray capacitance of the data bus.

There are some alternatives available to the designer to handle this problem. Basically, the capacitive loading of the data bus slows down the response time, even though DC specifications are still met. For systems operating with a relatively slow CPU clock frequency, more time is available in which to establish proper logic levels on the bus and therefore higher capacitive loads can be driven (see typical characteristics curves).

At higher CPU clock frequencies time can be extended for I/O reads (and/or writes) by inserting wait states (8080) or using clock extending circuits (6800).

Finally, if time is short and capacitive loading is high, exter- nal bus drivers must be used. These can be TRI-STATE buffers (low power Schottky such as the DM74LS240 series is recommended) or special higher drive current products which are designed as bus drivers. High current bipolar bus drivers with PNP inputs are recommended.

2.10 Power Supplies

Noise spikes on the V_{CC} supply line can cause conversion errors as the comparator will respond to this noise. A low inductance tantalum filter capacitor should be used close to the converter V_{CC} pin and values of 1 μF or greater are recommended. If an unregulated voltage is available in the system, a separate LM340LAZ-5.0, TO-92, 5V voltage regu- lator for the converter (and other analog circuitry) will greatly reduce digital noise on the V_{CC} supply.

2.11 Wiring and Hook-Up Precautions

Standard digital wire wrap sockets are not satisfactory for breadboarding this A/D converter. Sockets on PC boards can be used and all logic signal wires and leads should be grouped and kept as far away as possible from the analog signal leads. Exposed leads to the analog inputs can cause undesired digital noise and hum pickup, therefore shielded leads may be necessary in many applications.

Functional Description (Continued)

A single point analog ground that is separate from the logic ground points should be used. The power supply bypass capacitor and the self-clocking capacitor (if used) should both be returned to digital ground. Any $V_{REF}/2$ bypass capacitors, analog input filter capacitors, or input signal shielding should be returned to the analog ground point. A test for proper grounding is to measure the zero error of the A/D converter. Zero errors in excess of ¼ LSB can usually be traced to improper board layout and wiring (see section 2.5.1 for measuring the zero error).

3.0 TESTING THE A/D CONVERTER

There are many degrees of complexity associated with testing an A/D converter. One of the simplest tests is to apply a known analog input voltage to the converter and use LEDs to display the resulting digital output code as shown in *Figure 7*.

For ease of testing, the $V_{REF}/2$ (pin 9) should be supplied with 2.560 V_{DC} and a V_{CC} supply voltage of 5.12 V_{DC} should be used. This provides an LSB value of 20 mV.

If a full-scale adjustment is to be made, an analog input voltage of 5.090 V_{DC} (5.120−1½ LSB) should be applied to the $V_{IN}(+)$ pin with the $V_{IN}(-)$ pin grounded. The value of the $V_{REF}/2$ input voltage should then be adjusted until the digital output code is just changing from 1111 1110 to 1111 1111. This value of $V_{REF}/2$ should then be used for all the tests.

The digital output LED display can be decoded by dividing the 8 bits into 2 hex characters, the 4 most significant (MS) and the 4 least significant (LS). Table I shows the fractional binary equivalent of these two 4-bit groups. By adding the voltages obtained from the "VMS" and "VLS" columns in Table I, the nominal value of the digital display (when $V_{REF}/2$ = 2.560V) can be determined. For example, for an output LED display of 1011 0110 or B6 (in hex), the voltage values from the table are 3.520 + 0.120 or 3.640 V_{DC}. These voltage values represent the center-values of a perfect A/D converter. The effects of quantization error have to be accounted for in the interpretation of the test results.

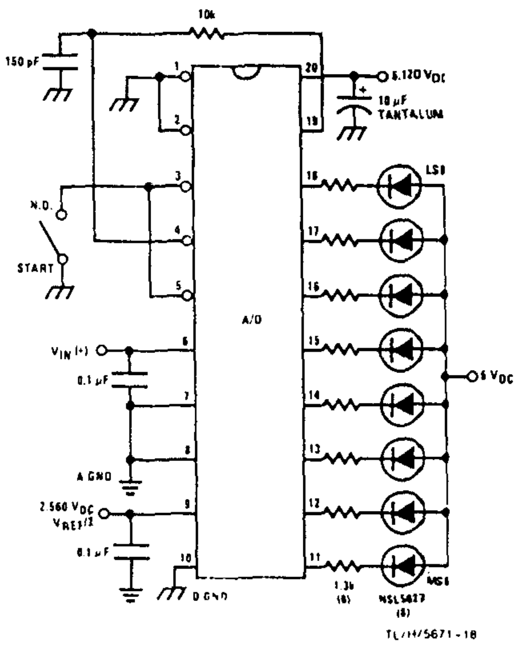

FIGURE 7. Basic A/D Tester

For a higher speed test system, or to obtain plotted data, a digital-to-analog converter is needed for the test set-up. An accurate 10-bit DAC can serve as the precision voltage source for the A/D. Errors of the A/D under test can be expressed as either analog voltages or differences in 2 digital words.

A basic A/D tester that uses a DAC and provides the error as an analog output voltage is shown in *Figure 8*. The 2 op amps can be eliminated if a lab DVM with a numerical subtraction feature is available to read the difference voltage, "A−C", directly. The analog input voltage can be supplied by a low frequency ramp generator and an X-Y plotter can be used to provide analog error (Y axis) versus analog input (X axis). The construction details of a tester of this type are provided in the NSC application note AN-179, "Analog-to-Digital Converter Testing".

For operation with a microprocessor or a computer-based test system, it is more convenient to present the errors digitally. This can be done with the circuit of *Figure 9*, where the output code transitions can be detected as the 10-bit DAC is incremented. This provides ¼ LSB steps for the 8-bit A/D under test. If the results of this test are automatically plotted with the analog input on the X axis and the error (in LSB's) as the Y axis, a useful transfer function of the A/D under test results. For acceptance testing, the plot is not necessary and the testing speed can be increased by establishing internal limits on the allowed error for each code.

4.0 MICROPROCESSOR INTERFACING

To dicuss the interface with 8080A and 6800 microprocessors, a common sample subroutine structure is used. The microprocessor starts the A/D, reads and stores the results of 16 successive conversions, then returns to the user's program. The 16 data bytes are stored in 16 successive memory locations. All Data and Addresses will be given in hexadecimal form. Software and hardware details are provided separately for each type of microprocessor.

4.1 Interfacing 8080 Microprocessor Derivatives (8048, 8085)

This converter has been designed to directly interface with derivatives of the 8080 microprocessor. The A/D can be mapped into memory space (using standard memory address decoding for $\overline{CS}$ and the $\overline{MEMR}$ and $\overline{MEMW}$ strobes) or it can be controlled as an I/O device by using the $\overline{I/O\ R}$ and $\overline{I/O\ W}$ strobes and decoding the address bits A0 → A7 (or address bits A8 → A15 as they will contain the same 8-bit address information) to obtain the $\overline{CS}$ input. Using the I/O space provides 256 additional addresses and may allow a simpler 8-bit address decoder but the data can only be input to the accumulator. To make use of the additional memory reference instructions, the A/D should be mapped into memory space. An example of an A/D in I/O space is shown in *Figure 10*.

Functional Description (Continued)

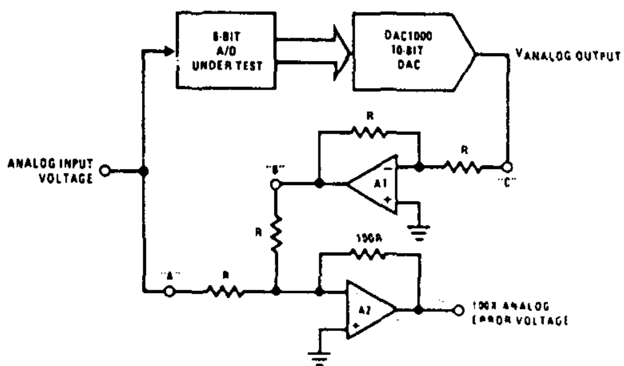

FIGURE 8. A/D Tester with Analog Error Output

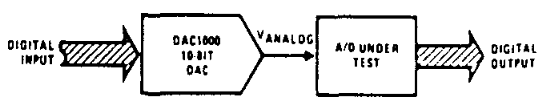

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FIGURE 9. Basic "Digital" A/D Tester

TABLE I. DECODING THE DIGITAL OUTPUT LEDs

HEX	BINARY				FRACTIONAL BINARY VALUE FOR		OUTPUT VOLTAGE CENTER VALUES WITH $V_{REF}/2 = 2.560\ V_{DC}$	
					MS GROUP	LS GROUP	VMS GROUP*	VLS GROUP*
F	1	1	1	1	15/16	15/256	4.800	0.300
E	1	1	1	0	7/8	7/128	4.480	0.280
D	1	1	0	1	13/16	13/256	4.160	0.260
C	1	1	0	0	3/4	3/64	3.840	0.240
B	1	0	1	1	11/16	11/256	3.520	0.220
A	1	0	1	0	5/8	5/128	3.200	0.200
9	1	0	0	1	9/16	9/256	2/880	0.180
8	1	0	0	0	1/2	1/32	2/560	0.160
7	0	1	1	1	7/16	7/256	2.240	0.140
6	0	1	1	0	3/8	3/128	1.920	0.120
5	0	1	0	1	5/16	2/256	1.600	0.100
4	0	1	0	0	1/4	1/64	1/280	0.080
3	0	0	1	1	3/16	3/256	0.960	0.060
2	0	0	1	0	1/8	1/128	0.640	0.040
1	0	0	0	1	1/16	1/256	0.320	0.020
0	0	0	0	0			0	0

*Display Output = VMS Group + VLS Group

3

LAMPIRAN 6

DATA BOOK IC TL074

Texas Instruments **IC LINIER**

TL 074, TL 084, TL 074A, TL 084A, TL 074B, TL 084B
Penguat Operasi dengan Jalanmasuk JFET
(JFET-input Operational Amplifiers)

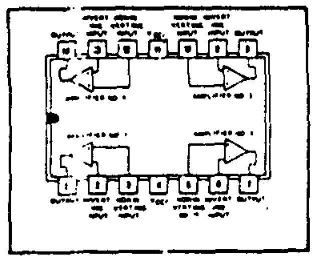
Penjelasan TL 074

Penguat operasi dengan jalanmasuk JFET dari seri TL 074 sudah dirancang sebagai versi penguat seri TL 084 yang berdesah-rendah yang disertai panjaran masukan rendah dan laju lantingan cepat. Karena cacat harmonisa yang kecil dan juga desah yang rendah, maka seri TL 074 adalah cocok sebagai penguat yang setiatinggi *(high-fidelity)* dan dalam penerapan penguat depan audio. Masing-masing penguat memiliki jalanmasuk JFET (guna memperoleh impedansi masukan tinggi) yang dikopelkan kepada tingkat keluaran duakutub *(bipolar)*; kesemuanya terintegrasi dalam satu *chip* monolit.

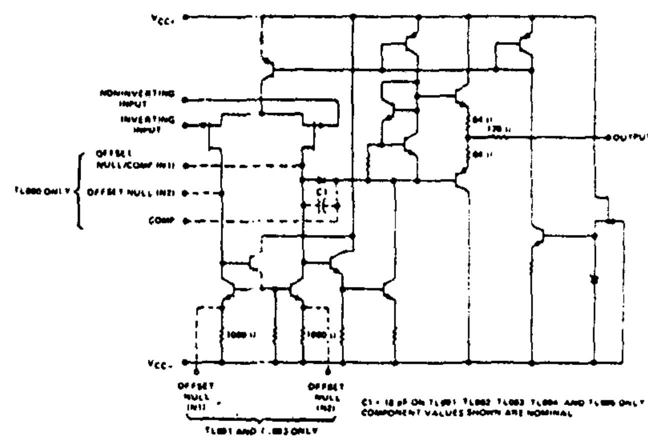
Penjelasan TL 084

Rumpun penguat operasi dengan jalanmasuk JFET

Kemasan .jeris-berdua (DIL) J atau N kemasan pipih W (Tampak atas)



Skema (tiap penguat)



Tarif Maksimum mutlak pengoperasian dalam jelajahan suhu udara-bebas Satuan

	TL 074C TL 084M	TL 074I TL 084I	TL 074C /TL 084C TL 074AC /TL 084AC TL 074BC /TL 084BC	UNIT
Tegangan catu, V_{CC+}	18	18	18	V
Tegangan catu, V_{CC-}	−18	−18	−18	V
Tegangan masukan diferensial	± 30	± 30	± 30	V
Tegangan masukan	± 15	± 15	± 15	V
Lama hubungsingkat keluaran	tak terbatas	tak terbatas	tak t[illegible]batas	
Borosan total terus-menerus pada (atau di bawah) suhu udara-bebas 25° C	680	680	6[illegible]0	mW
Jelajahan suhu udara-bebas operasi	−55 s/d 125	−25 s/d 85	0 s/d 70	°C
Jelajahan suhu simpan	−65 s/d 150	−65 s/d 150	−65 s/d 150	°C
Jelajahan suhu timah dalam jarak 1/16 inci (1,6 mm) dari kemasan selama 60 detik Kemasan J atau JG	300	300	30[illegible]	°C
Suhu timah dalam jarak 1/16 inci (1,6 mm) dari kemasan selama 10 detik Kemasan N atau P		260	2[illegible]	°C

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