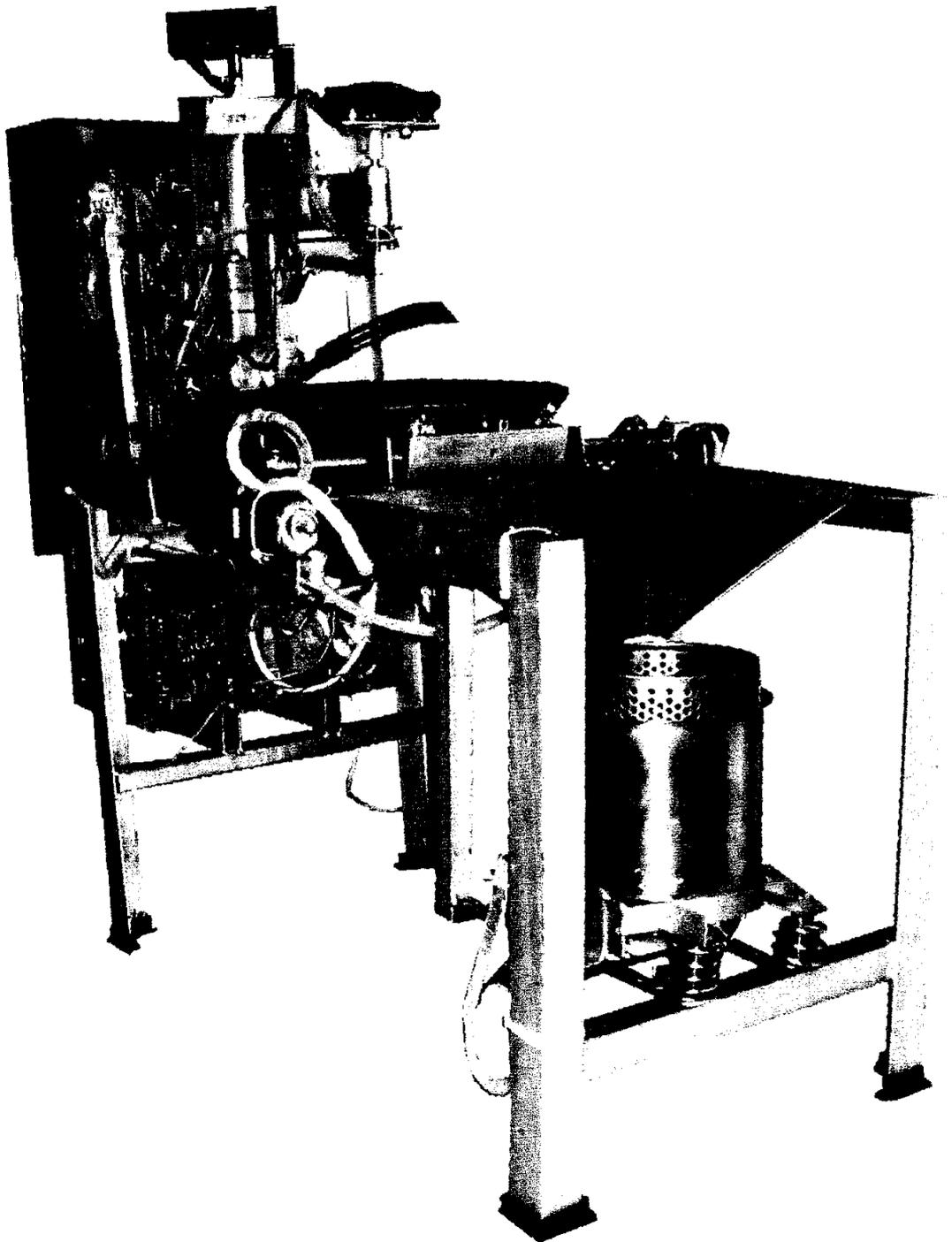


**LAMPIRAN**

# LAMPIRAN A

## Gambar Alat



## LAMPIRAN C

### LISTING MIKROKONTROLLER

```
#include<stdio.h>
#include<regx51.h>
sbit DQ = P0_4;
sfr ldata = 0x90;
sbit rs = P3_0;
sbit en = P3_1;
unsigned int suhu;
char a;
int b,c,d,e,f;

void delay(int useconds)
{
int s;
for (s=0; s<useconds;s++);
}
unsigned char ow_reset(void)
{
unsigned char presence;
DQ = 0; //pull DQ line low
delay(29); // leave it low for 4801s
DQ = 1; // allow line to return high
delay(3); // wait for presence
presence = DQ; // get presence signal
delay(25); // wait for end of timeslot
return(presence); // presence signal returned
} // 0=presence, 1 = no part
unsigned char read_bit(void)
{
unsigned char i;
DQ = 0; // pull DQ low to start timeslot
DQ = 1; // then return high
for (i=0; i<3; i++); // delay 151s from start of timeslot
return(DQ); // return value of DQ line
}
void write_bit(char bitval)
{
DQ = 0; // pull DQ low to start timeslot
if(bitval==1) DQ =1; // return DQ high if write 1
delay(5); // hold value for remainder of timeslot
DQ = 1;
}
unsigned char read_byte(void)
{
unsigned char i;
unsigned char value = 0;
for (i=0;i<8;i++)
{
if(read_bit()) value|=0x01<<i; // reads byte in, one bit at a time and then
// shifts it left
delay(6); // wait for rest of timeslot
}
return(value);
}
void write_byte(char val)
{
unsigned char i;
unsigned char temp;
for (i=0; i<8; i++) // writes byte, one bit at a time
{
temp = val>>i; // shifts val right 'i' spaces
temp &= 0x01; // copy that bit to temp
write_bit(temp); // write bit in temp into
}
}
```

```

delay(5);
}
void MSDelay(unsigned int itime)
{
    unsigned int i, j;
    for(i=0;i<itime;i++)
        for(j=0;j<1275;j++);
}
void lcddata(unsigned char value)
{ldata = value;
rs = 1;
en = 1;
MSDelay(20);
en = 0;
return;
}

void tampilkan_ke_lcd(char *tulisan)
{
    char hitung_tulisan;
    while (hitung_tulisan=*tulisan++)
        {
            lcddata(hitung_tulisan);
        };
}

unsigned char Read_Current (void)
{
    int lsb, msb, temp, nilai;
    float Current; //This value may be declared globally
    if(ow_reset()==0) //If a presence is detected, continue to read
    {
        write_byte(0xCC); // Skip Net Address Command
        write_byte(0x69); // Read Registers Command
        write_byte(0x0E); //Current Register Address
        msb = read_byte(); // Read msb
        lsb = read_byte() & 0xF8; // Read lsb and mask off lower 3 bits

        suhu = 256*msb + lsb;
        suhu = 65535 - suhu;
        suhu = suhu/4;
        nilai = suhu*(-0.2215)+3698.8;
        if (nilai >100 & nilai < 200)
        {nilai=nilai-20;}
        if (nilai < 100)
        {nilai=nilai-40;}

        lcddata(nilai/100 %10 + 0x30);
        lcddata(nilai/10 %10 + 0x30);
        lcddata(nilai %10 + 0x30);
        lcddata(0xDF);
        lcddata('C');

        return(0); //Return 0 if no error
    }
    return(1); //Return 1 if no presence detected
}

void motor_putar()
{P3_7 = 1;
}

void motor_aduk()
{P2_4 = 1;
P2_5 = 1;
}

void motor_wajan()
{P2_2 = 1;// on
P2_3 = 1;//balik
}

void pemanasl()
{P2_6 = 1;
}

```

```

P2_7 = 1;
}
void pemanas2()
{P2_6 = 0;
P2_7 = 0;
}
void posisi()//akuuuu
{satu:
if (P0_5 == 0)
P2_4 = 0;
else
goto satu;
dua:
MSDelay(1000);
if (P0_6 == 0)
P2_5 = 0;
else
goto dua;
}
void lcdcmd(unsigned char value)
{
ldata = value;
rs = 0;
en = 1;
MSDelay(20);
en = 0;
return;
}
void wajan_naik()
{lcdcmd(0x01);
tampilkan_ke_lcd("penirisan");
MSDelay(1000);
P2_1 = 1; //motor atas
MSDelay(100);
P2_1 = 0;
MSDelay(200);
P2_1 = 1;
MSDelay(1000);
P2_1 = 0;
MSDelay(1000);
//motor wajan
P2_3 = 1;
while(P0_3 != 0);
P2_2 = 1;
MSDelay(50);
P2 = 0x00;
}
void wajan_turun()
{P2 = 0x0C;
MSDelay(100);
P2 = 0x00;
MSDelay(2000);//motor wajan
P2_1 = 1;
P2_0 = 1;
MSDelay(100);
P2 = 0x00;
MSDelay(100);
P2 = 0x03;
MSDelay(200);//motor atas
P2 = 0x00;
}

void init_lcd()
{lcdcmd(0x038);
MSDelay(20);
lcdcmd(0x0C);
MSDelay(20);
lcdcmd(0x06);
MSDelay(20);
lcdcmd(0x01);
}

```

```

MSDelay(20);
}
void mulai()
{
pemanas1();
a = 0;
while(P0_3 != 0)
{P3_2 = 0;
if (P0_3 !=0)
MSDelay(500);
P3_2 = 1;
if (P0_3 !=0)
{MSDelay(500);}
a++;
if (a>10)
break;
}

if (a>=10)
{P3_2 = 0;
while (P0_3 != 0)
{
if (P0_3 !=0)
MSDelay(1000);
if (suhu < 15597)
pemanas2();
else
pemanas1();
}
}
}
lcdcmd(0x01);
pemanas1();
P3_2 = 1;
lcdcmd(0x01);
tampilkan_ke_lcd("tunggu suhu");
lcdcmd(0xC4);
read_current();
while(suhu > 14687)
{lcdcmd(0xC4);
read_current();
MSDelay(1000);
}
}
void daging()
{
lcdcmd(0x01);
tampilkan_ke_lcd("masukkan");
lcdcmd(0xC0);
tampilkan_ke_lcd("daging + bumbu");
a = 0;
while(P0_3 != 0)
{P3_2 = 0;
if (P0_3 !=0)
MSDelay(500);
P3_2 = 1;
if (P0_3 !=0)
MSDelay(1000);
a++;
if (a>10)
break;
}
if (a>=10)
{P3_2 = 0;
while (P0_3 != 0);
}
P3_2 = 1;
lcdcmd(0x01);
}
void daging_bumbu()
{

```

```

lcdcmd(0x01);
tampilkan_ke_lcd("masukkan");
lcdcmd(0xC0);
tampilkan_ke_lcd("daging berbumbu");
MSDelay(1000);
a = 0;
while(P0_3 != 0)
{
P3_2 = 0;
if (P0_3 !=0)
MSDelay(500);
P3_2 = 1;
if (P0_3 !=0)
MSDelay(1000);
a++;
if (a>10)
break;
}
if (a>=10)
{
P3_2 = 0;
while (P0_3 != 0);
}
P3_2 = 1;
lcdcmd(0x01);
}
void waktu()
{
c = 0;
tampilkan_ke_lcd("sisa ");
if (b != f)
motor_aduk();
while (b != 0)
{
if (b == d)
posisi();
if (b == e)
motor_aduk();
lcdcmd(0x85);
lcddata(b/10 %10 + 0x30);
lcddata(b %10 + 0x30);
tampilkan_ke_lcd(" menit");
c = 0;
while (c <= 173)
{
lcdcmd(0xc4);
read_current();
MSDelay(10);
c++;
}
}
b--;
}
}
void waktu_kering()
{
c = 0;
while (b != 0)
{
c = 0;
while (c <= 233)
{
MSDelay(100);
c++;
}
}
b--;
}
}
void main(void)
{
P3 = 0x04;
P1 = 0x00;
P2 = 0x00;
P0 = 0xff;
init_lcd();
lcdcmd(0x01);
lcdcmd(0x84);
tampilkan_ke_lcd("wibisono");
lcdcmd(0xC3);
}

```

```

tampilkan_ke_lcd("5103003007");
while(P0_3 != 0);
lcdcmd(0x01);
tampilkan_ke_lcd("tombol 1 = 100g");
lcdcmd(0xc0);
tampilkan_ke_lcd("tombol 2 = 250g");
while(1)
{ if (P0_0 == 0)
{lcdcmd(0x01);
tampilkan_ke_lcd("masukkan minyak");
lcdcmd(0xc0);
tampilkan_ke_lcd("2 sendok makan");
mulai();
daging();
b=10;
d=5;
e=25;
f=25;
waktu();
pemanas2();
wajan_naik();
MSDelay(500);
wajan_turun();
motor_putar();
b=3;
waktu_kering();
P3_7 = 0;//goreng
pemanas1();
lcdcmd(0x01);
tampilkan_ke_lcd("masukkan minyak");
lcdcmd(0xc0);
tampilkan_ke_lcd("200 ml");
mulai();
daging_bumbu();
b=20;
d=5;
e=15;
f=20;
waktu();
pemanas2();
wajan_naik();
MSDelay(500);
wajan_turun();
motor_putar();
b=3;
waktu_kering();
P3_7 = 0;
lcdcmd(0x01);
tampilkan_ke_lcd("selesai!!!!");
while(P0_3 != 0)
{P3_2 = 0;
if (P0_3 !=0)
MSDelay(500);
P3_2 = 1;
if (P0_3 !=0)
MSDelay(1000);
}
lcdcmd(0x01);
lcdcmd(0x80);
tampilkan_ke_lcd("tombol 1 = 100g");
lcdcmd(0xc0);
tampilkan_ke_lcd("tombol 2 = 250g");
}
else
if (P0_1 == 0)
{lcdcmd(0x01);
tampilkan_ke_lcd("masukkan minyak");
lcdcmd(0xc0);
tampilkan_ke_lcd("2 sendok makan");
mulai();

```

```

daging();
b=10;
d=5;
e=25;
f=15;
waktu();
pemanas2();
wajan_naik();
MSDelay(500);
wajan_turun();
motor_putar();
b=3;
waktu_kering();
P3_7 = 0;//goreng
pemanas1();
lcdcmd(0x01);
tampilkan_ke_lcd("masukkan minyak");
lcdcmd(0xc0);
tampilkan_ke_lcd("300 ml");
mulai();
daging_bumbu();
b=30;
d=10;
e=20;
f=30;
waktu();
pemanas2();
wajan_naik();
MSDelay(500);
wajan_turun();
motor_putar();
b=3;
waktu_kering();
P3_7 = 0;
lcdcmd(0x01);
tampilkan_ke_lcd("selesai!!!!");
while(P0_3 != 0)
{
P3_2 = 0;
if (P0_3 !=0)
MSDelay(500);
P3_2 = 1;
if (P0_3 !=0)
MSDelay(1000);
}
lcdcmd(0x01);
lcdcmd(0x80);
tampilkan_ke_lcd("tombol 1 = 100g");
lcdcmd(0xc0);
tampilkan_ke_lcd("tombol 2 = 250g");
}
//motor_aduk();
}
}

```

## LAMPIRAN D

### DATA PENGAMBILAN SAMPEL

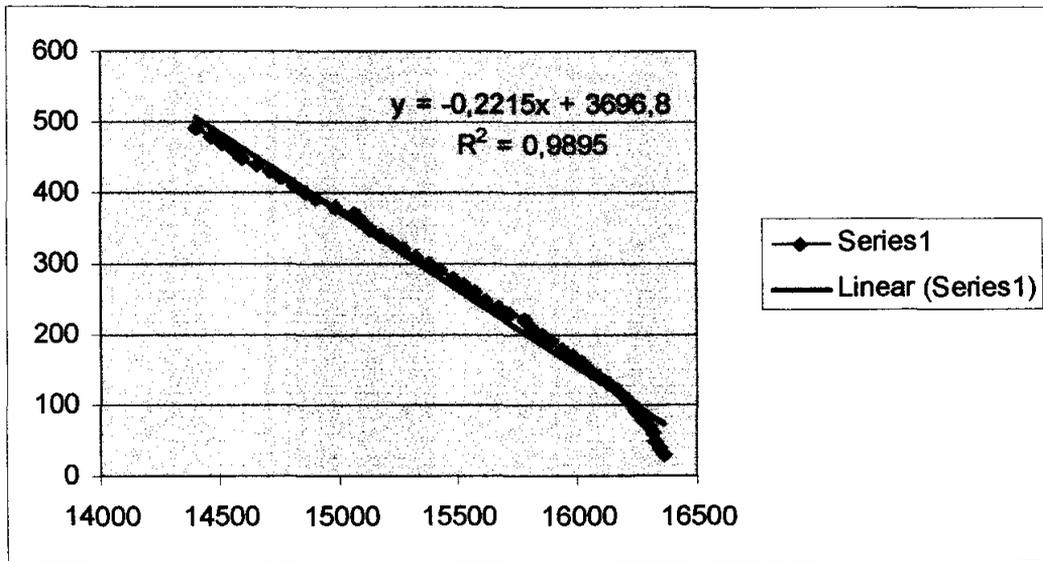
Tabel Sampel

DS2760	Multimeter UNI-T Type UT720B	Hasil dari persamaan Y	Selisih
16365	30	71,9525	41,9525
16347	40	75,9395	35,9395
16331	50	79,4835	29,4835
16313	60	83,4705	23,4705
16295	70	87,4575	17,4575
16273	80	92,3305	12,3305
16249	90	97,6465	7,6465
16225	100	102,9625	2,9625
16195	110	109,6075	-0,3925
16159	120	117,5815	-2,4185
16129	130	124,2265	-5,7735
16091	140	132,6435	-7,3565
16051	150	141,5035	-8,4965
16013	160	149,9205	-10,0795
15979	170	157,4515	-12,5485
15933	180	167,6405	-12,3595
15891	190	176,9435	-13,0565
15849	200	186,2465	-13,7535
15803	210	196,4355	-13,5645
15775	220	202,6375	-17,3625
15715	230	215,9275	-14,0725
15667	240	226,5595	-13,4405
15613	250	238,5205	-11,4795
15567	260	248,7095	-11,2905
15523	270	258,4555	-11,5445
15475	280	269,0875	-10,9125
15423	290	280,6055	-9,3945
15377	300	290,7945	-9,2055
15327	310	301,8695	-8,1305
15265	320	315,6025	-4,3975
15225	330	324,4625	-5,5375
15181	340	334,2085	-5,7915
15129	350	345,7265	-4,2735
15091	360	354,1435	-5,8565
15065	370	359,9025	-10,0975
14981	380	378,5085	-1,4915
14901	390	396,2285	6,2285
14861	400	405,0885	5,0885
14811	410	416,1635	6,1635
14761	420	427,2385	7,2385

**Tabel Sampel (lanjutan)**

DS2760	Multimeter UNI-T Type UT720B	Hasil dari persamaan Y	Selisih
14711	430	438,3135	8,3135
14657	440	450,2745	10,2745
14597	450	463,5645	13,5645
14561	460	471,5385	11,5385
14509	470	483,0565	13,0565
14461	480	493,6885	13,6885
14403	490	506,5355	16,5355

**Grafik dari pengambilan sampel**



## BIODATA



Nama : Wibisono

NRP : 5103003007

Tempat/ Tgl. Lahir : Surabaya / 1 April 1982

Agama : Katholik

Alamat Rumah : Jl. Tarmidi 52

Samarinda – Kalimantan Timur

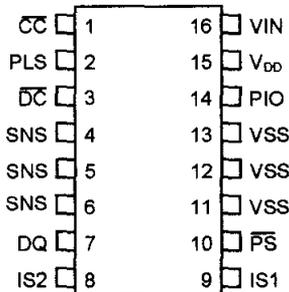
### **Riwayat Pendidikan :**

- Tahun 1988, Lulus TK Kristus Radja Surabaya.
- Tahun 1996, Lulus SD Swasta Megawati Surabaya.
- Tahun 1999, Lulus SLTP Katholik Santa Agnes Surabaya.
- Tahun 2003, Lulus SMK Katholik St. Louis Surabaya.
- Tahun 2003 hingga buku ini ditulis, tercatat sebagai mahasiswa di Jurusan Teknik Elektro, Fakultas Teknik, Universitas Katolik Widya Mandala, Surabaya.

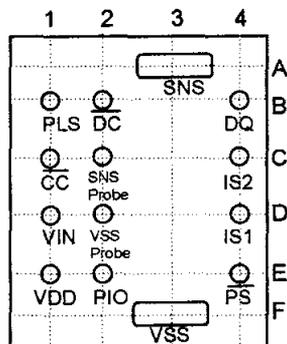
**FEATURES**

- + safety circuit
- Overvoltage protection
- Overcurrent/short circuit protection
- Undervoltage protection
- Zero Volt Battery Recovery Charge available in two configurations:
- Internal 25mΩ sense resistor
- External user-selectable sense resistor
- Current measurement
- 12-bit bidirectional measurement
- Internal sense resistor configuration: 0.625mA LSB and ±1.9A dynamic range
- External sense resistor configuration: 15.625μV LSB and ±64mV dynamic range
- Current accumulation
- Internal sense resistor: 0.25mAh LSB
- External sense resistor: 6.25μVhr LSB
- Voltage measurement with 4.88mV resolution
- Temperature measurement using integrated sensor with 0.125°C resolution
- System power management and control feature support
- 2 bytes of lockable EEPROM
- 5 bytes of general purpose SRAM
- Dallas 1-Wire® interface with unique 64-bit device address
- Low power consumption:
  - Active current: 90μA max
  - Sleep current: 2μA max

**PIN ASSIGNMENT**



DS2760  
16-Pin TSSOP Package



DS2760  
Flip-Chip Packaging  
Top View

**PIN DESCRIPTION**

- CC - Charge control output
- DC - Discharge control output
- DQ - Data input/output
- PIO - Programmable I/O pin
- PLS - Battery pack positive terminal input
- PS - Power switch sense input
- VIN - Voltage sense input
- VDD - Power supply input (2.5V to 5.5V)
- VSS - Device ground
- SNS - Sense resistor connection
- IS1 - Current sense input
- IS2 - Current sense input
- SNS Probe - Do not connect
- VSS Probe - Do not connect

is a registered trademark of Dallas Semiconductor.

**ORDERING INFORMATION**

Part	Marking	Description
50AE+	DS2760A	TSSOP, External Sense Resistor, 4.275V Vov, Lead-Free
50BE+	DS2760B	TSSOP, External Sense Resistor, 4.35V Vov, Lead-Free
50AE+T&R	DS2760A	DS2760AE+ on Tape & Reel, Lead-Free
50BE+T&R	DS2760B	DS2760BE+ on Tape & Reel, Lead-Free
60AE+025	2760A25	TSSOP, 25mΩ Sense Resistor, 4.275V Vov, Lead-Free
60BE+025	2760B25	TSSOP, 25mΩ Sense Resistor, 4.35V Vov, Lead-Free
60AE+025/T&R	2760A25	DS2760AE+025 in Tape & Reel, Lead-Free
60BE+025/T&R	2760B25	DS2760BE+025 in Tape & Reel, Lead-Free
60AX	DS2760A	Flipchip, External Sense Resistor, Tape & Reel, 4.275V Vov
60BX	DS2760B	Flipchip, External Sense Resistor, Tape & Reel, 4.35V Vov
60AX-025	DS2760AR	Flipchip, 25mΩ Sense Resistor, Tape & Reel, 4.275V Vov
60BX-025	DS2760BR	Flipchip, 25mΩ Sense Resistor, Tape & Reel, 4.35V Vov
60AE	DS2760A	TSSOP, External Sense Resistor, 4.275V Vov
60BE	DS2760B	TSSOP, External Sense Resistor, 4.35V Vov
60AE/T&R	DS2760A	DS2760AE on Tape & Reel
60BE/T&R	DS2760B	DS2760BE on Tape & Reel
60AE-025	2760A25	TSSOP, 25mΩ Sense Resistor, 4.275V Vov
60BE-025	2760B25	TSSOP, 25mΩ Sense Resistor, 4.35V Vov
60AE-025/T&R	2760A25	DS2760AE-025 in Tape & Reel
60BE-025/T&R	2760B25	DS2760BE-025 in Tape & Reel

**DESCRIPTION**

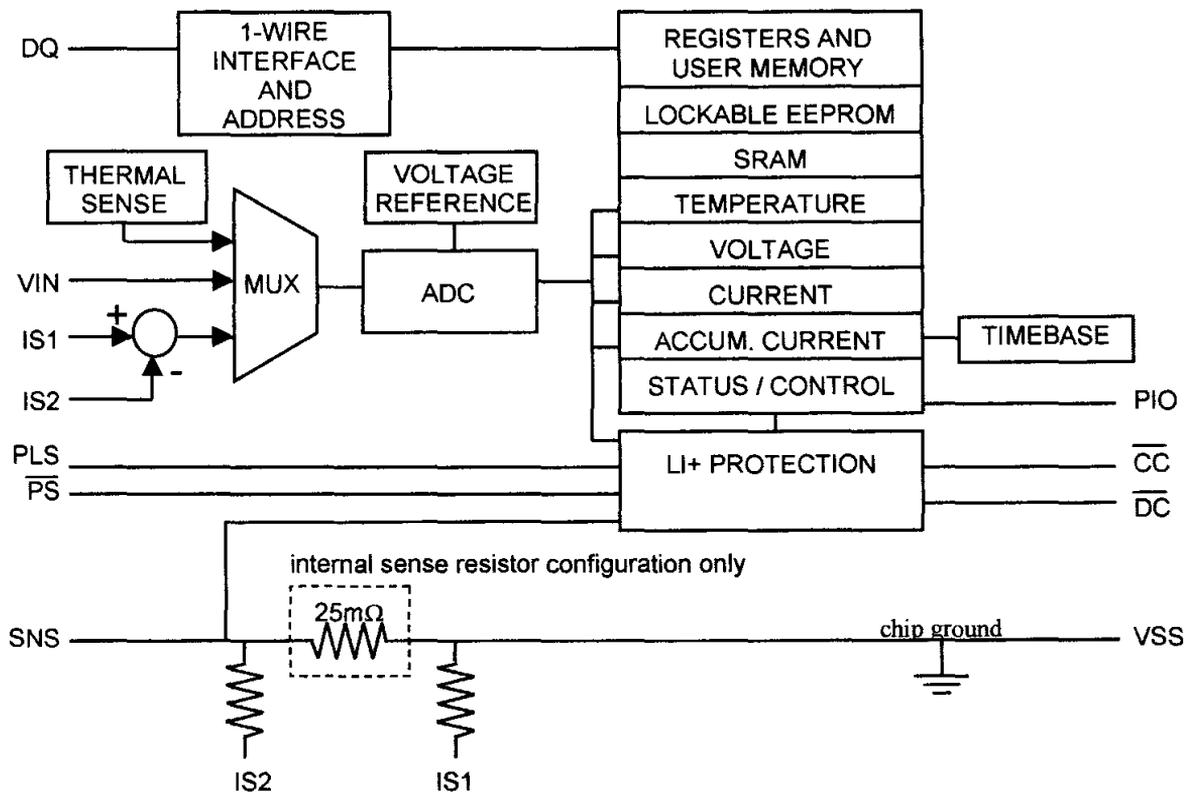
DS2760 High-Precision Li+ Battery Monitor is a data acquisition, information storage, and safety protection device tailored for cost-sensitive battery pack applications. This low-power device integrates precise temperature, voltage, and current measurement, nonvolatile data storage, and Li+ protection into a small footprint of either a TSSOP package or flip chip. The DS2760 is a key component in applications including remaining capacity estimation, safety monitoring, and battery-specific data storage.

With its 1-Wire interface, the DS2760 gives the host system read/write access to status and control registers, instrumentation registers, and general purpose data storage. Each device has a unique factory-programmed 64-bit net address which allows it to be individually addressed by the host system, supporting multi-battery operation.

DS2760 is capable of performing temperature, voltage and current measurement to a resolution sufficient to support process monitoring applications such as battery charge control, remaining capacity estimation, and safety monitoring. Temperature is measured using an on-chip sensor, eliminating the need for a separate thermistor. Bidirectional current measurement and accumulation are accomplished using either an internal 25mΩ sense resistor or an external device. The DS2760 also features a programmable I<sup>2</sup>C interface that allows the host system to sense and control other electronics in the pack, including switches, relays, solenoid motors, speakers and LEDs.

Three types of memory are provided on the DS2760 for battery information storage: EEPROM, lockable EEPROM and SRAM. EEPROM memory saves important battery data in true nonvolatile memory that is not affected by severe battery depletion, accidental shorts or ESD events. Lockable EEPROM becomes read-only when locked to provide additional security for unchanging battery data. SRAM provides fast, nonvolatile storage for temporary data.

CK DIAGRAM Figure 1



BATTERY-ENABLED PIN DESCRIPTION Table 1

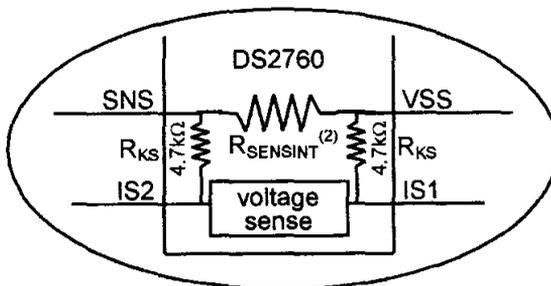
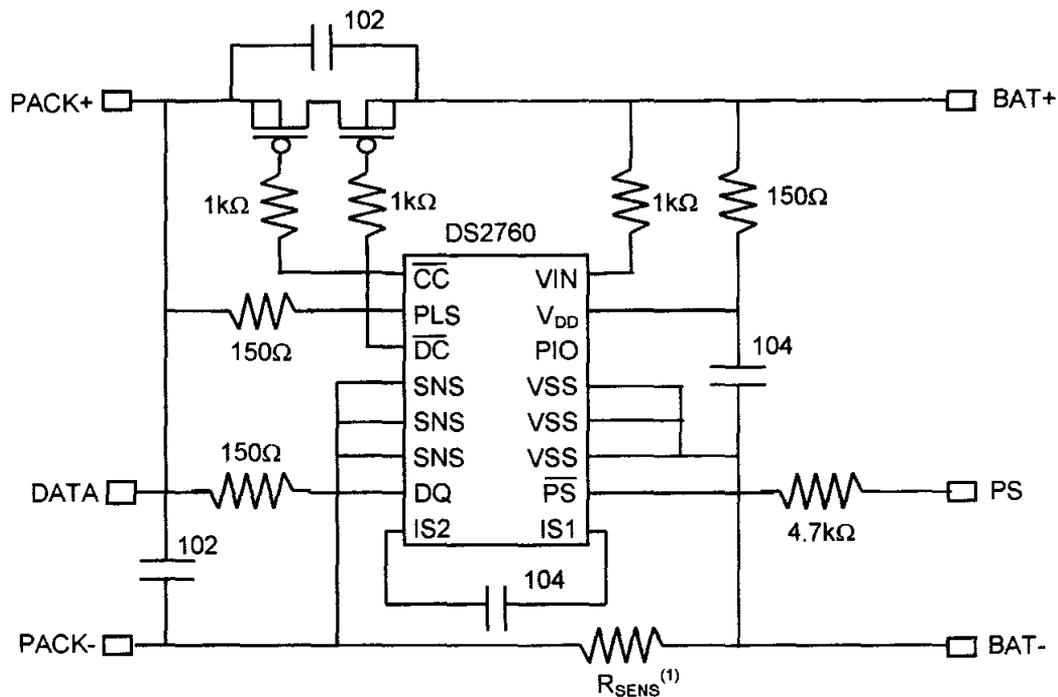
IBOL	TSSOP*	FLIP CHIP*	DESCRIPTION
$\overline{C}$	1	C1	<b>Charge Protection Control Output.</b> Controls an external p-channel high-side charge protection FET.
$\overline{D}$	3	B2	<b>Discharge Protection Control Output.</b> Controls an external p-channel high-side discharge protection FET.
Q	7	B4	<b>Data Input/Out.</b> 1-Wire data line. Open-drain output driver. Connect this pin to the DATA terminal of the battery pack. Pin has an internal 1 $\mu$ A pull-down for sensing disconnection.
IO	14	E2	<b>Programmable I/O Pin.</b> Used to control and monitor user-defined external circuitry. Open drain to VSS.
PLS	2	B1	<b>Battery Pack Positive Terminal Input.</b> The device monitors the state of the battery pack's positive terminal through this pin in order to detect events such as the attachment of a charger or the removal of a short circuit. Additionally, a charge path to recover a deeply depleted cell is provided from PLS to VDD.
$\overline{PS}$	10	E4	<b>Power Switch Sense Input.</b> The device wakes up from Sleep Mode when it senses the closure of a switch to VSS on this pin. Pin has an internal 1 $\mu$ A pull-up to VDD.
VIN	16	D1	<b>Voltage Sense Input.</b> The voltage of the Li+ cell is monitored via this input pin. This pin has a weak pullup to VDD.
VDD	15	E1	<b>Power Supply Input.</b> Connect to the positive terminal of the Li+ cell through a decoupling network.
VSS	11,12,13	F3	<b>Device Ground.</b> Connect directly to the negative terminal of the Li+ cell. For the external sense resistor configuration, connect the sense resistor between VSS and SNS.
SNS	4,5,6	A3	<b>Sense Resistor Connection.</b> Connect to the negative terminal of the battery pack. In the internal sense resistor configuration, the sense resistor is connected between VSS and SNS.
IS1	9	D4	<b>Current Sense Input.</b> This pin is internally connected to VSS through a 4.7k $\Omega$ resistor. Connect a 0.1 $\mu$ F capacitor between IS1 and IS2 to complete a low-pass input filter.
IS2	8	C4	<b>Current Sense Input.</b> This pin is internally connected to SNS through a 4.7k $\Omega$ resistor.
SNS probe	N/A	C2	<b>Do Not Connect.</b>
VSS probe	N/A	D2	<b>Do Not Connect.</b>

Mechanical drawing for the 16-pin TSSOP and DS2760 flip-chip package can be found at:

[/pdfserv.maxim-ic.com/arpdf/Packages/16tssop.pdf](http://pdfserv.maxim-ic.com/arpdf/Packages/16tssop.pdf)

[/pdfserv.maxim-ic.com/arpdf/Packages/chips/2760x.pdf](http://pdfserv.maxim-ic.com/arpdf/Packages/chips/2760x.pdf)

APPLICATION EXAMPLE Figure 2



$R_{SENS}$  is present for external sense resistor configurations only  
 $R_{SENSINT}$  is present for internal sense resistor configurations only

## OPERATION MODES

DS2760 has two power modes: Active and Sleep. While in Active Mode, the DS2760 continually measures current, voltage and temperature to provide data to the host system and to support current regulation and Li+ safety monitoring. In Sleep Mode, the DS2760 ceases these activities. The DS2760 enters Sleep Mode when any of the following conditions occurs:

- PMOD bit in the Status Register has been set to 1 and the DQ line is low for longer than 100 milliseconds (pack disconnection)
- voltage on VIN drops below undervoltage threshold  $V_{UV}$  for  $t_{UVD}$  (cell depletion)
- pack is disabled through the issuance of a SWAP command (SWEN bit =1)

DS2760 returns to Active Mode when any of the following occurs:

- PMOD bit has been set to 1 and the SWEN bit is set to 0 and the DQ line is pulled high (pack connection)
- $\overline{PS}$  pin is pulled low (power switch)
- voltage on PLS becomes greater than the voltage on VIN (charger connection) with the SWEN bit set to 0
- pack is enabled through the issuance of a SWAP command (SWEN bit =1)

DS2760 defaults to Sleep Mode when power is first applied.

## PROTECTION CIRCUITRY

While in Active Mode, the DS2760 constantly monitors cell voltage and current to protect the battery from overcharge (overvoltage), overdischarge (undervoltage) and excessive charge and discharge currents (overcurrent, short circuit). Conditions and DS2760 responses are described in the sections below and summarized in Table 2 and Figure 3.

### PROTECTION CONDITIONS AND DS2760 RESPONSES Table 2

Condition Name	Activation			Release Threshold
	Threshold	Delay	Response	
Overvoltage	$V_{IN} > V_{OV}$	$t_{OVD}$	$\overline{CC}$ high	$V_{IN} < V_{CE}$
Undervoltage	$V_{IN} < V_{UV}$	$t_{UVD}$	$\overline{CC}$ , $\overline{DC}$ high, Sleep Mode	$V_{PLS} > V_{DD}^{(1)}$ (charger connected)
Overcurrent, Charge	$V_{IS} > V_{OC}^{(2)}$	$t_{OCD}$	$\overline{CC}$ , $\overline{DC}$ high	$V_{PLS} < V_{DD} - V_{TP}^{(3)}$
Overcurrent, Discharge	$V_{IS} < -V_{OC}^{(2)}$	$t_{OCD}$	$\overline{DC}$ high	$V_{PLS} > V_{DD} - V_{TP}^{(4)}$
Short Circuit	$V_{SNS} > V_{SC}$	$t_{SCD}$	$\overline{DC}$ high	$V_{PLS} > V_{DD} - V_{TP}^{(4)}$

$V_{IS1} - V_{IS2}$ . Logic high =  $V_{PLS}$  for  $\overline{CC}$  and  $V_{DD}$  for  $\overline{DC}$ . All voltages are with respect to VSS.  $I_{SNS}$  is the sense current delivered from pin SNS.

When  $V_{DD} < 2.2V$ , release is delayed until the recovery charge current ( $I_{RC}$ ) passed from PLS to  $V_{DD}$  recharges the battery and allows  $V_{DD}$  to exceed 2.2V.

For the internal sense resistor configuration, the overcurrent thresholds are expressed in terms of current:  $I_{SNS} > I_{OC}$  for charge direction and  $I_{SNS} < -I_{OC}$  for discharge direction

with test current  $I_{TST}$  current flowing from PLS to VSS (pull-down on PLS)

with test current  $I_{TST}$  current flowing from  $V_{DD}$  to PLS (pull-up on PLS)

**Overvoltage.** If the voltage of the cell exceeds overvoltage threshold  $V_{OV}$  for a period longer than overvoltage delay  $t_{OVD}$ , the DS2760 shuts off the external charge FET and sets the OV flag in the Protection Register. When the cell voltage falls below charge enable threshold  $V_{CE}$ , the DS2760 turns the

FET back on (unless another protection condition prevents it). Discharging remains enabled overvoltage.

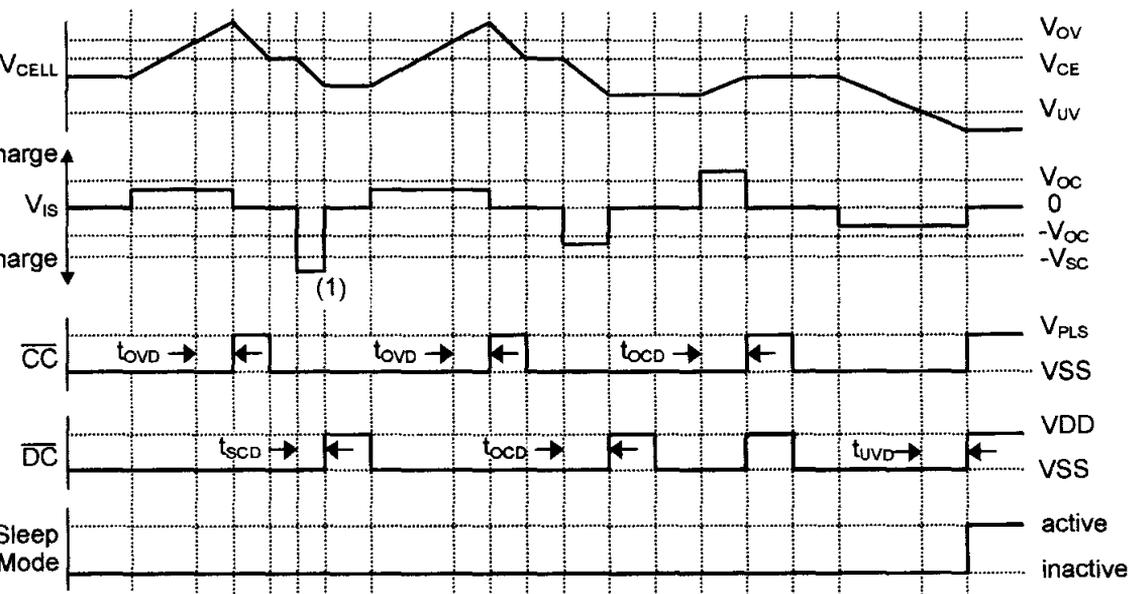
**voltage.** If the voltage of the cell drops below undervoltage threshold  $V_{UV}$  for a period longer than voltage delay  $t_{UVD}$ , the DS2760 shuts off the charge and discharge FETs, sets the UV flag in the Protection Register, and enters Sleep Mode. The DS2760 provides a current-limited ( $I_{RC}$ ) recovery path from PLS to VDD to gently charge severely depleted cells. The recovery path is enabled  $0 \leq V_{DD} < 3V(\text{typ})$ . Once VDD reaches  $3V(\text{typ})$ , the DS2760 will return to normal operation, and connection of a charger to turn on the charge FET and pull out of Sleep Mode.

**Current, Charge Direction.** The voltage difference between the IS1 pin and the IS2 pin ( $V_{IS} = V_{IS1} - V_{IS2}$ ) is the filtered voltage drop across the current sense resistor. If  $V_{IS}$  exceeds overcurrent threshold  $V_{OC}$  for a period longer than overcurrent delay  $t_{OCD}$ , the DS2760 shuts off both external FETs and sets the OVC flag in the Protection Register. The charge current path is not re-established until the voltage on the PLS pin drops below  $V_{DD} - V_{TP}$ . The DS2760 provides a test current of value  $I_{TST}$  from PLS to VSS to pull PLS down in order to detect the removal of the offending charge current source.

**Current, Discharge Direction.** If  $V_{IS}$  is less than  $-V_{OC}$  for a period longer than  $t_{OCD}$ , the DS2760 shuts off the external discharge FET and sets the DOC flag in the Protection Register. The discharge current path is not re-established until the voltage on PLS rises above  $V_{DD} - V_{TP}$ . The DS2760 provides a test current of value  $I_{TST}$  from  $V_{DD}$  to PLS to pull PLS up in order to detect the removal of the offending impedance load.

**Short Circuit.** If the voltage on the SNS pin with respect to VSS exceeds short circuit threshold  $V_{SC}$  for a period longer than short circuit delay  $t_{SCD}$ , the DS2760 shuts off the external discharge FET and sets the SC flag in the Protection Register. The discharge current path is not re-established until the voltage on PLS rises above  $V_{DD} - V_{TP}$ . The DS2760 provides a test current of value  $I_{TST}$  from  $V_{DD}$  to PLS to pull PLS up in order to detect the removal of the short circuit.

**LIUM-ION PROTECTION CIRCUITRY EXAMPLE WAVEFORMS Figure 3**



(1) To allow the device to react quickly to short circuits, detection is actually done on the SNS pin rather than on the filtered IS1 and IS2 pins. The actual short circuit detect condition is  $V_{SNS} > V_{SC}$ .

ary. All of the protection conditions described above are OR'ed together to affect the  $\overline{CC}$  and  $\overline{DC}$  S.

$\overline{DC}$  = (Undervoltage) or (Overcurrent, EITHER Direction) or (Short Circuit) or (Protection Register bit DE = 0) or (Sleep Mode)

$\overline{CC}$  = (Overvoltage) or (Undervoltage) or (Overcurrent, Charge Direction) or (Protection Register bit CE = 0) or (Sleep Mode)

## CURRENT MEASUREMENT

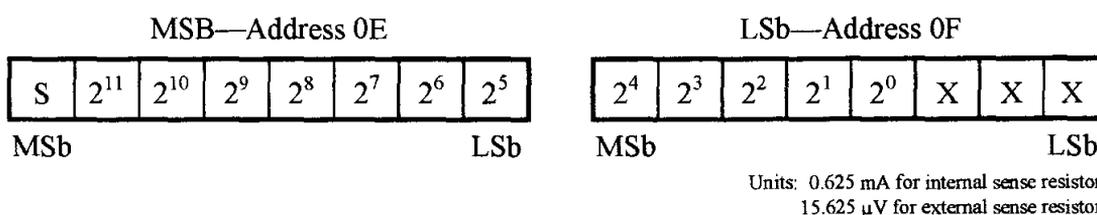
In Active Mode of operation, the DS2760 continually measures the current flow into and out of the battery by measuring the voltage drop across a current sense resistor. The DS2760 is available in two configurations: (1) internal 25mΩ current sense resistor, and (2) external user-selectable sense resistor. In the internal configuration, the DS2760 considers the voltage difference between pins IS1 and IS2 ( $V_{IS} = V_{IS1} - V_{IS2}$ ) to be the filtered voltage drop across the sense resistor. A positive  $V_{IS}$  value indicates current is flowing into the battery (charging), while a negative  $V_{IS}$  value indicates current is flowing out of the battery (discharging).

Current is measured with a signed resolution of 12-bits. The current register is updated in two's complement format every 88ms (128/fsample) with an average of 128 readings. Currents outside the range of the register are reported at the limit of the range. The format of the Current Register is shown in Figure 4.

In the internal sense resistor configuration, the DS2760 maintains the Current Register in units of Amps, with a resolution of 0.625mA and full scale range of no less than  $\pm 1.9A$  (see Note 7 on  $I_{FS}$  spec for more details). The DS2760 automatically compensates for internal sense resistor process variations and temperature effects when reporting current.

In the external sense resistor configuration, the DS2760 writes the measured  $V_{IS}$  voltage to the Current Register, with a resolution of 15.625μV and a full scale range of  $\pm 64mV$ .

## CURRENT REGISTER FORMAT Figure 4



## CURRENT ACCUMULATOR

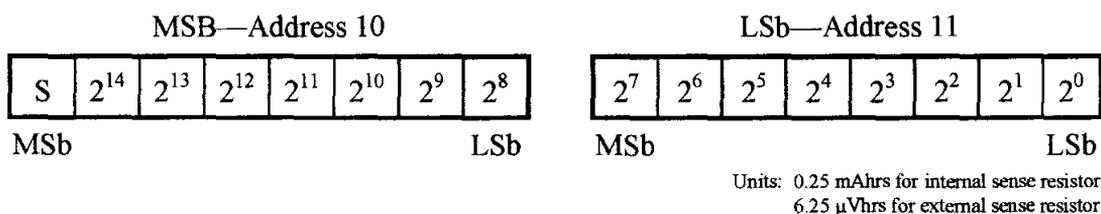
The Current Accumulator facilitates remaining capacity estimation by tracking the net current flow into and out of the battery. Current flow into the battery increments the Current Accumulator while current flow out of the battery decrements it. Data is maintained in the Current Accumulator in two's complement format. The format of the Current Accumulator is shown in Figure 5.

In the internal sense resistor configuration, the DS2760 maintains the Current Accumulator in units of Amp-hrs, with a resolution of 0.25mAhrs and full scale range of  $\pm 8.2Ahrs$ . When using an external sense

For the DS2760, the Current Accumulator maintains the Current Accumulator in units of Volt-hours, with a resolution of 0.25 mVhrs and a full scale range of  $\pm 205$  mVhrs.

The Current Accumulator is a read/write register that can be altered by the host system as needed.

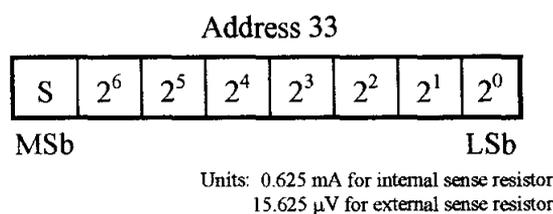
## CURRENT ACCUMULATOR FORMAT Figure 5



## CURRENT OFFSET COMPENSATION

The current measurement and the current accumulation are both internally compensated for offset on a regular basis minimizing error resulting from variations in device temperature and voltage. Additionally a constant bias may be utilized to alter any other sources of offset. This bias resides in I2C address 33h in two's-complement format and is subtracted from each current measurement. The current offset bias is applied to both the internal and external sense resistor configurations. The factory default for the current offset compensation is a value of 0.

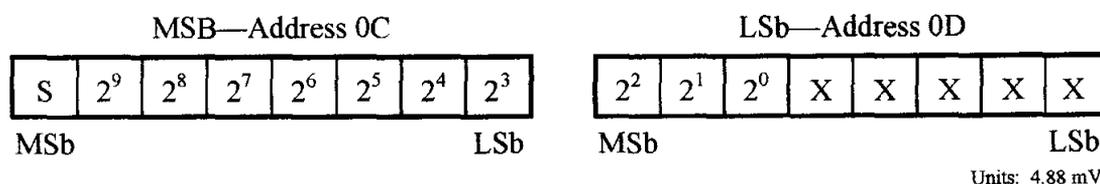
## CURRENT OFFSET BIAS Figure 6



## VOLTAGE MEASUREMENT

The DS2760 continually measures the voltage between pins VIN and VSS over a range of 0 to 4.75V. The resulting data is placed in the Voltage Register in two's-complement format with a resolution of 4.88 mV. Voltages above the maximum register value are reported as the maximum value. The Voltage Register format is shown in Figure 7.

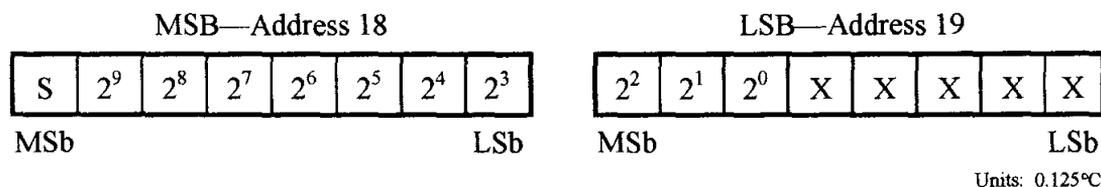
## VOLTAGE REGISTER FORMAT Figure 7



## TEMPERATURE MEASUREMENT

DS2760 uses an integrated temperature sensor to continually measure battery temperature. Temperature measurements are placed in the Temperature Register in two's-complement format with a resolution of  $0.125^{\circ}\text{C}$  over a range of  $\pm 127^{\circ}\text{C}$ . The Temperature Register format is shown in Figure 8.

### TEMPERATURE REGISTER FORMAT Figure 8



## PROGRAMMABLE I/O

To use the PIO pin as an output, write the desired output value to the PIO bit in the Special Feature Register. Writing a 0 to the PIO bit enables the PIO output driver, pulling the PIO pin to VSS. Writing a 1 to the PIO bit disables the output driver, allowing the PIO pin to be pulled high or used as an input. To read the value on the PIO pin, read the PIO bit. The DS2760 turns off the PIO output driver and sets the PIO pin high when it enters Sleep Mode or when DQ is low for more than 2 seconds, regardless of the state of the PMOD bit.

## POWER SWITCH INPUT

DS2760 provides a power control function that uses the discharge protection FET to gate battery power to the system. The  $\overline{\text{PS}}$  pin, internally pulled to  $V_{\text{DD}}$  through a  $1\mu\text{A}$  current source, is continuously monitored for a low-impedance connection to VSS. If the DS2760 is in Sleep Mode, the detection of a low on  $\overline{\text{PS}}$  causes the device to transition into Active Mode, turning on the discharge FET. If the DS2760 is already in Active Mode, activity on  $\overline{\text{PS}}$  has no effect other than the mirroring of its logic level in the  $\overline{\text{PS}}$  bit in the Special Feature Register. The reading of a 0 in the  $\overline{\text{PS}}$  bit should be immediately followed by writing a 1 to the  $\overline{\text{PS}}$  bit to ensure proper operation.

## EEPROM MEMORY

DS2760 has a 256-byte linear address space with registers for instrumentation, status and control in the first 32 bytes, with lockable EEPROM and SRAM memory occupying portions of the remaining address space. All EEPROM and SRAM memory is general-purpose except addresses 30h, 31h, and 33h, which should be written with the default values for the Protection Register, Status Register, and Current Register, respectively. When the MSB of any 2-byte register is read, both the MSB and LSB are latched and held for the duration of the Read Data command to prevent updates during the read and to ensure synchronization between the two register bytes. For consistent results, always read the MSB and LSB of a two-byte register during the same Read Data command sequence.

EEPROM memory is shadowed by RAM to eliminate programming delays between writes and to allow writes to be verified by the host system before being copied to EEPROM. All reads and writes to/from EEPROM memory actually access the shadow RAM. In unlocked EEPROM blocks, the Write Data command updates shadow RAM. In locked EEPROM blocks, the Write Data command is ignored. The Recall Data command copies the contents of shadow RAM to EEPROM in an unlocked block of EEPROM but has no effect on locked blocks. The Recall Data command copies the contents of a block of EEPROM to shadow RAM regardless of whether the block is locked or not.

## MEMORY MAP Table 3

Address (Hex)	Description	Read/Write
00	Protection Register	R/W
01	Status Register	R
02-06	Reserved	
07	EEPROM Register	R/W
08	Special Feature Register	R/W
09-0B	Reserved	
0C	Voltage Register MSb	R
0D	Voltage Register LSb	R
0E	Current Register MSB	R
0F	Current Register LSb	R
10	Accumulated Current Register MSB	R/W
11	Accumulated Current Register LSb	R/W
12-17	Reserved	
18	Temperature Register MSB	R
19	Temperature Register LSb	R
1A-1F	Reserved	
20-2F	EEPROM, block 0	R/W*
30-3F	EEPROM, block 1	R/W*
40-7F	Reserved	
80-8F	SRAM	R/W
90-FF	Reserved	

\*EEPROM block is read/write until locked by the LOCK command, after which it is read-only.

## PROTECTION REGISTER

The Protection Register consists of flags that indicate protection circuit status and switches that give additional control over the charging and discharging paths. Bits OV, UV, COC and DOC are set when corresponding protection conditions occur and remain set until cleared by the host system. The default values of the CE and DE bits of the Protection Register are stored in lockable EEPROM in the corresponding bits in address 30h. A Recall Data command for EEPROM block 1 recalls the default values of 1 into CE and DE. The format of the Protection Register is shown in Figure 9. The function of each bit is described in detail in the following paragraphs.

## PROTECTION REGISTER FORMAT Figure 9

Address 00							
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
OV	UV	COC	DOC	$\overline{CC}$	$\overline{DC}$	CE	DE

**OV** - Overvoltage Flag. When set to 1, this bit indicates the battery pack has experienced an overvoltage condition. This bit must be reset by the host system.

**UV** - Undervoltage Flag. When set to 1, this bit indicates the battery pack has experienced an undervoltage condition. This bit must be reset by the host system.

- Charge Overcurrent Flag. When set to 1, this bit indicates the battery pack has experienced a -direction overcurrent condition. This bit must be reset by the host system.

- Discharge Overcurrent Flag. When set to 1, this bit indicates the battery pack has experienced a rge-direction overcurrent condition. This bit must be reset by the host system.

$\overline{CC}$  Pin Mirror. This read-only bit mirrors the state of the  $\overline{CC}$  output pin.

$\overline{DC}$  Pin Mirror. This read-only bit mirrors the state of the  $\overline{DC}$  output pin.

Charge Enable. Writing a 0 to this bit disables charging ( $\overline{CC}$  output high, external charge FET off) less of cell or pack conditions. Writing a 1 to this bit enables charging, subject to override by the ice of any protection conditions. The DS2760 automatically sets this bit to 1 when it transitions Sleep Mode to Active Mode.

Discharge Enable. Writing a 0 to this bit disables discharging ( $\overline{DC}$  output high, external discharge off) regardless of cell or pack conditions. Writing a 1 to this bit enables discharging, subject to de by the presence of any protection conditions. The DS2760 automatically sets this bit to 1 when sitions from Sleep Mode to Active Mode.

## STATUS REGISTER

Default values for the Status Register bits are stored in lockable EEPROM in the corresponding bits address 31h. A Recall Data command for EEPROM block 1 recalls the default values into the Status Register bits. The format of the Status Register is shown in Figure 10. The function of each bit is iberbed in detail in the following paragraphs.

### STATUS REGISTER FORMAT Figure 10

Address 01

bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
X	X	PMOD	RNAOP	SWEN	X	X	X

**MOD** – Sleep Mode Enable. A value of 1 in this bit enables the DS2760 to enter Sleep Mode when the line goes low for greater than 2 seconds and leave Sleep Mode when the DQ line goes high. A value disables DQ-related transitions into and out of Sleep Mode. This bit is read-only. The desired default value should be set in bit 5 of address 31h. The factory default is 0.

**OP** – Read Net Address Opcode. A value of 0 in this bit sets the opcode for the Read Net Address command to 33h, while a 1 sets the opcode to 39h. This bit is read-only. The desired default value should t in bit 4 of address 31h. The factory default is 0.

**EN** - SWAP Command Enable. A value of 1 in this bit location enables the recognition of a SWAP command. If set to 0, SWAP commands are ignored. The desired default value should be set in bit 3 of sss 31h. This bit is read-only. The factory default is 0.

Reserved bits.

## ROM REGISTER

Format of the EEPROM Register is shown in Figure 11. The function of each bit is described in the following paragraphs.

### ROM REGISTER FORMAT Figure 11

Address 07							
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
EEC	LOCK	X	X	X	X	BL1	BL0

– EEPROM Copy Flag. A 1 in this read-only bit indicates that a Copy Data command is in progress. While this bit is high, writes to EEPROM addresses are ignored. A 0 in this bit indicates that data may be written to unlocked EEPROM blocks.

– EEPROM Lock Enable. When this bit is 0, the Lock command is ignored. Writing a 1 to this bit enables the Lock command. After the Lock command is executed, the LOCK bit is reset to 0. The bit's default is 0.

– EEPROM Block 1 Lock Flag. A 1 in this read-only bit indicates that EEPROM Block 1 (addresses 30-3F) is locked (read-only) while a 0 indicates Block 1 is unlocked (read/write).

– EEPROM Block 0 Lock Flag. A 1 in this read-only bit indicates that EEPROM Block 0 (addresses 20-2F) is locked (read-only) while a 0 indicates Block 0 is unlocked (read/write).

Reserved bits.

## SPECIAL FEATURE REGISTER

Format of the Special Feature Register is shown in Figure 12. The function of each bit is described in the following paragraphs.

### SPECIAL FEATURE REGISTER FORMAT Figure 12

Address 08							
bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
$\overline{\text{PS}}$	PIO	MSTR	X	X	X	X	X

–  $\overline{\text{PS}}$  Pin Mirror. This read-only bit mirrors the state of the PS pin. The reading of a 0 in this bit should be immediately followed by writing a 1 to this location to insure proper operation.

– PIO Pin Sense and Control. See the *Programmable I/O* section for details on this read/write bit.

– MSTR - SWAP Master Status Bit. This bit indicates whether a device has been selected through the SWAP command. Selection of this device through the SWAP command and the appropriate Net Address result in setting this bit, indicating that this device is the master. A 0 signifies that this device is not the master.

Reserved bits.

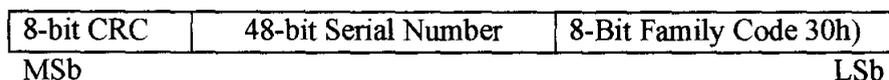
## 1-WIRE BUS SYSTEM

A 1-Wire bus is a system which has a single bus master and one or more slaves. A multidrop bus is a bus with multiple slaves. A single-drop bus has only one slave device. In all instances, the DS2760 is a slave device. The bus master is typically a microprocessor in the host system. The operation of this bus system consists of four topics: 64-Bit Net Address, Hardware Configuration, Command Sequence, and 1-Wire Signaling.

## 1-WIRE NET ADDRESS

The DS2760 has a unique, factory-programmed 1-Wire net address which is 64 bits in length. The first 8 bits are the 1-Wire family code (30h for DS2760). The next 48 bits are a unique serial number. The last 8 bits are a CRC of the first 56 bits (see Figure 13). The 64-bit net address and the 1-Wire I/O controller built into the device enable the DS2760 to communicate via the 1-Wire protocol detailed in the 1-Wire Bus System section of this data sheet.

### 1-WIRE NET ADDRESS FORMAT Figure 13



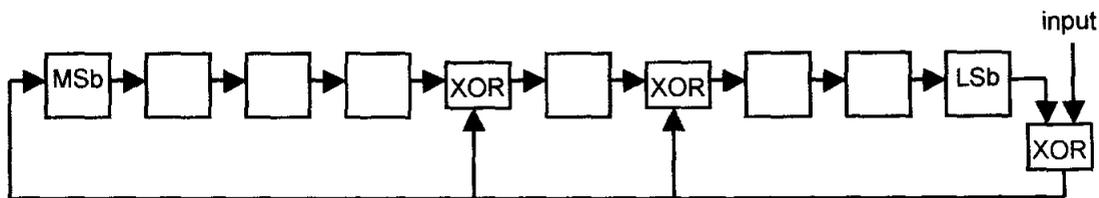
## CRC GENERATION

The DS2760 has an 8-bit CRC stored in the most significant byte of its 1-Wire net address. To ensure error-free transmission of the address, the host system can compute a CRC value from the first 56 bits of the address and compare it to the CRC from the DS2760. The host system is responsible for verifying the CRC value and taking action as a result. The DS2760 does not compare CRC values and does not generate a command sequence from proceeding as a result of a CRC mismatch. Proper use of the CRC results in a communication channel with a very high level of integrity.

The CRC can be generated by the host using a circuit consisting of a shift register and XOR gates as shown in Figure 10, or it can be generated in software. Additional information about the Dallas 1-Wire Cyclic Redundancy Check is available in Application Note 27 entitled "Understanding and Using Cyclic Redundancy Checks with Dallas Semiconductor Touch Memory Products". (This application note can be found on the Maxim/Dallas Semiconductor website at [www.maxim-ic.com](http://www.maxim-ic.com)).

In the circuit in Figure 14, the shift register bits are initialized to 0. Then, starting with the least significant bit of the family code, one bit at a time is shifted in. After the 8<sup>th</sup> bit of the family code has been entered, then the serial number is entered. After the 48<sup>th</sup> bit of the serial number has been entered, the shift register contains the CRC value.

**1-WIRE CRC GENERATION BLOCK DIAGRAM Figure 14**

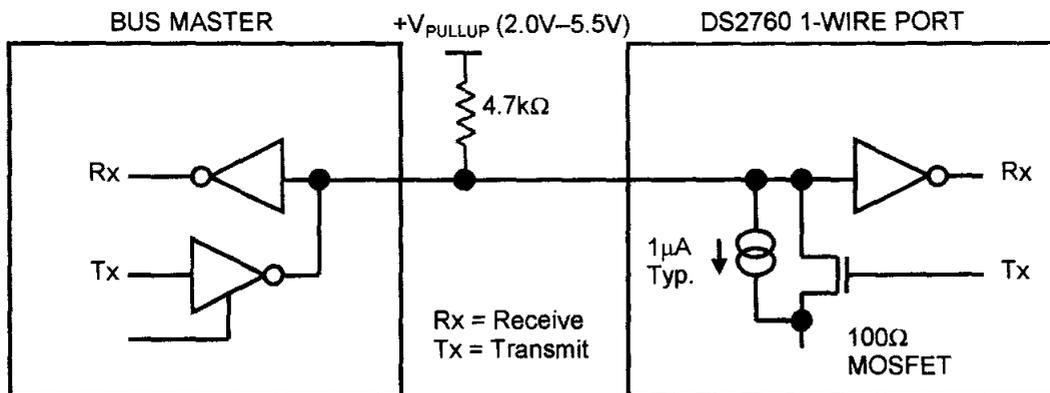


**1-WIRE SOFTWARE CONFIGURATION**

Since the 1-Wire bus has only a single line, it is important that each device on the bus be able to drive the line for an appropriate time. To facilitate this, each device attached to the 1-Wire bus must connect to the bus through open-drain or tri-state output drivers. The DS2760 used an open-drain output driver as part of its directional interface circuitry shown in Figure 15. If a bidirectional pin is not available on the bus master, separate output and input pins can be tied together.

The 1-Wire bus must have a pull-up resistor at the bus-master end of the bus. For short line lengths, the value of this resistor should be approximately 5kΩ. The idle state for the 1-Wire bus is high. If, for any reason, a bus transaction must be suspended, the bus MUST be left in the idle state in order to properly resume the transaction later. If the bus is left low for more than 120μs, slave devices on the bus begin to interpret the low period as a Reset Pulse, effectively terminating the transaction.

**1-WIRE BUS INTERFACE CIRCUITRY Figure 15**



**1-WIRE TRANSACTION SEQUENCE**

The protocol for accessing the DS2760 via the 1-Wire port is as follows:

- 1. Initialization
- 2. Set Address Command
- 3. Function Command
- 4. Transaction/Data

The sections that follow describe each of these steps in detail.

Transactions of the 1-Wire bus begin with an initialization sequence consisting of a Reset Pulse issued by the bus master followed by a presence pulse simultaneously transmitted by the DS2760 and other slaves on the bus. The presence pulse tells the bus master that one or more devices are on the bus and ready to operate. For more details, see the *1-Wire Signaling* section.

## ADDRESS COMMANDS

When the bus master has detected the presence of one or more slaves, it can issue one of the Net Address Commands described in the following paragraphs. The name of each ROM Command is followed by the opcode for that command in square brackets. Figure 16 presents a transaction flowchart of the Net Address Commands.

**Net Address [33h or 39h].** This command allows the bus master to read the DS2760's 1-Wire net address. This command can only be used if there is a single slave on the bus. If more than one slave is present, a data collision occurs when all slaves try to transmit at the same time (open-drain produces a  $\overline{\text{AND}}$  result). The RNAOP bit in the Status Register selects the opcode for this command, with RNAOP=0 indicating 33h and RNAOP=1 indicating 39h.

**Single Net Address [55h].** This command allows the bus master to specifically address one DS2760 on the 1-Wire bus. Only the addressed DS2760 responds to any subsequent Function Command. All other devices ignore the Function Command and wait for a reset pulse. This command can be used with more than one slave device on the bus.

**Default Net Address [CCh].** This command saves time when there is only one DS2760 on the bus by allowing the bus master to issue a Function Command without specifying the address of the slave. If more than one slave device is present on the bus, a subsequent Function Command can cause a data collision when all slaves transmit data at the same time.

**Search Net Address [F0h].** This command allows the bus master to use a process of elimination to identify the 1-Wire net addresses of all slave devices on the bus. The search process involves the execution of a simple three-step routine: read a bit, read the complement of the bit, then write the desired value of that bit. The bus master performs this simple three-step routine on each bit location of the net address. After one complete pass through all 64 bits, the bus master knows the address of one device. Remaining devices can then be identified on additional iterations of the process. See Chapter 5 of the *Application of DS19xx iButton® Standards* for a comprehensive discussion of a net address search, including an example. (This publication can be found on the Maxim/Dallas Semiconductor website at [www.maxim-ic.com](http://www.maxim-ic.com)).

**SWAP [AAh].** SWAP is a Net Address level command specifically intended to aid in distributed multiplexing applications and is described specifically with regards to power control using the 27xx series products. The term power control refers to the ability of the DS2760 to control the flow of power into and out of the battery pack using control pins  $\overline{\text{DC}}$  and  $\overline{\text{CC}}$ . The SWAP command is issued followed by the Net Address. The effect is to cause the addressed device to enable power to or from the system while simultaneously (break-before-make) deselecting and powering down (SLEEP) all other packs. This sequencing sequence is controlled by a timing pulse issued on the DQ line following the net address. The falling edge of the pulse is used to disable power with the rising edge enabling power flow by the selected device. The DS2760 will recognize a SWAP command, device address, and timing pulse if and only if the WEN bit is set.

## FUNCTION COMMANDS

Successfully completing one of the Net Address Commands, the bus master can access the features of the DS2760 with any of the Function Commands described in the following paragraphs. The name of the function is followed by the 8-bit opcode for that command in square brackets.

**Data [69h, XX].** This command reads data from the DS2760 starting at memory address XX. The first byte of the data in address XX is available to be read immediately after the MSb of the address has been received. Because the address is automatically incremented after the MSb of each byte is received, the second byte of the data at address XX+1 is available to be read immediately after the MSb of the data at address XX is received. If the bus master continues to read beyond address FFh, the DS2760 outputs logic 1 until a Reset occurs. Addresses labeled “Reserved” in the Memory Map contain undefined data. The Read Data Command may be terminated by the bus master with a Reset Pulse at any bit boundary.

**Data [6Ch, XX].** This command writes data to the DS2760 starting at memory address XX. The first byte of the data to be stored at address XX can be written immediately after the MSb of address XX has been received. Because the address is automatically incremented after the MSb of each byte is written, the second byte of the data to be stored at address XX+1 can be written immediately after the MSb of the data to be stored at address XX is received. If the bus master continues to write beyond address FFh, the DS2760 ignores the data. Writes to read-only memory, reserved addresses and locked EEPROM blocks are ignored. Incomplete bytes are not written. Writes to unlocked EEPROM blocks are to shadow RAM rather than EEPROM. See the *Memory* section for more details.

**Data [48h, XX].** This command copies the contents of shadow RAM to EEPROM for the 16-byte EEPROM block containing address XX. Copy Data commands that address locked blocks are ignored. While the Copy Data command is executing, the EEC bit in the EEPROM Register is set to 1 and writes to EEPROM addresses are ignored. Reads and writes to non-EEPROM addresses can still occur while the Copy Data command is in progress. The Copy Data command takes  $t_{EEC}$  time to execute, starting on the next falling edge of the bus after the address is transmitted.

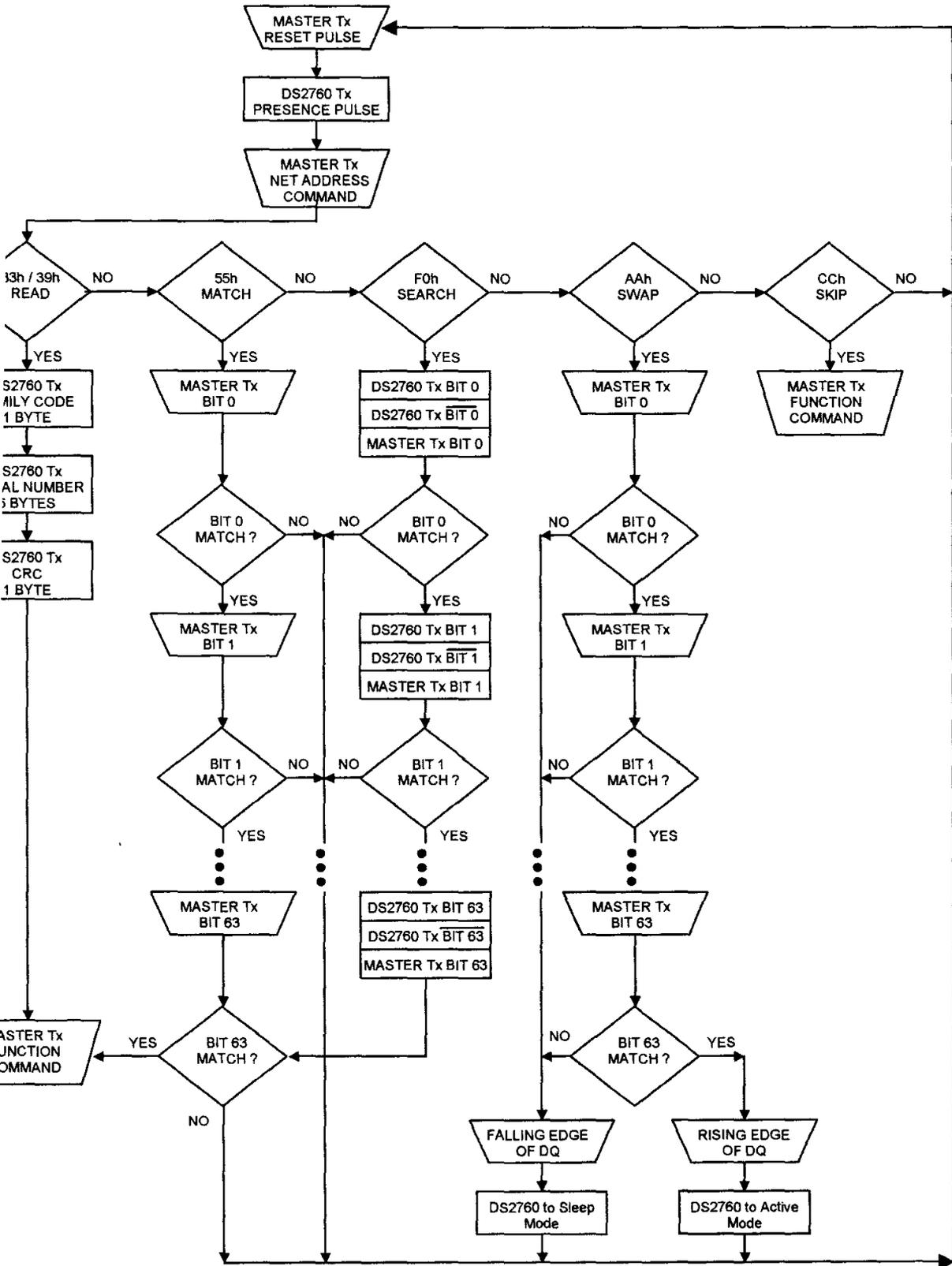
**Data [B8h, XX].** This command recalls the contents of the 16-byte EEPROM block containing address XX to shadow RAM.

**Data [6Ah, XX].** This command locks (write-protects) the 16-byte block of EEPROM memory beginning at memory address XX. The LOCK bit in the EEPROM Register must be set to 1 before the Lock command is executed. If the LOCK bit is 0, the Lock command has no effect. The Lock command is permanent; a locked block can never be written again.

**FUNCTION COMMANDS Table 4**

Command	Description	Command Protocol	Bus State After Command Protocol	Bus Data
Read Data	Reads data from memory starting at address XX	69h, XX	Master Rx	up to 256 bytes of data
Write Data	Writes data to memory starting at address XX	6Ch, XX	Master Tx	up to 256 bytes of data
Copy Data	Copies shadow RAM data to EEPROM block containing address XX	48h, XX	Bus Idle	none
Recall Data	Recalls EEPROM block containing address XX to shadow RAM	B8h, XX	Bus Idle	none
Lock	Permanently locks the block of EEPROM containing address XX	6Ah, XX	Bus Idle	none

ADDRESS COMMAND FLOW CHART Figure 16

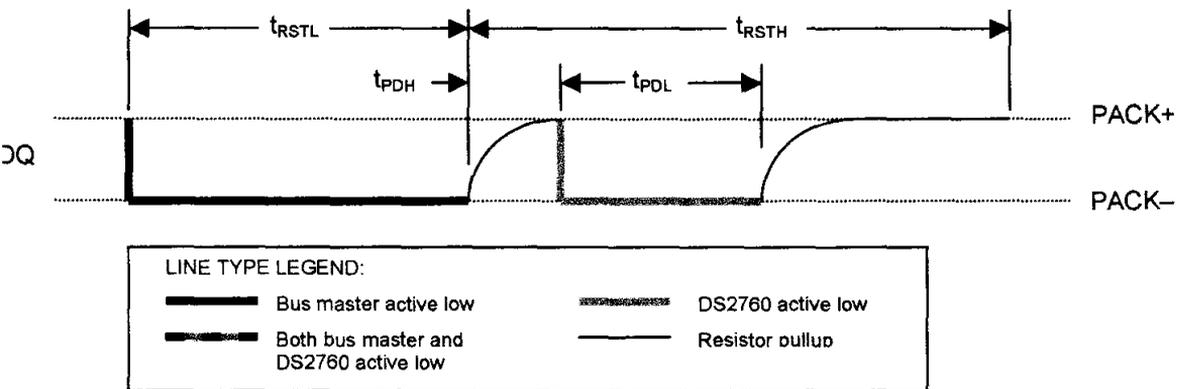


## SIGNALING

1-Wire bus requires strict signaling protocols to insure data integrity. The four protocols used by the DS2760 are: the initialization sequence (Reset Pulse followed by Presence Pulse), Write 0, Write 1, and Data. All of these types of signaling except the Presence Pulse are initiated by the bus master.

The initialization sequence required to begin any communication with the DS2760 is shown in Figure 17. The Presence Pulse following a Reset Pulse indicates the DS2760 is ready to accept a Net Address and Data. The bus master transmits (Tx) a Reset Pulse for  $t_{RSTL}$ . The bus master then releases the line and goes into receive mode (Rx). The 1-Wire bus line is then pulled high by the pull-up resistor. After sensing the rising edge on the DQ pin, the DS2760 waits for  $t_{PDH}$  and then transmits the Presence Pulse for  $t_{PDL}$ .

### 1-WIRE INITIALIZATION SEQUENCE Figure 17



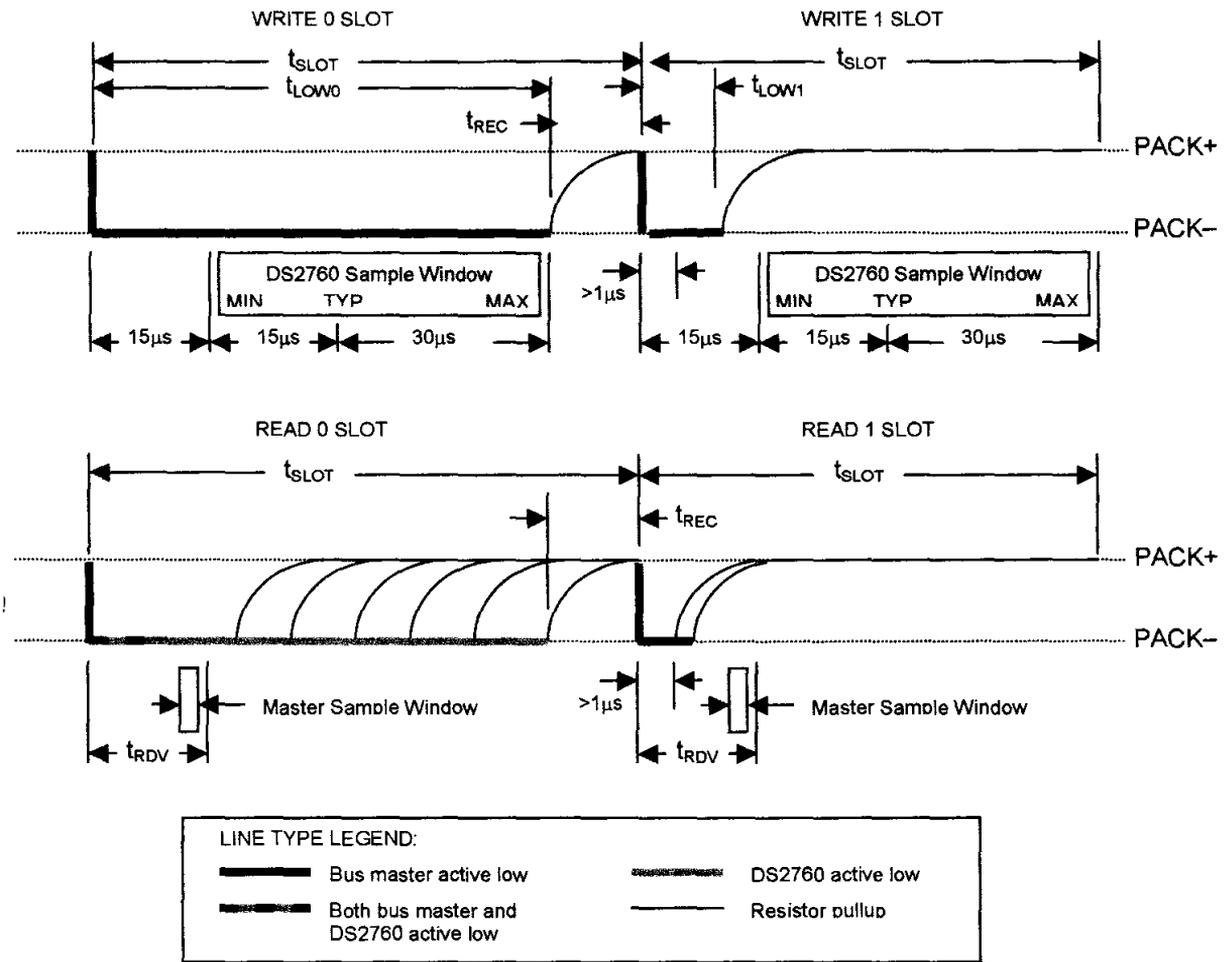
## WRITE TIME SLOTS

A write time slot is initiated when the bus master pulls the 1-Wire bus from a logic high (inactive) level to a logic low level. There are two types of write time slots: Write 1 and Write 0. All write time slots must be 60µs to 120µs in duration with a 1µs minimum recovery time,  $t_{REC}$ , between cycles. The DS2760 samples the 1-Wire bus line between 15µs and 60µs after the line falls. If the line is high when sampled, a Write 1 occurs. If the line is low when sampled, a Write 0 occurs (see Figure 18). For the bus master to generate a Write 1 time slot, the bus line must be pulled low and then released, allowing the line to be pulled high within 15µs after the start of the write time slot. For the host to generate a Write 0 time slot, the bus line must be pulled low and held low for the duration of the write time slot.

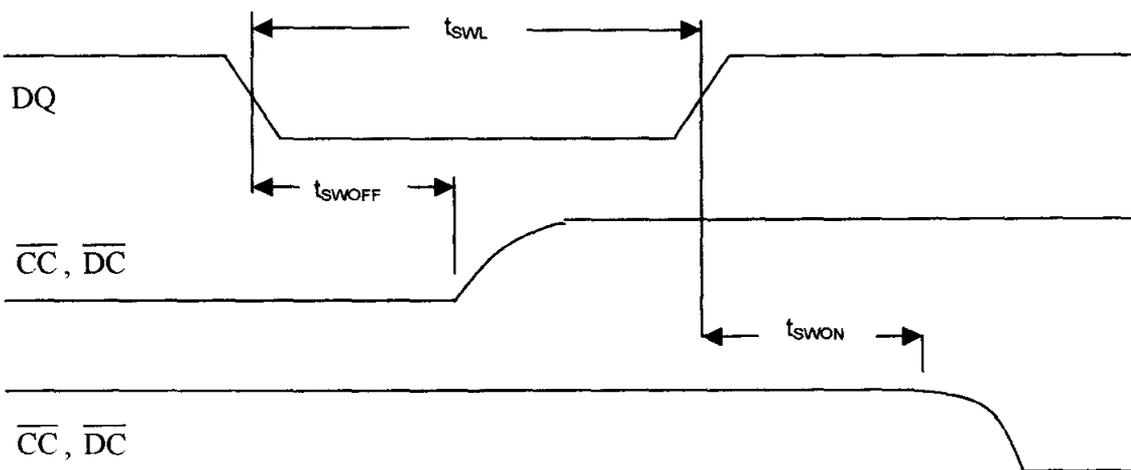
## READ TIME SLOTS

A read time slot is initiated when the bus master pulls the 1-Wire bus line from a logic high level to a logic low level. The bus master must keep the bus line low for at least 1µs and then release it to allow the DS2760 to present valid data. The bus master can then sample the data  $t_{RDV}$  (15µs) from the start of the read time slot. By the end of the read time slot, the DS2760 releases the bus line and allows it to be pulled high by the external pull-up resistor. All read time slots must be 60µs to 120µs in duration with a 1µs minimum recovery time,  $t_{REC}$ , between cycles. See Figure 18 for more information.

**RE WRITE AND READ TIME SLOTS Figure 18**



**AP COMMAND TIMING Figure 19**



**ABSOLUTE MAXIMUM RATINGS\***

Voltage on PLS and $\overline{CC}$ pin, Relative to VSS	-0.3V to +18V
Voltage on PIO pin, Relative to VSS	-0.3V to +12V
Voltage on VIN and $\overline{PS}$ , Relative to VSS	-0.3V to $V_{DD} + 0.3$
Voltage on any other pin, Relative to VSS	-0.3V to +6V
Continuous Internal Sense Resistor Current	$\pm 2.5$ A
Maximum Internal Sense Resistor Current	$\pm 50$ A for $<100\mu\text{s/sec}$ , $<1000$ pulses
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-55°C to +125°C
Shipping Temperature	See IPC/JEDEC J-STD-020A Specification

\*This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

**RECOMMENDED DC****OPERATING CONDITIONS**(-20°C to +70°C,  $2.5\text{V} \leq V_{DD} \leq 5.5\text{V}$ )

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	$V_{DD}$		2.5		5.5	V	1
Input Pin	DQ		-0.3		5.5	V	1

**ELECTRICAL CHARACTERISTICS**(-20°C to +70°C;  $2.5\text{V} \leq V_{DD} \leq 5.5\text{V}$ )

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS	NOTES
Supply Current	$I_{ACTIVE}$	DQ = $V_{DD}$ , norm. operation		60	90	$\mu\text{A}$	
Sleep Mode Current	$I_{SLEEP}$	DQ = 0V, no activity, $\overline{PS}$ floating		1	2	$\mu\text{A}$	
Input Logic High: PIO	$V_{IH}$		1.5			V	1
Input Logic High: $\overline{PS}$	$V_{IH}$		$V_{DD} - 0.2\text{V}$			V	1
Input Logic Low: PIO	$V_{IL}$				0.4	V	1
Input Logic Low: $\overline{PS}$	$V_{IL}$				0.2	V	1
Output Logic High: $\overline{CC}$	$V_{OH}$	$I_{OH} = -0.1\text{mA}$	$V_{PLS} - 0.4\text{V}$			V	1
Output Logic High: $\overline{DC}$	$V_{OH}$	$I_{OH} = -0.1\text{mA}$	$V_{DD} - 0.4\text{V}$			V	1
Output Logic Low: $\overline{CC}$ , $\overline{DC}$	$V_{OL}$	$I_{OL} = 0.1\text{mA}$			0.4	V	1
Output Logic Low: PIO	$V_{OL}$	$I_{OL} = 4\text{mA}$			0.4	V	1
Pulldown Current	$I_{PD}$			1		$\mu\text{A}$	
Input Resistance: VIN	$R_{IN}$		5			$\text{M}\Omega$	
Internal Current Sense Resistor	$R_{SNS}$	+25°C	20	25	30	$\text{m}\Omega$	
Wake Low to Sleep time	$t_{SLEEP}$		2.1			sec	

**CRITICAL CHARACTERISTICS:****TECTION CIRCUITRY****(0°C to +50°C; 2.5V ≤ V<sub>DD</sub> ≤ 5.5V)**

<b>PARAMETER</b>	<b>SYMBOL</b>	<b>MIN</b>	<b>TYP</b>	<b>MAX</b>	<b>UNITS</b>	<b>NOTES</b>
Overvoltage Detect	V <sub>OV</sub>	4.325 4.250	4.350 4.275	4.375 4.300	V	1, 2
Charge Enable	V <sub>CE</sub>	4.10	4.15	4.20	V	1
Undervoltage Detect	V <sub>UV</sub>	2.5	2.6	2.7	V	1
Overcurrent Detect	I <sub>OC</sub>	1.8	1.9	2.0	A	3
Undercurrent Detect	V <sub>OC</sub>	45	47.5	50	mV	1, 4
Short Circuit Detect	I <sub>SC</sub>	5.0	8.0	11	A	3
Open Circuit Detect	V <sub>SC</sub>	150	200	250	mV	1
Overvoltage Delay	t <sub>OVD</sub>	0.8	1	1.2	sec	
Undervoltage Delay	t <sub>UV</sub>	90	100	110	ms	
Overcurrent Delay	t <sub>OC</sub>	5	10	20	ms	
Short Circuit Delay	t <sub>SC</sub>	80	100	120	μs	
Threshold	V <sub>TP</sub>	0.5	1.0	1.5	V	
Test Current	I <sub>TST</sub>	10	20	40	μA	
Recovery Charge Current	I <sub>RC</sub>	0.5	1	2	mA	13

**CRITICAL CHARACTERISTICS:****TEMPERATURE, VOLTAGE, CURRENT****(0°C to +50°C; 2.5V ≤ V<sub>DD</sub> ≤ 5.5V)**

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Temperature Resolution	T <sub>LSB</sub>		0.125		°C	
Temperature Full Scale Resolution	T <sub>FS</sub>	127			°C	
Temperature Error	T <sub>ERR</sub>			±3	°C	5
Voltage Resolution	V <sub>LSB</sub>		4.88		mV	
Voltage Full Scale Resolution	V <sub>FS</sub>	4.75			V	
Voltage Offset Error	V <sub>OERR</sub>			1	LSB	6
Voltage Gain Error	V <sub>GERR</sub>			5	%V reading	
Current Resolution	I <sub>LSB</sub>		0.625 15.625		mA μV	3 4
Current Full Scale Resolution	I <sub>FS</sub>	1.9	2.56 64		A mV	3, 7 4
Current Offset Error	I <sub>OERR</sub>			1	LSB	8
Current Gain Error	I <sub>GERR</sub>			3 1	%I reading	3, 9, 14 4
Integrated Current Resolution	q <sub>CA</sub>		0.25 6.25		mAhr μVhr	3 4
Current Sampling Frequency	f <sub>SAMP</sub>		1456		Hz	
Internal Timebase Accuracy	t <sub>ERR</sub>		±1	±3	%	10

**CRITICAL CHARACTERISTICS:****RE INTERFACE**(-20°C to +70°C; 2.5V ≤ V<sub>DD</sub> ≤ 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Slot	t <sub>SLOT</sub>	60		120	μs	
Recovery Time	t <sub>REC</sub>	1			μs	
0 Low Time	t <sub>LOW0</sub>	60		120	μs	
1 Low Time	t <sub>LOW1</sub>	1		15	μs	
Data Valid	t <sub>RDV</sub>			15	μs	
Time High	t <sub>RSTH</sub>	480			μs	
Time Low	t <sub>RSTL</sub>	480		960	μs	
ence Detect High	t <sub>PDH</sub>	15		60	μs	
ence Detect Low	t <sub>PDL</sub>	60		240	μs	
AP timing pulse width	t <sub>SWL</sub>	0.2		120	μs	
AP timing pulse	t <sub>SWOFF</sub>	0		1	μs	12
ing edge to DC release						
AP timing pulse rising	t <sub>SWON</sub>	0		1	μs	12
to DC engage						
Capacitance	C <sub>DQ</sub>			60	pF	

**FROM RELIABILITY SPECIFICATION**(-20°C to +70°C; 2.5V ≤ V<sub>DD</sub> ≤ 5.5V)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Time to EEPROM Time	t <sub>EEC</sub>		2	10	ms	
EEPROM Copy Endurance	N <sub>EEC</sub>	25000			cycles	11

**NOTES**

All voltages are referenced to VSS.

See "Ordering Information" section of datasheet to determine corresponding part number for each V<sub>OV</sub> value.

Internal current sense resistor configuration.

External current sense resistor configuration.

Self heating due to output pin loading and sense resistor power dissipation can alter the reading from ambient conditions.

Voltage offset measurement is with respect to V<sub>OV</sub> at +25°C.

The current register supports measurement magnitudes up to 2.56A using the internal sense resistor option and 64mV with the external resistor option. Compensation of the internal sense resistor value for process and temperature variation can reduce the maximum reportable magnitude to 1.9A.

Current offset error null to ±1LSB typically requires 3.5s in-system calibration by user.

Current gain error specification applies to gain error in converting the voltage difference at IS1 and IS2, and excludes any error remaining after the DS2760 compensates for the internal sense resistor's temperature coefficient of 3700ppm/°C to an accuracy of ±500ppm/°C. The DS2760 does not compensate for external sense resistor characteristics, and any error terms arising from the use of an external sense resistor should be taken into account when calculating total current measurement error.

Typical value for t<sub>ERR</sub> is at 3.6V and +25°C.

10-year data retention at +70°C.

Typical load capacitance on  $\overline{DC}$  and  $\overline{CC}$  is 1000pF.

Test conditions are PLS = 4.1V, V<sub>DD</sub> = 2.5V. Maximum current for conditions of PLS = 15V, V<sub>DD</sub> = 0V is 10mA.

Error at time of shipment from Dallas Semiconductor is 3% max. Board mounting processes may cause the current gain error to widen to as much as 10% for devices with the internal sense resistor option. Contact factory for on-board calibration procedure for devices with the internal sense resistor option to improve accuracy.



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Educational: [www.stampsinclass.com](http://www.stampsinclass.com)

# DS2760 Thermocouple Kit (#28022)

## 1-Wire<sup>®</sup> Thermocouple Interface

### Introduction

Thermocouples provide a low-cost, reliable means of measuring temperature over a wide range. The challenge when using a thermocouple is accurately measuring the very low Seebeck output voltage (fractional to low millivolts) from the element, and providing for cold junction temperature compensation.

The Dallas/Maxim DS2760 High Precision Li+ Battery Monitor is very easily configured into an effective thermocouple interface. The Parallax DS2760 Thermocouple Module capitalizes on this application and provides a complete connection between the BASIC Stamp and a standard thermocouple element.

### Features

- 1-Wire<sup>®</sup> interface allows multiple devices with just one Stamp IO pin
- Cold Junction measurement: 0°C to +127°C (0.125°C resolution)
- Low power consumption:
  - Active current: 90  $\mu$ A max
  - Sleep current: 2  $\mu$ A max

### Packing List

Verify that your DS2760 kit is complete in accordance with the list below:

- DS2760 Thermocouple Module #550-28022
- (3) Thermocouple elements:
  - (1) K-type (Chromel / Alumel) #800-00011
  - (1) J-type (Iron / Constantan) #800-00012
  - (1) T-type (Copper / Constantan) #800-00010
- This documentation

Note: DS2760 demonstration software may be downloaded from [www.parallax.com](http://www.parallax.com).

## Connections

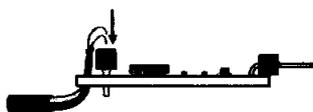
Before connecting the DS2760 Thermocouple Module to the BASIC Stamp you will need to prepare a thermocouple element, and then connect it to the cold junction port of the module. Start by carefully removing about one inch (250 mm) of the outer sleeve from each end of the element. From each lead on the temperature measurement end, remove about ½ inch (125 mm) of insulation and then carefully twist together (using pliers if necessary) and trim as shown in Figure 1.

**Figure 1: Thermocouple Junction**



On the cold junction (DS2760 module) end of the element, remove only ¼ inch (60 mm) of insulation from each lead. Route these leads through the bottom of the thermocouple module PCB and insert snugly into the pin sockets as shown in Figure 2.

**Figure 2: Cold Junction Connection to DS2760 PCB**

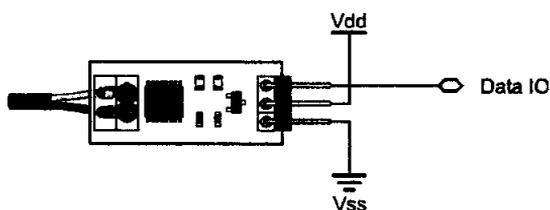


Use this table to ensure that you make the proper thermocouple connections to the module. If the leads are reversed, the measured temperature will be incorrect.

Type	Materials	SNS	Vss
K	Chromel / Alumel	Red	Yellow
J	Iron / Constantan	Red	White
T	Copper / Constantan	Red	Blue

Finally, the DS2760 Thermocouple Module is connected to the BASIC Stamp as shown in Figure 3 below (Note that the module includes a 4.7 KΩ pull-up on the 1-Wire® data line).

**Figure 3: DS2760 Connections to BASIC Stamp**



## BASIC Stamp Application

The following BASIC Stamp application will run on either the BS2p or BS2pe and demonstrates how easy measuring wide-range temperatures can be when using the DS2760 Thermocouple Module. Other Stamps will require a Serial-to-1-Wire protocol converter, as well as code to manage the large tables across program slots, and are not covered in this document.

A little background: When two dissimilar metal wires are joined, a voltage will be developed across the open end that is proportional to the temperature difference between the joined and open ends. This effect was discovered by Thomas Seebeck in 1821. Through empirical testing, voltage tables have been established that correspond to the thermocouple junction temperature. These tables, however, use a cold junction (voltage measurement point) reference of zero degrees Celsius, forcing electronic devices to employ cold junction compensation.

Using the DS2760 we can measure the Seebeck voltage from the thermocouple with a resolution of 15.625 microvolts, then measure the cold junction temperature with a resolution of 0.125 degrees Celsius. A simple table look-up using the cold junction temperature will give us the cold junction compensation voltage. This is combined with the Seebeck voltage and, using a modified binary search algorithm, we can determine the compensated temperature from the thermocouple data table.

```
' =====
'
'   File..... DS2760TC_Demo.BPE
'   Purpose... Thermocouple temperature measurement using the DS2760
'   Author.... Parallax, Inc.  (Copyright 2004, All Rights Reserved)
'   E-mail.... support@parallax.com
'   Started...
'   Updated... 19 JAN 2004
'
'   {$STAMP BS2pe, KTablePos.BPE, JTablePos.BPE, TTablePos.BPE}
'   {$PBASIC 2.5}
' =====
'
' -----[ Program Description ]-----
'
' This program lets a BS2p or BS2pe read the temperature from the Parallax
' DS2760 thermocouple module.  User input of thermocouple type (K, J, or T)
' and temperature display is via the DEBUG window.
'
' -----[ Revision History ]-----
'
' -----[ I/O Definitions ]-----
'
OW                PIN      8                ' 1-Wire buss pin
```

' -----[ Constants ]-----

```
ReadNet      CON      $33          ' read OW net address
SkipNet      CON      $CC          ' skip OW net address
RdReg        CON      $69          ' read register
```

' -----[ Variables ]-----

```
idx          VAR      Nib          ' loop counter
type         VAR      Nib          ' device type
char         VAR      Byte         ' display byte/char

vIn          VAR      Word         ' in millivolts
tmpCJ        VAR      Word         ' device temp in C
tCuV         VAR      Word         ' thermocouple millivolts
sign         VAR      Word         ' TC sign bit

cjComp       VAR      Word         ' temp compensation
tempC        VAR      Word         ' temp in Celsius
tempF        VAR      Word         ' temp in Fahrenheit

tblLo        VAR      Word         ' table pointers
tblHi        VAR      Word
eePntr       VAR      Word
testVal      VAR      Word         ' test value from table
error        VAR      Bit         ' 1 = out of range
```

' -----[ EEPROM Data ]-----

' -----[ Initialization ]-----

Stamp\_Check:

```
#IF ($stamp < BS2P) #THEN
  #ERROR "This program requires BS2p or BS2pe"
#ENDIF
```

Check\_Device:

```
OWOUT OW, %0001, [ReadNet]      ' get serial number
OWIN  OW, %0010, [SPSTR 8]      ' store in SPRAM
GET idx, char                    ' read device type
IF (char <> $30) THEN           ' if not $30, wrong device
  DEBUG "No DS2760 found."
  STOP                          ' stop program
ENDIF
```

Menu:

```
DEBUG CLS,  
"-----", CR,  
" DS2760 Thermocouple Interface ", CR,  
"-----", CR,  
CR,  
"Select TC Type (1 - 3)", CR,  
CR,  
"(1) K - Chromel/Alumel", CR,  
"(2) J - Iron/Constantan", CR,  
"(3) T - Copper/Constantan", CR,  
CR,  
">>> "
```

```
DEBUGIN DEC1 type ' get selection  
IF (type < 1) OR (type > 3) THEN Menu ' validate selection  
DEBUG CRSRXY, 0, 3, CLRDN ' remove selections  
STORE type ' point READ to table
```

Show\_SN:

```
DEBUG CRSRXY, 0, 4, "Device SN... "  
FOR idx = 0 TO 7  
GET idx, char  
DEBUG HEX2 char  
NEXT
```

Show\_Type:

```
DEBUG CRSRXY, 0, 6, "TC Type..... "  
LOOKUP (type - 1), ["KJT"], char  
DEBUG char
```

' -----[ Program Code ]-----

Main:

```
DO  
GOSUB Read_TC_Volts ' read Seebeck voltage  
GOSUB Read_CJ_Temp ' read cold junction temp  
READ (tmpCJ * 2), Word cjComp ' get compensation voltage  
  
' combine cjComp and tCuV  
'  
IF sign THEN  
' TC below cold junction  
IF (tCuV < cjComp) THEN  
cjComp = cjComp - tCuV  
ELSE  
cjComp = 0 ' limit to 0C  
ENDIF
```

```

ELSE
  ' TC above cold junction
  cjComp = cjComp + tCuV
ENDIF

LOOKUP type, [1023, 1023, 400], tblHi      ' set high end of search
GOSUB TC_Lookup                            ' reverse lookup of table
tempF = tempC * 9 / 5 + 32                 ' x 1.8 + 32

IF (error = 0) THEN
  DEBUG CRSRXY, 0, 7,
    "Temp °C..... ", SDEC tempC, CLREOL
  DEBUG CRSRXY, 0, 8,
    "Temp °F..... ", SDEC tempF, CLREOL
ELSE
  DEBUG CRSRXY, 0, 7,
    "Temp °C..... Out of Range", CLREOL
  DEBUG CRSRXY, 0, 8,
    "Temp °F..... Out of Range", CLREOL
ENDIF

PAUSE 1000
LOOP
END

```

' -----[ Subroutines ]-----

```

' Reads device input voltage (Vin pin)
' -- mV in millivolts (max reading is 4.75 volts)

```

Read\_Vin:

```

OWOUT OW, %0001, [SkipNet, RdReg, $0C]
OWIN  OW, %0010, [vIn.BYTE1, vIn.BYTE0]
IF (vIn.BIT15) THEN                                ' check sign
  vIn = 0                                          ' disallow negative
ELSE
  vIn = vIn >> 5 */ $4E1                          ' x 4.88 millivolts
ENDIF
RETURN

```

```

' Reads current register to get TC voltage
' -- each raw bit = 15.625 uV
' -- tCuV in microvolts

```

Read\_TC\_Volts:

```

OWOUT OW, %0001, [SkipNet, RdReg, $0E]           ' read current register
OWIN  OW, %0010, [tCuV.BYTE1, tCuV.BYTE0]

```

```

sign = tCuV.BIT15           ' save sign bit
tCuV = tCuV >> 3           ' correct alignment
IF sign THEN
    tCuV = tCuV | $F000     ' pad 2's-compliment bits
ENDIF
tCuV = ABS tCuV */ 4000    ' x 15.625 uV
RETURN

```

```

' Reads cold junction (device) temperature
' -- each raw bit = 0.125 degrees C
' -- returns tmpCJ in whole degrees C

```

Read\_CJ\_Temp:

```

OWOUT OW, %0001, [SkipNet, RdReg, $18]
OWIN  OW, %0010, [tmpCJ.BYTE1, tmpCJ.BYTE0]
IF (tmpCJ.BIT15) THEN           ' check sign
    tmpCJ = 0                   ' disallow negative
ELSE
    tmpCJ = tmpCJ.HIGHBYTE      ' >> 5 x 0.125 (>> 3)
ENDIF
RETURN

```

```

' Search currently selected TC table for nearest entry
' -- uses modified binary algorithm to find cjComp
' -- high end of search set before calling (tblHi)
' -- successful search sets tempC

```

TC\_Lookup:

```

tblLo = 0                       ' low entry of table
tempC = 22                      ' default to room temp

READ (tblHi * 2), Word testVal   ' check max temp
IF (cjComp > testVal) THEN
    error = 1                   ' out of range
ELSE
    DO
        eePntr = (tblLo + tblHi) / 2           ' midpoint of search span
        READ (eePntr * 2), Word testVal       ' read value from midpoint

        IF (cjComp = testVal) THEN
            EXIT                               ' found it!
        ELSEIF (cjComp < testVal) THEN
            tblHi = eePntr                    ' search lower half
        ELSE
            tblLo = eePntr                    ' search upper half
        ENDIF
    END

```

```

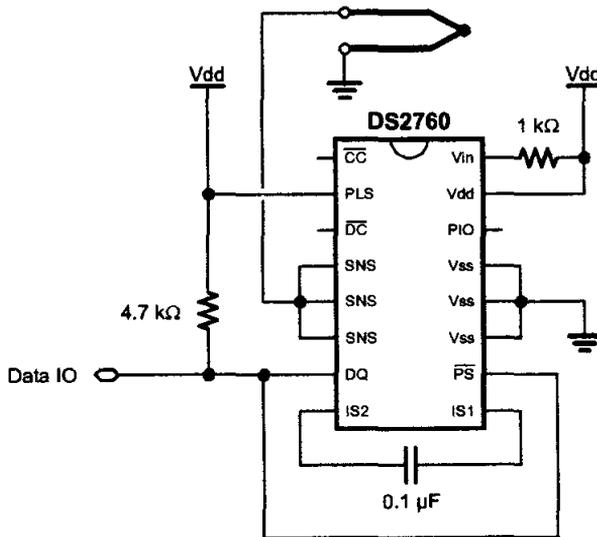
IF ((tblHi - tblLo) < 2) THEN           ' span at minimum
    eePntr = tblLo
    EXIT
ENDIF
LOOP
tempC = eePntr
ENDIF
RETURN

```

## Additional Resources

- Advanced thermocouple interface software (download from Parallax)
- Web Links:
  - [www.maxim-ic.com/quick\\_view2.cfm/qv\\_pk/2931](http://www.maxim-ic.com/quick_view2.cfm/qv_pk/2931)
  - [www.capgo.com/Resources/Sensors/Temperature/Thermocouple/Thermocouple.html](http://www.capgo.com/Resources/Sensors/Temperature/Thermocouple/Thermocouple.html)
  - [instserv.com/rmocoupl.htm](http://instserv.com/rmocoupl.htm)
  - [instrumentation-central.com/pages/thermocouple\\_reference\\_table.htm](http://instrumentation-central.com/pages/thermocouple_reference_table.htm)

## DS2760 Module Schematic



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