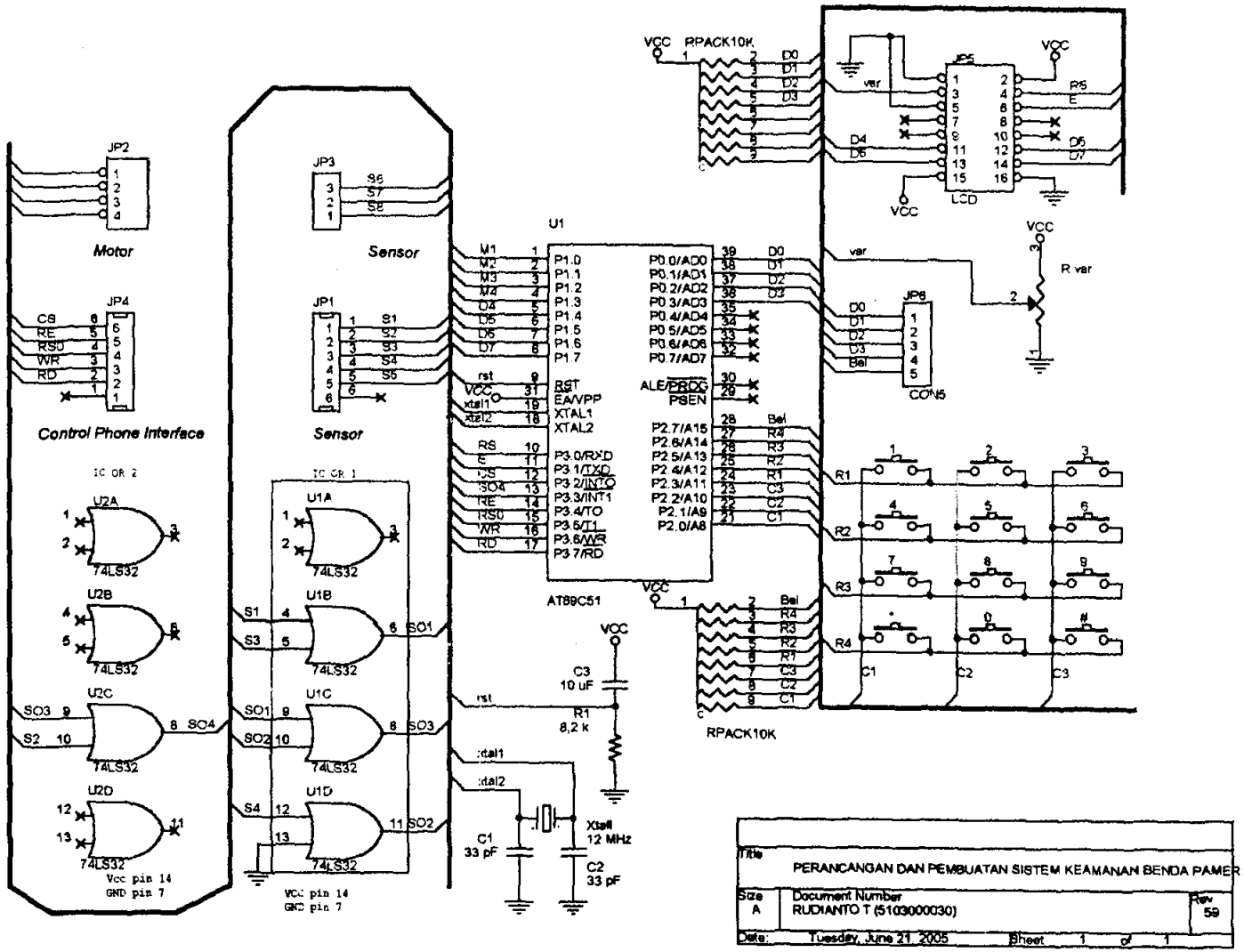
LAMPIRAN

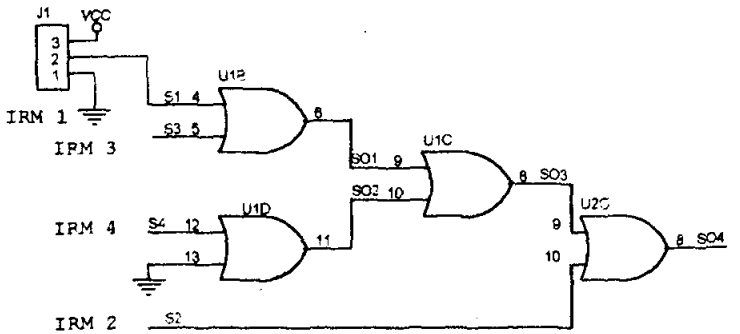
LAMPIRAN A

SKEMA RANGKAIAN

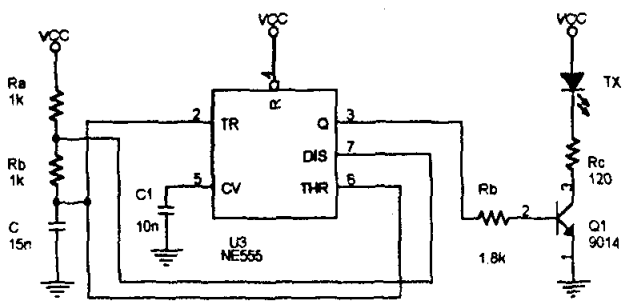


Title	PERANCANGAN DAN PEMBUATAN SISTEM KEAMANAN BENDA PAMER	
Size: A	Document Number: RUDIANTO T (5103000030)	Rev: 59
Date: Tuesday, June 21, 2005	Sheet 1 of 1	

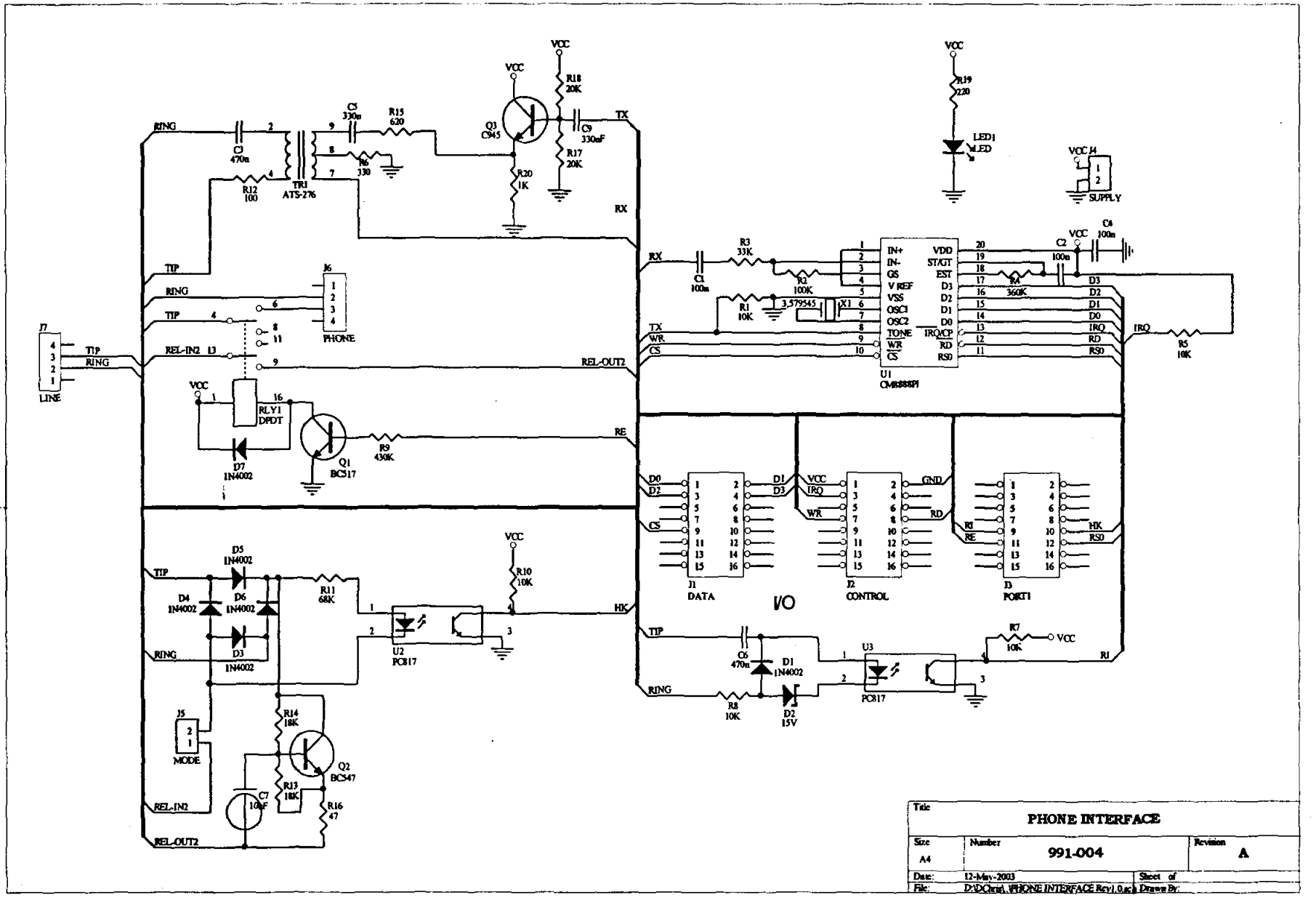
Rangkaian penerima infra merah



Rangkaian pemancar infra merah



Title	RANGKAIAN SENSOR INFRA MERAH		
Size A	Document Number <Doc>		Rev <RevCode>
Date	Tuesday, June 21, 2005	Sheet 1 of 1	


VCC
RING
TIP
RX
TX
REL-IN2
REL-OUT2
RE
HK
RI
IRQ
WR
RD
CS
D0
D1
D2
D3
RS0
GND
MODE
LINE
PHONE
SUPPLY
LED1
RLY1
DPDT
TR1
ATS-276
Q1
BC517
Q2
BC547
Q3
C945
U1
CM8888PI
U2
PC817
U3
PC817
D1
1N4002
D2
15V
D3
1N4002
D4
1N4002
D5
1N4002
D6
1N4002
D7
1N4002
J1
DATA
J2
CONTROL
J3
PORT1
I/O
R1
10K
R2
100K
R3
33K
R4
360K
R5
10K
R6
330
R7
10K
R8
10K
R9
430K
R10
10K
R11
68K
R12
100
R13
18K
R14
18K
R15
620
R16
47
R17
20K
R18
20K
R19
220
R20
1K
C1
100n
C2
100n
C3
470n
C4
100n
C5
330n
C6
470n
C7
10nF
C9
330nF
X1
3.579545
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PHONE INTERFACE
Size
A4
Number
991-004
Revision
A
Date:
12-May-2003
Sheet of
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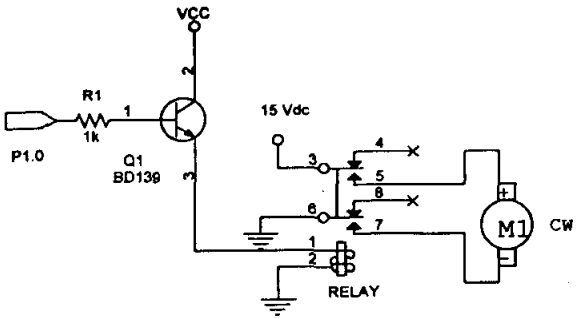
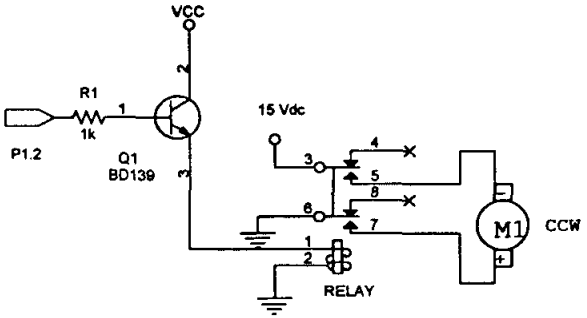
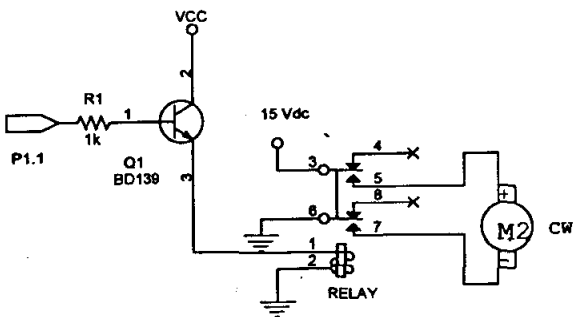
D:\DCircuit\PHONE INTERFACE Rev1.0.sch
Drawn By:



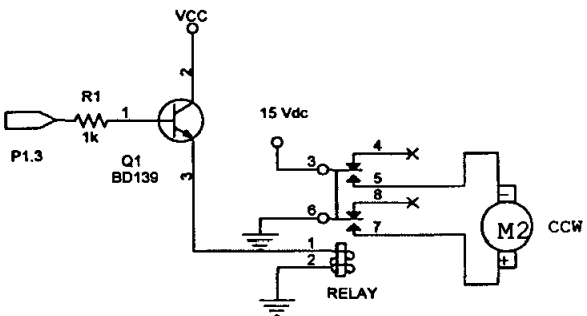
menurunkan tempat benda pamer



menaikkan tempat benda pamer

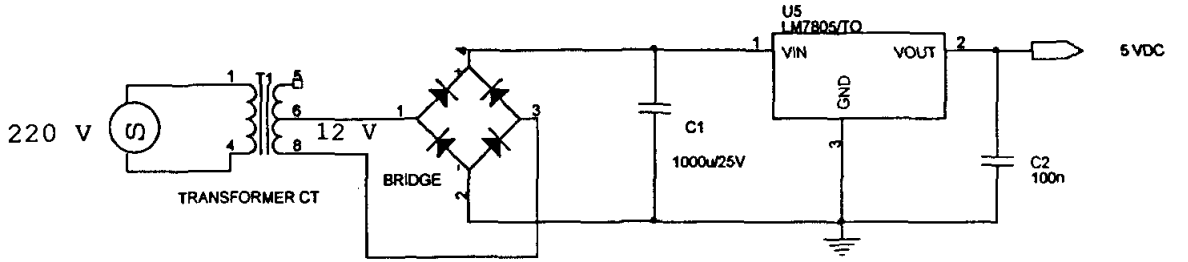


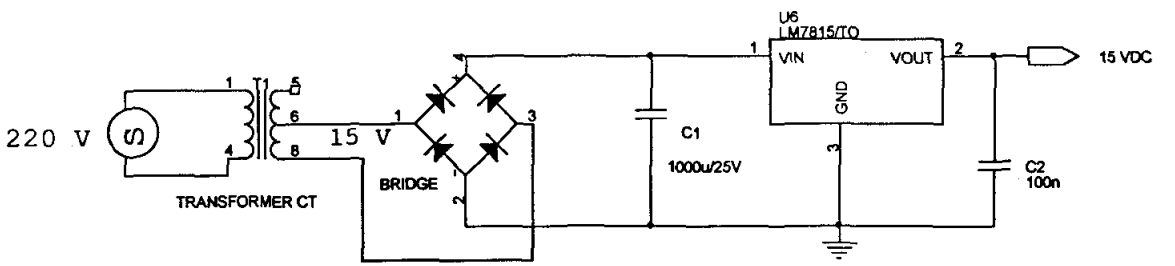
menutup benda pamer



membuka penutup benda pamer

Title: RANGKAIAN DRIVER MOTOR DC		
Size: A	Document Number: RUDIANTO T (5103000030)	Rev
Date: Tuesday, June 21, 2005	Sheet 1 of 1	





Title: RANGKAIAN POWER SUPPLY		
Size: A	Document Number: RUDIANTO T (5103000030)	Rev: <RevCode>
Date: Tuesday, June 28, 2005	Sheet 1 of 1	

LAMPIRAN B

LISTING PROGRAM

```
$MOD51

ORG  0000H
AJMP RESET

MT8888          EQU  0000H
DTMF1           EQU  0DH
DIGIT           EQU  31H
PASS            EQU  50H
COMP            EQU  60H
FIXED           EQU  70H

BUZZ            BIT  P2.7
RS              BIT  P3.0
E               BIT  P3.1
CS8888          BIT  P3.2
RE              BIT  P3.4
RS0X            BIT  P3.5

PESAN0:     DB 'INPUT PASSWORD  ',0FH
PESAN1:     DB 'INPUT TELP NO   ',0FH
PESAN2:     DB 'AGREE?1=NO 2=YES',0FH
PESAN3:     DB '--->CHECKING<---',0FH
PESAN4:     DB ' ALARM ACTIVATE ',0FH
PESAN5:     DB 'VERIFY PASSWORD',0FH
PESAN6:     DB 'SET PASS 1=Y 2=N',0FH

DSEG   AT 30H
MODE:  DS      1

CSEG
;++++++++++++++++++++++++++++++++++++++++++++

RESET:
MOV    P1,#0H              ;MATIKAN MOTOR DC
MOV    P2,#0H              ;MATIKAN BUZZER
MOV    SP,#40H             ;STACK POINTER PADA 40H
LCALL  RESET8888           ;RESET MT8888
MOV    MODE,#DTMF1         ;PINDAH DATA 0DH UNTUK
                            INISIALISASI MT8888
LCALL  INIT8888            ;INISIALISASI MT8888
LCALL  INIT_LCD
LCALL  PASSWORD
AJMP   NOMOR
```

```
;--------------------------------------
;PROSEDUR PASSWORD
;--------------------------------------
PASSWORD:
MOV       A,#01H              ;DISPLAY CLEAR
ACALL     KIRIM_PERINTAH
MOV       DPTR,#PESAN0        ;TAMPILKAN PESAN 0
ACALL     KIRIMPESAN_LCD
MOV       A,#0C0H             ; BARIS 2  LCD AKTIF
ACALL     KIRIM_PERINTAH
MOV       PASS,#51H

CEK_PASS:
MOV       DIGIT,#00H
ACALL     SCAN_KEY             ;CEK PENEKANAN TOMBOL
MOV       A,DIGIT
CJNE      A,#00H,PASS1
AJMP      CEK_PASS

PASS1:
CJNE      A,#23H,PASS2         ;TOMBOL # DITEKAN ?
MOV       R1,PASS
MOV       @R1,#'$'             ;ISI PASSWORD SELESAI
RET

PASS2:
MOV       A,#2AH               ;TAMPILKAN * PADA LCD
ACALL     KIRIM_KARAKTER       ;KIRIM KE LCD
MOV       A,DIGIT
SWAP      A
MOV       R1,PASS
MOV       @R1,A
INC       50H
AJMP      CEK_PASS

;--------------------------------------
; PROSEDUR MASUKKAN NOMOR
;--------------------------------------
NOMOR:
MOV       FIXED,#71H
MOV       A,#01H               ;DISPLAY CLEAR
ACALL     KIRIM_PERINTAH
MOV       DPTR,#PESAN1         ;TAMPILKAN PESAN 1
ACALL     KIRIMPESAN_LCD
MOV       A,#0C0H              ;BARIS 2 LCD AKTIF
ACALL     KIRIM_PERINTAH
```

```
CEK_NO:
MOV         DIGIT,#00H
ACALL       SCAN_KEY
MOV         A,DIGIT
CJNE        A,#00H,CEK1
AJMP        CEK_NO

CEK1:
CJNE        A,#23H,CEK2             ;TOMBOL # DITEKAN?
MOV         R1,FIXED
MOV         @R1,#'$'                ;ISI NOMOR SELESAI
AJMP        STARTD

CEK2:
MOV         A,DIGIT                 ;ISI AKUMULATOR=ISI DIGIT
ACALL       KIRIM_KARAKTER          ;TAMPILKAN DI LCD
MOV         R1,FIXED
MOV         @R1,DIGIT
INC         70H
AJMP        CEK_NO

;---------------------------------------
; CONFIRM PHONE NUMBER
;---------------------------------------

STARTD:
MOV         A,#80H                  ;AKTIFKAN BARIS 1 LCD
ACALL       KIRIM_PERINTAH
MOV         DPTR,#PESAN2            ;TAMPILKAN PESAN 2
ACALL       KIRIMPESAN_LCD

TANYA1:
MOV         DIGIT,#00H
ACALL       SCAN_KEY
MOV         A,DIGIT
CJNE        A,#31H,TANYA2           ;1 DITEKAN ?
AJMP        NOMOR                   ;UBAH NOMOR TELEPON

TANYA2:
CJNE        A,#32H,TANYA1           ;2 DITEKAN?

PROSES:
MOV         A,#01H                  ;DISPLAY CLEAR
ACALL       KIRIM_PERINTAH
MOV         DPTR,#PESAN3            ;TAMPILKAN PESAN 3
ACALL       KIRIMPESAN_LCD
```

```
SETB            P3.3            ;P3.3 = INPUT SENSOR
NOP
NOP

;---------------------------------------
;RED ALERT
;---------------------------------------
JNB         P3.3,$              ;SENSOR TERHALANG?

RED_ALERT:
MOV         A,#01H              ;CLEAR LCD
ACALL       KIRIM_PERINTAH
MOV         DPTR,#PESAN4
ACALL       KIRIMPESAN_LCD
SETB        BUZZ                ;BUZZER ON
SETB        P1.0                ;TEMPAT BARANG TURUN
ACALL       DELAY2S
ACALL       DELAY2S
CLR         P1.0
SETB        P1.1                ;TUTUP DAERAH UTAMA
ACALL       DELAY_3S
ACALL       DELAY500MS
CLR         P1.1

;---------------------------------------
;DIALING NUMBER
;---------------------------------------
SETB        RE                  ;ANGKAT GAGANG TELEPON
ACALL       DELAY_3S
ACALL       DTMFDIALING         ;MELAKUKAN DTMF DIALING
ACALL       DELAY2S
ACALL       DELAY2S
ACALL       DELAY2S
ACALL       DELAY2S
ACALL       DELAY2S
CLR         BUZZ                ;BUZZER OFF
CLR         RE                  ;TUTUP GAGANG

;---------------------------------------
;CONFIRM PASSWORD
;---------------------------------------
CONF:
MOV         A,#01H              ;DISPLAY CLEAR
ACALL       KIRIM_PERINTAH
MOV         DPTR,#PESAN5        ;TAMPILKAN PESAN 5
ACALL       KIRIMPESAN_LCD
```

```
MOV         A,#0C0H             ;BARIS 2  LCD AKTIF
ACALL       KIRIM_PERINTAH
MOV         COMP,#61H

CEK_CONF:
MOV         DIGIT,#00H
ACALL       SCAN_KEY
MOV         A,DIGIT
CJNE        A,#00H,CONF1
AJMP        CEK_CONF

CONF1:
CJNE        A,#23H,CONF2        ;TOMBOL # DITEKAN?
MOV         R1,COMP
MOV         @R1,#'$'
AJMP        VER                 ;PERIKSA PASSWORD

CONF2:
MOV         A,#2AH              ;TAMPILKAN * PADA LCD
ACALL       KIRIM_KARAKTER
MOV         A,DIGIT
SWAP        A
MOV         R1,COMP
MOV         @R1,A
INC         60H
AJMP        CEK_CONF

;---------------------------------------
;PASSWORD VERIFY
;---------------------------------------
VER:
MOV         PASS,#51H
MOV         COMP,#61H

CEK_VER:
MOV         R1,COMP             ;COMP->A
MOV         A,@R1
MOV         R1,PASS             ;PASS->B
MOV         B,@R1

CJNE        A,B,CONF            ;A = B ?

INC         50H                 ;AMBIL DATA BERIKUTNYA
INC         60H                 ;AMBIL DATA BERIKUTNYA
CJNE        A,#'$',CEK_VER      ;DATA DI COMP HABIS?
MOV         A,B
CJNE        A,#'$',CONF         ;DATA DI PASS HABIS?
```

```
;--------------------------------------
;CHANGE PASSWORD
;--------------------------------------
CHANGE:
MOV       A,#01H                    ;CLEAR_LCD
ACALL     KIRIM_PERINTAH

MOV       DPTR,#PESAN6
ACALL     KIRIMPESAN_LCD

CH1:
MOV       DIGIT,#00H
ACALL     SCAN_KEY
MOV       A,DIGIT

CJNE      A,#31H,CH2
AJMP      CH3

CH2:
CJNE      A,#32H,CH1
AJMP      COMPLETE

CH3:
LCALL    PASSWORD

;--------------------------------------
;PASSWORD CHANGE COMPLETE
;--------------------------------------
COMPLETE:
SETB      P1.3                   ;BUKA DAERAH UTAMA
ACALL     DELAY_3S
CLR       P1.3
SETB      P1.2                   ;TEMPAT BARANG NAIK
ACALL     DELAY2S
ACALL     DELAY2S
ACALL     DELAY500MS
CLR       P1.2
AJMP      PROSES                ;KEMBALI PERIKSA SENSOR

;--------------------------------------
;WRITE DTMF
;DIAMBIL DARI TUTORIAL PHONE INTERFACE
;--------------------------------------
WRITEDTMF:
PUSH      DPH
PUSH      DPL
CLR       RS0X                    ;RS0=0
```

```
MOV         DPTR,#MT8888
MOVX        @DPTR,A
POP         DPL
POP         DPH
RET

;----------------------------------------
;READ STATUS MT8888
;DIAMBIL DARI TUTORIAL PHONE INTERFACE
;----------------------------------------
READSTAT:
PUSH        DPH
PUSH        DPL
SETB        RS0X                        ;RS0=1
MOV         DPTR,#MT8888
MOVX        A,@DPTR
CLR         RS0X                      ;RS0=0
POP         DPL
POP         DPH
RET

;-------------------------------------
;WRITE CONTROL REGISTER
;DIAMBIL DARI TUTORIAL PHONE INTERFACE
;-------------------------------------
WRITECR:
PUSH        DPH
PUSH        DPL
SETB        RS0X                    ;RS0=1
MOV         DPTR,#MT8888
MOVX        @DPTR,A
CLR         RS0X                    ;RS0=0
POP         DPL
POP         DPH
RET

;----------------------------------------
;RESET MT8888
;DIAMBIL DARI TUTORIAL PHONE INTERFACE
;----------------------------------------
RESET8888:
PUSH        ACC
CLR         CS8888
CLR         RE
ACALL       READSTAT
MOV         A,#00H
ACALL       WRITECR
```

```
ACALL     WRITECR
MOV       A,#08H
ACALL     WRITECR
MOV       A,#00H
ACALL     WRITECR
ACALL     READSTAT
POP       ACC
RET

;----------------------------------------
;INIT MT8888
;DIAMBIL DARI TUTORIAL PHONE INTERFACE
;----------------------------------------
INIT8888:
PUSH      ACC
PUSH      DPH
PUSH      DPL
MOV       A,MODE
ACALL     WRITECR
JNB       ACC.3,EO_INIT8888
SWAP      A
ACALL     WRITECR

EO_INIT8888:
POP       DPL
POP       DPH
POP       ACC
RET

;-----------------------------------------------
;DTMF DIALING NUMBER
;DIAMBIL DARI TUTORIAL PHONE INTERFACE
;DENGAN MODIFIKASI PADA PROSES PENGIRIMAN DATA
;-----------------------------------------------
DTMFDIALING:
MOV       FIXED,#71H

NXTNUMBER:
MOV       R1,FIXED
MOV       A,@R1
CJNE      A,#'$',DIAL
RET

DIAL:
INC       70H
CJNE      A,#30H,DIAL19
```

```
DIAL0:
MOV         A,#0AH
ACALL       WRITEDTMF
UP1:
ACALL       READSTAT
JNB         ACC.1,UP1
AJMP        NXTNUMBER

DIAL19:
ACALL       WRITEDTMF
UP2:
ACALL       READSTAT
JNB         ACC.1,UP2
AJMP        NXTNUMBER

;++++++++++++++++++++++++++++++++++++++++++++
;     PROSEDUR SCAN KEYPAD
;++++++++++++++++++++++++++++++++++++++++++++
SCAN_KEY:

KOLOM1:     PUSH    80H             ;SAVE LOGIC P2.7
            MOV     A,#7EH
            MOV     P2,A
            ACALL   DELAY_15MS
            MOV     A,P2
            ACALL   DELAY_15MS
            CJNE    A,#7EH,ANGKA1
            AJMP    KOLOM2

ANGKA1:     CJNE    A,#76H,ANGKA4
            MOV     A,#31H
            MOV     DIGIT,A
            ACALL   DELAY_065S
            AJMP    OUT_KEY

ANGKA4:     CJNE    A,#6EH,ANGKA7
            MOV     A,#34H
            MOV     DIGIT,A
            ACALL   DELAY_065S
            AJMP    OUT_KEY

ANGKA7:     CJNE    A,#5EH,ANGKA11
            MOV     A,#37H
            MOV     DIGIT,A
            ACALL   DELAY_065S
            AJMP    OUT_KEY
```

```
ANGKA11:  MOV     A,#2AH
          MOV     DIGIT,A
          ACALL   DELAY_065S
          AJMP    OUT_KEY

KOLOM2:   MOV     A,#7DH
          MOV     P2,A
          ACALL   DELAY_15MS
          MOV     A,P2
          ACALL   DELAY_15MS
          CJNE    A,#7DH,ANGKA2
          AJMP    KOLOM3

ANGKA2:   CJNE    A,#75H,ANGKA5
          MOV     A,#32H
          MOV     DIGIT,A
          ACALL   DELAY_065S
          AJMP    OUT_KEY

ANGKA5:   CJNE    A,#6DH,ANGKA8
          MOV     A,#35H
          MOV     DIGIT,A
          ACALL   DELAY_065S
          AJMP    OUT_KEY

ANGKA8:   CJNE    A,#5DH,ANGKA0
          MOV     A,#38H
          MOV     DIGIT,A
          ACALL   DELAY_065S
          AJMP    OUT_KEY

ANGKA0:   MOV     A,#30H
          MOV     DIGIT,A
          ACALL   DELAY_065S
          AJMP    OUT_KEY

KOLOM3:   MOV     A,#7BH
          MOV     P2,A
          ACALL   DELAY_15MS
          MOV     A,P2
          ACALL   DELAY_15MS
          CJNE    A,#7BH,ANGKA3
          AJMP    OUT_KEY
```

```
ANGKA3:   CJNE   A,#73H,ANGKA6
          MOV    A,#33H
          MOV    DIGIT,A
          ACALL  DELAY_065S
          AJMP   OUT_KEY

ANGKA6:   CJNE   A,#6BH,ANGKA9
          MOV    A,#36H
          MOV    DIGIT,A
          ACALL  DELAY_065S
          AJMP   OUT_KEY

ANGKA9:   CJNE   A,#5BH,ANGKA12
          MOV    A,#39H
          MOV    DIGIT,A
          ACALL  DELAY_065S
          AJMP   OUT_KEY

ANGKA12:  MOV    A,#23H
          MOV    DIGIT,A
          ACALL  DELAY_065S
          AJMP   OUT_KEY

OUT_KEY:  POP  80H
          RET

;++++++++++++++++++++++++++++++++++++++++++++
;     PROSEDUR INISIALISASI LCD
;++++++++++++++++++++++++++++++++++++++++++++
INIT_LCD:
MOV       A,#30H
ACALL     KIRIM_PERINTAH
MOV       A,#30H
ACALL     KIRIM_PERINTAH
MOV       A,#30H
ACALL     KIRIM_PERINTAH
MOV       A,#20H
ACALL     KIRIM_PERINTAH
MOV       A,#28H              ;FUNCTION SET
ACALL     KIRIM_PERINTAH
MOV       A,#06H              ;ENTRY MODE SET
ACALL     KIRIM_PERINTAH
MOV       A,#0CH              ;DISPLAY ON
ACALL     KIRIM_PERINTAH
MOV       A,#01H              ;DISPLAY CLEAR
ACALL     KIRIM_PERINTAH
RET
```

```
KIRIM_PERINTAH:
CLR         RS
ACALL       KIRIM_DATALCD
SWAP        A
ACALL       KIRIM_DATALCD
ACALL       DELAY_4MS
RET

KIRIM_DATALCD:
PUSH        ACC
ANL         A,#0F0H
MOV         R2,A
MOV         A,P1
ANL         A,#0FH
ORL         A,R2
MOV         P1,A
SETB        E
CLR         E
POP         ACC
RET

KIRIMPESAN_LCD:

LOOPKIRIMPESAN:
MOV         A,#00H
MOVC        A,@A+DPTR
CJNE        A,#0FH,KIRIM_LCD
RET

KIRIM_LCD:  ACALL     KIRIM_KARAKTER
            INC DPTR
            AJMP      LOOPKIRIMPESAN

KIRIM_KARAKTER:
SETB        RS
ACALL       KIRIM_DATALCD
SWAP        A
ACALL       KIRIM_DATALCD
ACALL       DELAY_50US
RET
```

```
;++++++++++++++++++++++++++++++++++++++++++++
;     PROSEDUR DELAY
;++++++++++++++++++++++++++++++++++++++++++++
DELAY2S:   PUSH 05H
           PUSH 06H
           PUSH 07H
           MOV  R5,#20
LDEL2S_2: MOV  R6,#200
LDEL2S_1: MOV  R7,#250

           DJNZ R7,$
           DJNZ R6,LDEL2S_1
           DJNZ R5,LDEL2S_2
           POP  07H
           POP  06H
           POP  05H
           RET

DELAY_4MS:      MOV  R0,#0FFH
                MOV  R1,#10H
DELAY_4MS1:     DJNZ R0,DELAY_4MS1
                DJNZ R1,DELAY_4MS1
                RET

DELAY_50US:     MOV  R0,#12H
                MOV  R1,#02H
DELAY_50US1:    DJNZ R0,DELAY_50US1
                DJNZ R1,DELAY_50US1
                RET

DELAY_15MS:     MOV  R0,#0FFH
                MOV  R1,#2FH
DELAY_15MS1:    DJNZ R0,DELAY_15MS1
                DJNZ R1,DELAY_15MS1
                RET

DELAY500MS:  MOV R2,#04H
D5:          MOV R0,#0FFH
D51:         MOV R1,#0FFH
             DJNZ R1,$
             DJNZ R0,D51
             DJNZ R2,D5
             NOP
             RET
```

```
DELAY_1S: MOV   R0,#62H
LOP:      MOV   R1,#68H
LOP1:     MOV   R2,#32H
HERE:     DJNZ  R2,$
          DJNZ  R1,LOP1
          DJNZ  R0,LOP
          RET

DELAY_3S: ACALL     DELAY_1S
          ACALL     DELAY_1S
          ACALL     DELAY_1S
          RET


DELAY_200MS: MOV    R7,#14
AGAIN:       ACALL  DELAY_15MS
             DJNZ   R7,AGAIN
             RET


DELAY_065S:    MOV  R0,#5H          ;DELAY 0,65S
TNDA1:         MOV  R1,#0FFH
TNDA2:         MOV  R2,#0H
               DJNZ R2,$
               DJNZ R1,TNDA2
               DJNZ R0,TNDA1
               RET

END
```

LAMPIRAN C

DATA SHEET

Features

- Compatible with MCS-51™ Products
- 4K Bytes of In-System Reprogrammable Flash Memory
  - *Endurance: 1,000 Write/Erase Cycles*
- Fully Static Operation: 0 Hz to 24 MHz
- Three-Level Program Memory Lock
- 128 x 8-Bit Internal RAM
- 32 Programmable I/O Lines
- Two 16-Bit Timer/Counters
- Six Interrupt Sources
- Programmable Serial Channel
- Low Power Idle and Power Down Modes

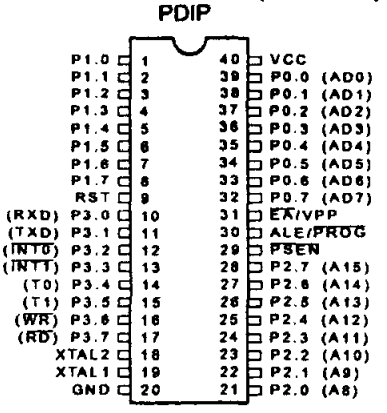
Description

The AT89C51 is a low-power, high-performance CMOS 8-bit microcomputer with 4K bytes of Flash Programmable and Erasable Read Only Memory (PEROM). The device is manufactured using Atmel's high density nonvolatile memory technology and is compatible with the industry standard MCS-51™ instruction set and pinout. The on-chip Flash allows the program memory to be reprogrammed in-system or by a conventional nonvolatile memory programmer. By combining a versatile 8-bit CPU with Flash on a monolithic chip, the Atmel AT89C51 is a powerful microcomputer which provides a highly flexible and cost effective solution to many embedded control applications.

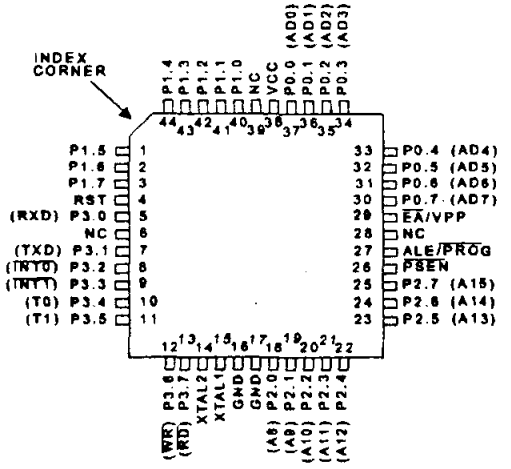
(continued)

Pin Configurations

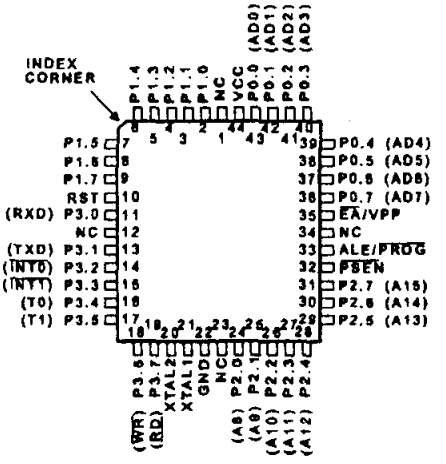
PDIP



PQFP/TQFP



PLCC

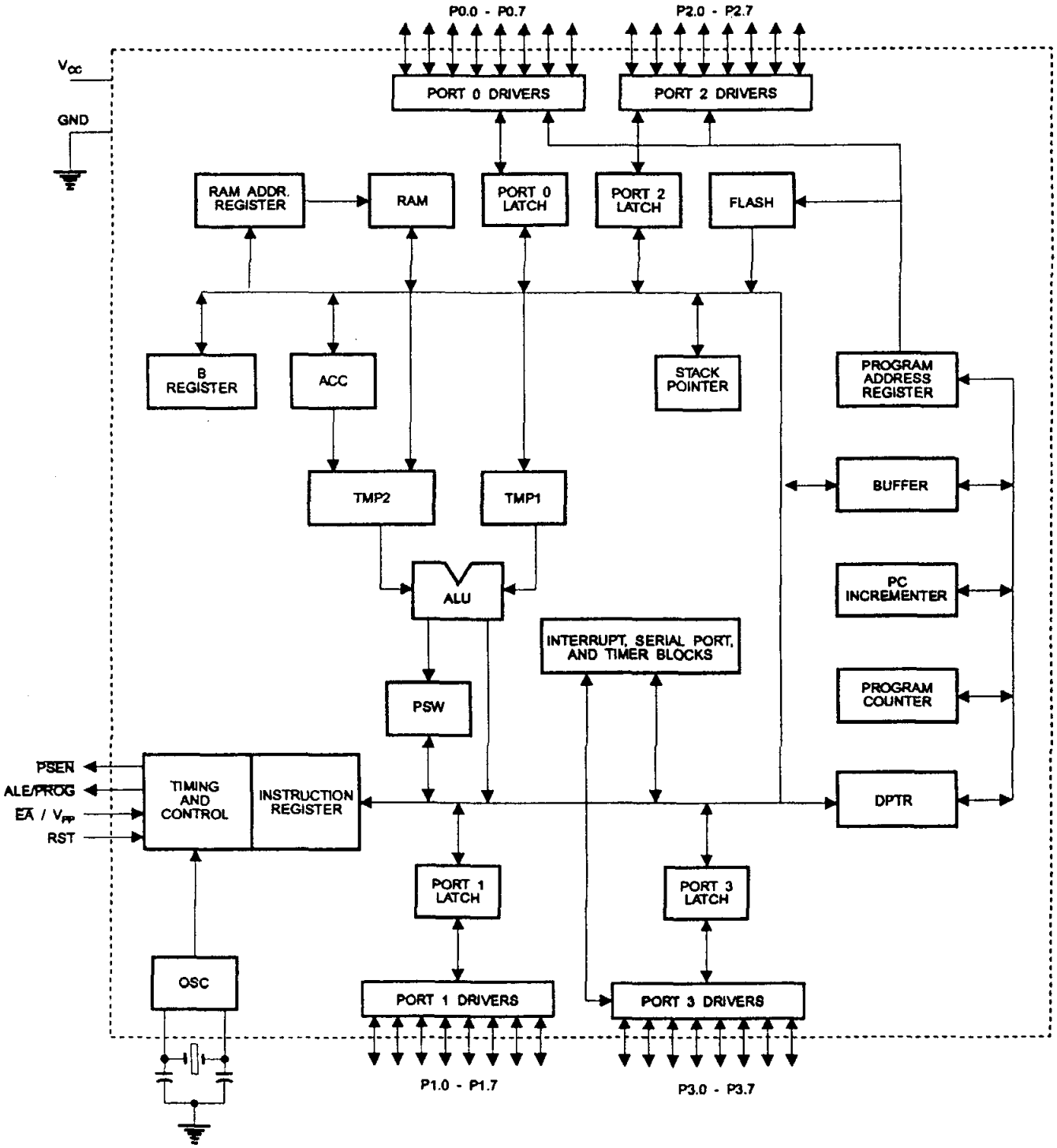


8-Bit Microcontroller with 4K Bytes Flash

AT89C51

0265F-A-12/97

lock Diagram



The AT89C51 provides the following standard features: 4K bytes of Flash, 128 bytes of RAM, 32 I/O lines, two 16-bit timer/counters, a five vector two-level interrupt architecture, a full duplex serial port, on-chip oscillator and clock circuitry. In addition, the AT89C51 is designed with static logic for operation down to zero frequency and supports two software selectable power saving modes. The Idle Mode stops the CPU while allowing the RAM, timer/counters, serial port and interrupt system to continue functioning. The Power Down Mode saves the RAM contents but freezes the oscillator disabling all other chip functions until the next hardware reset.

Pin Description

V_{CC}
Supply voltage.

GND
Ground.

Port 0
Port 0 is an 8-bit open drain bidirectional I/O port. As an output port each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high-impedance inputs.

Port 0 may also be configured to be the multiplexed low-order address/data bus during accesses to external program and data memory. In this mode P0 has internal pullups.

Port 0 also receives the code bytes during Flash programming, and outputs the code bytes during program verification. External pullups are required during program verification.

Port 1
Port 1 is an 8-bit bidirectional I/O port with internal pullups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}) because of the internal pullups.

Port 1 also receives the low-order address bytes during Flash programming and verification.

Port 2
Port 2 is an 8-bit bidirectional I/O port with internal pullups. The Port 2 output buffers can sink/source four TTL inputs. When 1s are written to Port 2 pins they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL}) because of the internal pullups.

Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application it uses strong internal pullups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

Port 3
Port 3 is an 8-bit bidirectional I/O port with internal pullups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}) because of the pullups.

Port 3 also serves the functions of various special features of the AT89C51 as listed below:

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

Port 3 also receives some control signals for Flash programming and verification.

RST
Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device.

ALE/$\overline{PROG}$
Address Latch Enable output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input ($\overline{PROG}$) during Flash programming.

In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external Data Memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

$\overline{PSEN}$
Program Store Enable is the read strobe to external program memory.

When the AT89C51 is executing code from external program memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external data memory.

$\overline{EA}$/V_{PP}
External Access Enable. $\overline{EA}$ must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed, $\overline{EA}$ will be internally latched on reset.

$\overline{EA}$ should be strapped to V_{CC} for internal program executions.

This pin also receives the 12-volt programming enable voltage (V_{PP}) during Flash programming, for parts that require 12-volt V_{PP}.

XTAL1
Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

XTAL2
Output from the inverting oscillator amplifier.

Oscillator Characteristics

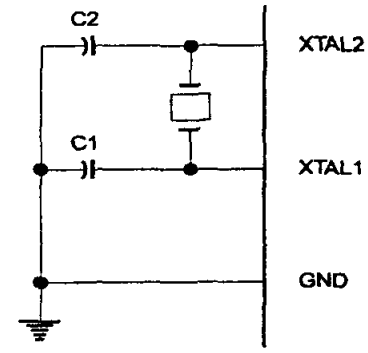
XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier which can be configured for use as an on-chip oscillator, as shown in Figure 1. Either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven as shown in Figure 2. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

Idle Mode

In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special functions registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

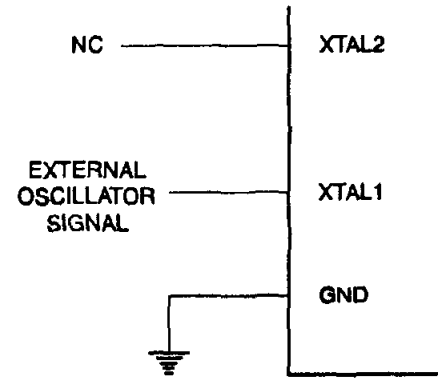
It should be noted that when idle is terminated by a hard ware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.

Figure 1. Oscillator Connections



Note: C1, C2 = 30 pF ± 10 pF for Crystals
= 40 pF ± 10 pF for Ceramic Resonators

Figure 2. External Clock Drive Configuration



Status of External Pins During Idle and Power Down Modes

Mode	Program Memory	ALE	$\overline{PSEN}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power Down	Internal	0	0	Data	Data	Data	Data
Power Down	External	0	0	Float	Data	Data	Data

Power Down Mode

In the power down mode the oscillator is stopped, and the instruction that invokes power down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the power down mode is terminated. The only exit from power down is a hardware reset. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

Program Memory Lock Bits

On the chip are three lock bits which can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in the table below:

When lock bit 1 is programmed, the logic level at the $\overline{EA}$ pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value, and holds that value until reset is activated. It is necessary that the latched value of $\overline{EA}$ be in agreement with the current logic level at that pin in order for the device to function properly.

Lock Bit Protection Modes

Program Lock Bits				Protection Type
	LB1	LB2	LB3	
1	U	U	U	No program lock features.
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, $\overline{EA}$ is sampled and latched on reset, and further programming of the Flash is disabled.
3	P	P	U	Same as mode 2, also verify is disabled.
4	P	P	P	Same as mode 3, also external execution is disabled.

Programming the Flash

The AT89C51 is normally shipped with the on-chip Flash memory array in the erased state (that is, contents = FFH) and ready to be programmed. The programming interface accepts either a high-voltage (12-volt) or a low-voltage (V_{CC}) program enable signal. The low voltage programming mode provides a convenient way to program the AT89C51 inside the user's system, while the high-voltage programming mode is compatible with conventional third party Flash or EPROM programmers.

The AT89C51 is shipped with either the high-voltage or low-voltage programming mode enabled. The respective top-side marking and device signature codes are listed in the following table.

	V_{PP} = 12V	V_{PP} = 5V
Top-Side Mark	AT89C51 xxxx yyww	AT89C51 xxxx-5 yyww
Signature	(030H)=1EH (031H)=51H (032H)=FFH	(030H)=1EH (031H)=51H (032H)=05H

The AT89C51 code memory array is programmed byte-by-byte in either programming mode. *To program any non-blank byte in the on-chip Flash Memory, the entire memory must be erased using the Chip Erase Mode.*

Programming Algorithm: Before programming the AT89C51, the address, data and control signals should be set up according to the Flash programming mode table and Figures 3 and 4. To program the AT89C51, take the following steps.

1. Input the desired memory location on the address lines.
2. Input the appropriate data byte on the data lines.
3. Activate the correct combination of control signals.
4. Raise $\overline{EA}/V_{PP}$ to 12V for the high-voltage programming mode.
5. Pulse ALE/$\overline{PROG}$ once to program a byte in the Flash array or the lock bits. The byte-write cycle is self-timed and typically takes no more than 1.5 ms. Repeat steps 1 through 5, changing the address and data for the entire array or until the end of the object file is reached.

$\overline{Data}$ Polling: The AT89C51 features $\overline{Data}$ Polling to indicate the end of a write cycle. During a write cycle, an attempted read of the last byte written will result in the complement of the written datum on PO.7. Once the write cycle has been completed, true data are valid on all outputs, and the next cycle may begin. $\overline{Data}$ Polling may begin any time after a write cycle has been initiated.

Ready/$\overline{Busy}$: The progress of byte programming can also be monitored by the RDY/$\overline{BSY}$ output signal. P3.4 is pulled low after ALE goes high during programming to indicate BUSY. P3.4 is pulled high again when programming is done to indicate READY.

Program Verify: If lock bits LB1 and LB2 have not been programmed, the programmed code data can be read back via the address and data lines for verification. The lock bits cannot be verified directly. Verification of the lock bits is achieved by observing that their features are enabled.

Chip Erase: The entire Flash array is erased electrically by using the proper combination of control signals and by holding ALE/$\overline{PROG}$ low for 10 ms. The code array is written with all "1"s. The chip erase operation must be executed before the code memory can be re-programmed.

Reading the Signature Bytes: The signature bytes are read by the same procedure as a normal verification of locations 030H,

031H, and 032H, except that P3.6 and P3.7 must be pulled to a logic low. The values returned are as follows.

(030H) = 1EH indicates manufactured by Atmel
(031H) = 51H indicates 89C51
(032H) = FFH indicates 12V programming
(032H) = 05H indicates 5V programming

Programming Interface

Every code byte in the Flash array can be written and the entire array can be erased by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

All major programming vendors offer worldwide support for the Atmel microcontroller series. Please contact your local programming vendor for the appropriate software revision.

Flash Programming Modes

Mode		RST	$\overline{PSEN}$	ALE/$\overline{PROG}$	$\overline{EA}$/V_{PP}	P2.6	P2.7	P3.6	P3.7
Write Code Data		H	L		H/12V	L	H	H	H
Read Code Data		H	L	H	H	L	L	H	H
Write Lock	Bit - 1	H	L		H/12V	H	H	H	H
	Bit - 2	H	L		H/12V	H	H	L	L
	Bit - 3	H	L		H/12V	H	L	H	L
Chip Erase		H	L	 (1)	H/12V	H	L	L	L
Read Signature Byte		H	L	H	H	L	L	L	L

Note: 1. Chip Erase requires a 10-ms PROG pulse.

Figure 3. Programming the Flash

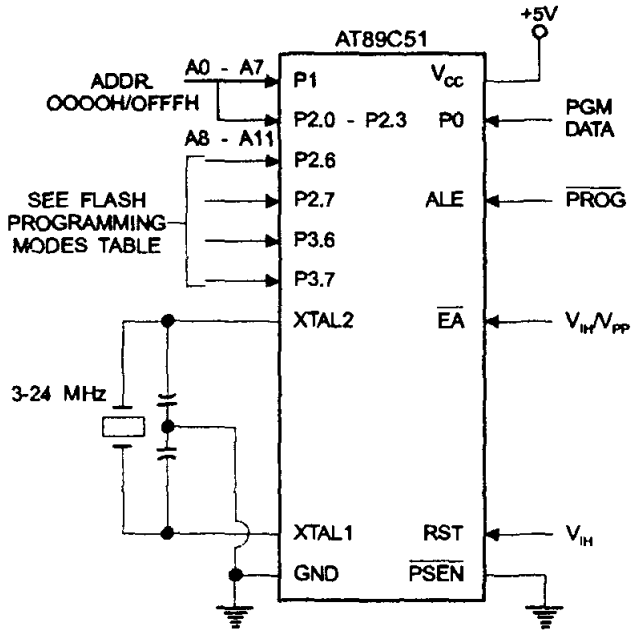
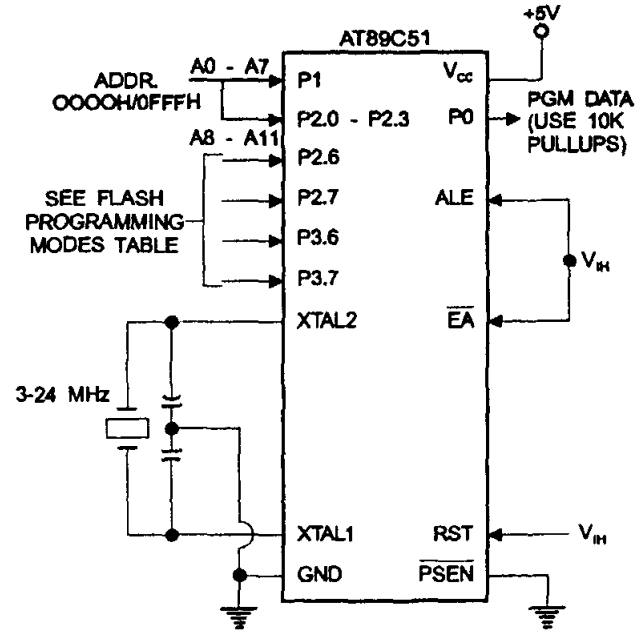


Figure 4. Verifying the Flash



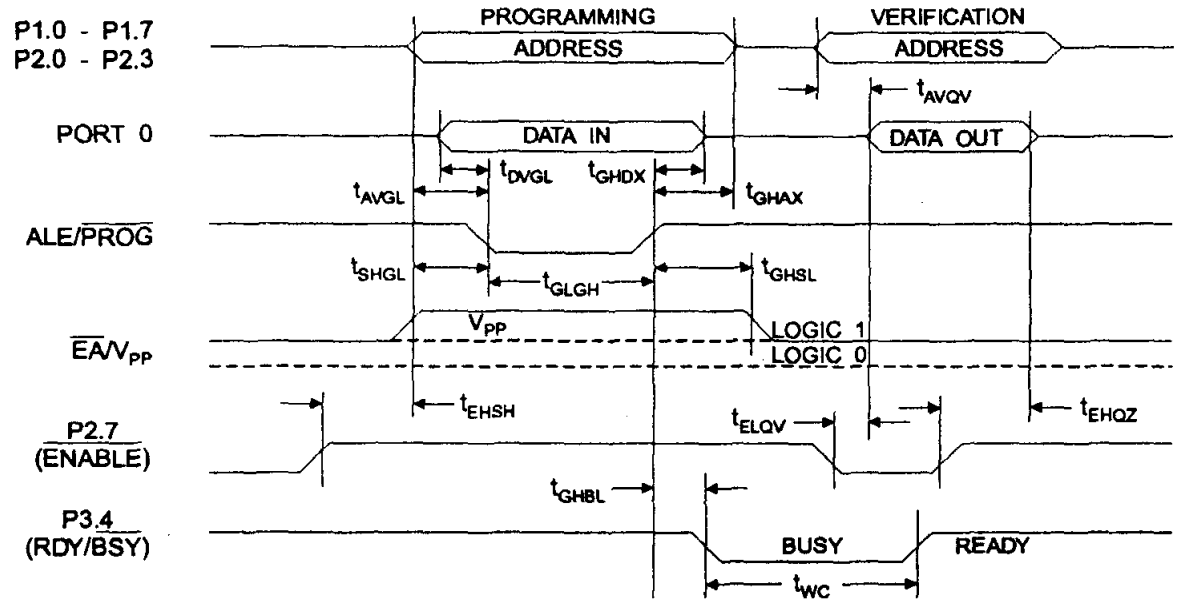
Flash Programming and Verification Characteristics

T_A = 0°C to 70°C, V_{CC} = 5.0 ± 10%

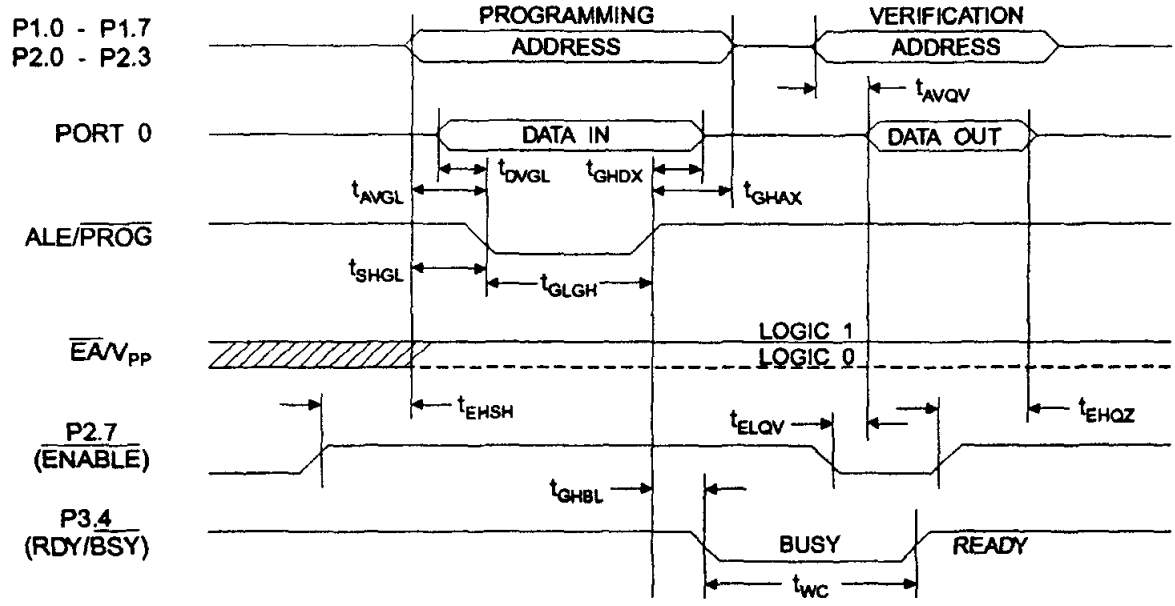
Symbol	Parameter	Min	Max	Units
V_{PP}(1)	Programming Enable Voltage	11.5	12.5	V
I_{PP}(1)	Programming Enable Current		1.0	mA
$1/t_{CLCL}$	Oscillator Frequency	3	24	MHz
t_{AVGL}	Address Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
t_{GHAX}	Address Hold After $\overline{PROG}$	$48t_{CLCL}$		
t_{DVGL}	Data Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
t_{GHDX}	Data Hold After $\overline{PROG}$	$48t_{CLCL}$		
t_{EHSH}	P2.7 ($\overline{ENABLE}$) High to V_{PP}	$48t_{CLCL}$		
t_{SHGL}	V_{PP} Setup to $\overline{PROG}$ Low	10		µs
t_{GHSL}(1)	V_{PP} Hold After $\overline{PROG}$	10		µs
t_{GLGH}	$\overline{PROG}$ Width	1	110	µs
t_{AVQV}	Address to Data Valid		$48t_{CLCL}$	
t_{ELQV}	$\overline{ENABLE}$ Low to Data Valid		$48t_{CLCL}$	
t_{EHQZ}	Data Float After $\overline{ENABLE}$	0	$48t_{CLCL}$	
t_{GHBL}	$\overline{PROG}$ High to $\overline{BUSY}$ Low		1.0	µs
t_{WC}	Byte Write Cycle Time		2.0	ms

Note: 1. Only used in 12-volt programming mode.

Flash Programming and Verification Waveforms - High Voltage Mode (V_{PP} = 12V)



Flash Programming and Verification Waveforms - Low Voltage Mode (V_{PP} = 5V)



Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0V to +7.0V
Maximum Operating Voltage	6.6V
DC Output Current	15.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_A = -40°C to 85°C, V_{CC} = 5.0V ± 20% (unless otherwise noted)

Symbol	Parameter	Condition	Min	Max	Units
V_{IL}	Input Low Voltage	(Except $\overline{EA}$)	-0.5	0.2 V_{CC} - 0.1	V
V_{IL1}	Input Low Voltage ($\overline{EA}$)		-0.5	0.2 V_{CC} - 0.3	V
V_{IH}	Input High Voltage	(Except XTAL1, RST)	0.2 V_{CC} + 0.9	V_{CC} + 0.5	V
V_{IH1}	Input High Voltage	(XTAL1, RST)	0.7 V_{CC}	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage(1) (Ports 1,2,3)	I_{OL} = 1.6 mA		0.45	V
V_{OL1}	Output Low Voltage(1) (Port 0, ALE, $\overline{PSEN}$)	I_{OL} = 3.2 mA		0.45	V
V_{OH}	Output High Voltage (Ports 1,2,3, ALE, $\overline{PSEN}$)	I_{OH} = -60 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -25 µA	0.75 V_{CC}		V
		I_{OH} = -10 µA	0.9 V_{CC}		V
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode)	I_{OH} = -800 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -300 µA	0.75 V_{CC}		V
		I_{OH} = -80 µA	0.9 V_{CC}		V
I_{IL}	Logical 0 Input Current (Ports 1,2,3)	V_{IN} = 0.45V		-50	µA
I_{TL}	Logical 1 to 0 Transition Current (Ports 1,2,3)	V_{IN} = 2V, VCC = 5V ± 10%		-650	µA
I_{LI}	Input Leakage Current (Port 0, $\overline{EA}$)	0.45 < V_{IN} < V_{CC}		±10	µA
RRST	Reset Pulldown Resistor		50	300	KΩ
C_{IO}	Pin Capacitance	Test Freq. = 1 MHz, T_A = 25°C		10	pF
I_{CC}	Power Supply Current	Active Mode, 12 MHz		20	mA
		Idle Mode, 12 MHz		5	mA
	Power Down Mode(2)	V_{CC} = 6V		100	µA
		V_{CC} = 3V		40	µA

Notes: 1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
Maximum I_{OL} per port pin: 10 mA
Maximum I_{OL} per 8-bit port: Port 0: 26 mA
Ports 1, 2, 3: 15 mA
Maximum total I_{OL} for all output pins: 71 mA
If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

2. Minimum V_{CC} for Power Down is 2V.

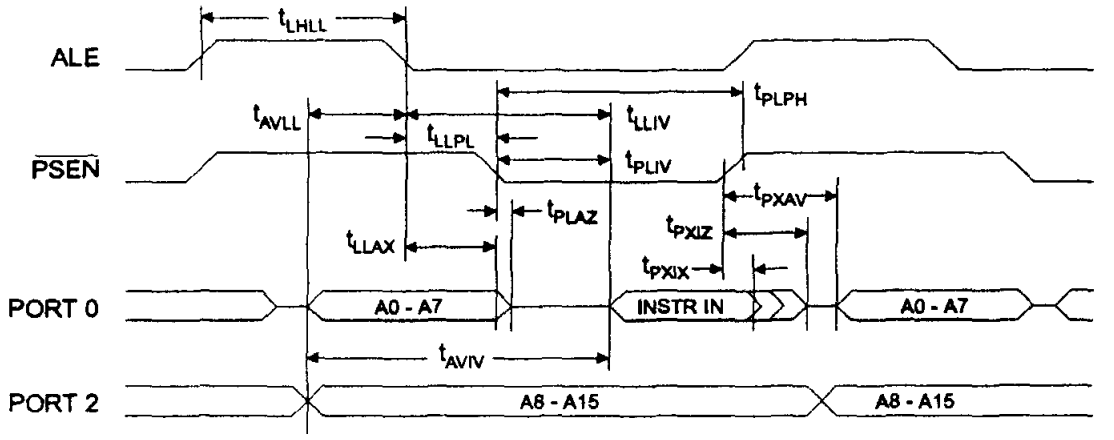
AC Characteristics

(Under Operating Conditions; Load Capacitance for Port 0, ALE/$\overline{PROG}$, and $\overline{PSEN}$ = 100 pF; Load Capacitance for all other outputs = 80 pF)

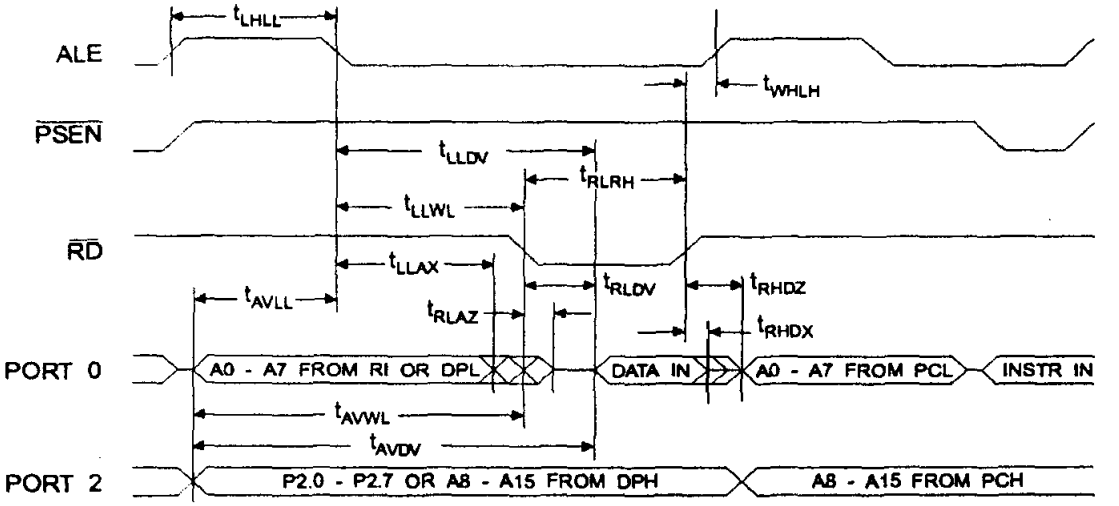
External Program and Data Memory Characteristics

Symbol	Parameter	12 MHz Oscillator		16 to 24 MHz Oscillator		Units
		Min	Max	Min	Max	
$1/t_{CLCL}$	Oscillator Frequency			0	24	MHz
t_{LHLL}	ALE Pulse Width	127		$2t_{CLCL}$-40		ns
t_{AVLL}	Address Valid to ALE Low	43		t_{CLCL}-13		ns
t_{LLAX}	Address Hold After ALE Low	48		t_{CLCL}-20		ns
t_{LLIV}	ALE Low to Valid Instruction In		233		$4t_{CLCL}$-65	ns
t_{LLPL}	ALE Low to $\overline{PSEN}$ Low	43		t_{CLCL}-13		ns
t_{PLPH}	$\overline{PSEN}$ Pulse Width	205		$3t_{CLCL}$-20		ns
t_{PLIV}	$\overline{PSEN}$ Low to Valid Instruction In		145		$3t_{CLCL}$-45	ns
t_{PXIX}	Input Instruction Hold After $\overline{PSEN}$	0		0		ns
t_{PXIZ}	Input Instruction Float After $\overline{PSEN}$		59		t_{CLCL}-10	ns
t_{PXAV}	$\overline{PSEN}$ to Address Valid	75		t_{CLCL}-8		ns
t_{AVIV}	Address to Valid Instruction In		312		$5t_{CLCL}$-55	ns
t_{PLAZ}	$\overline{PSEN}$ Low to Address Float		10		10	ns
t_{RLRH}	$\overline{RD}$ Pulse Width	400		$6t_{CLCL}$-100		ns
t_{WLWH}	$\overline{WR}$ Pulse Width	400		$6t_{CLCL}$-100		ns
t_{RLDV}	$\overline{RD}$ Low to Valid Data In		252		$5t_{CLCL}$-90	ns
t_{RHDX}	Data Hold After $\overline{RD}$	0		0		ns
t_{RHDZ}	Data Float After $\overline{RD}$		97		$2t_{CLCL}$-28	ns
t_{LLDV}	ALE Low to Valid Data In		517		$8t_{CLCL}$-150	ns
t_{AVDV}	Address to Valid Data In		585		$9t_{CLCL}$-165	ns
t_{LLWL}	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	200	300	$3t_{CLCL}$-50	$3t_{CLCL}$+50	ns
t_{AVWL}	Address to $\overline{RD}$ or $\overline{WR}$ Low	203		$4t_{CLCL}$-75		ns
t_{QVWX}	Data Valid to $\overline{WR}$ Transition	23		t_{CLCL}-20		ns
t_{QVWH}	Data Valid to $\overline{WR}$ High	433		$7t_{CLCL}$-120		ns
t_{WHQX}	Data Hold After $\overline{WR}$	33		t_{CLCL}-20		ns
t_{RLAZ}	$\overline{RD}$ Low to Address Float		0		0	ns
t_{WHLH}	$\overline{RD}$ or $\overline{WR}$ High to ALE High	43	123	t_{CLCL}-20	t_{CLCL}+25	ns

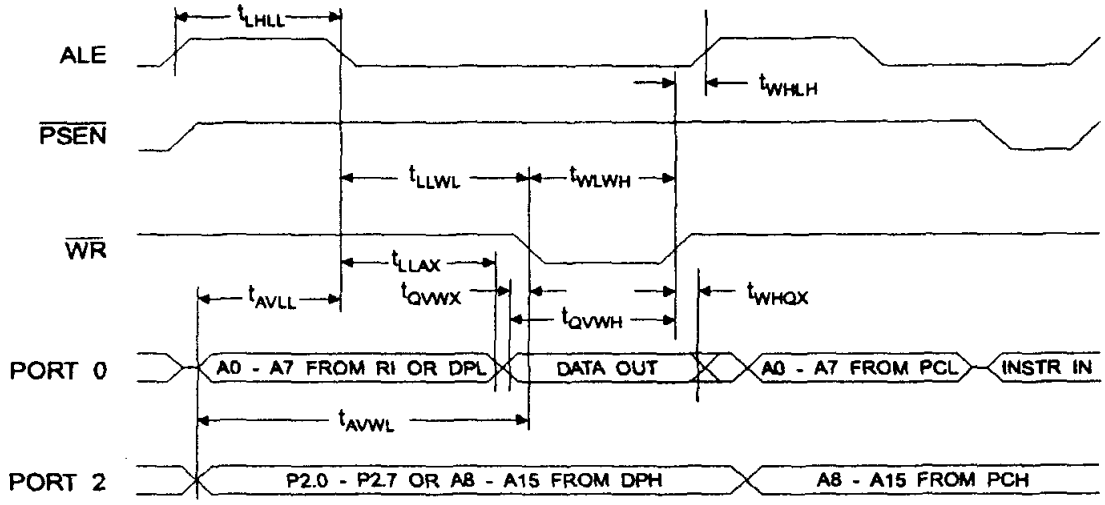
External Program Memory Read Cycle



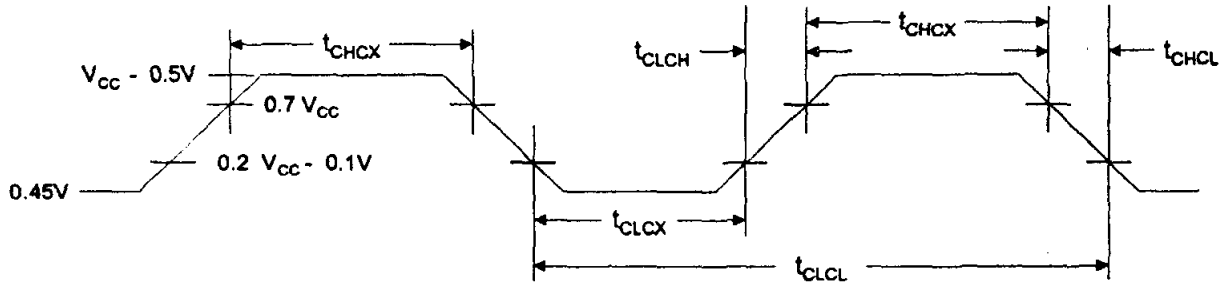
External Data Memory Read Cycle



External Data Memory Write Cycle



External Clock Drive Waveforms



External Clock Drive

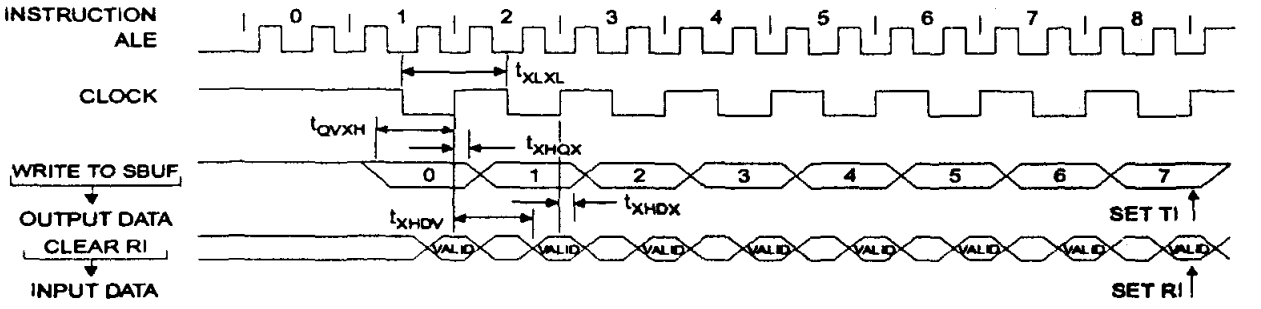
Symbol	Parameter	Min	Max	Units
$1/t_{CLCL}$	Oscillator Frequency	0	24	MHz
t_{CLCL}	Clock Period	41.6		ns
t_{CHCX}	High Time	15		ns
t_{CLCX}	Low Time	15		ns
t_{CLCH}	Rise Time		20	ns
t_{CHCL}	Fall Time		20	ns

Serial Port Timing: Shift Register Mode Test Conditions

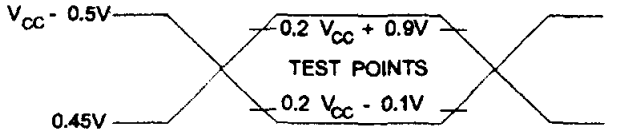
(V_{CC} = 5.0 V ± 20%; Load Capacitance = 80 pF)

Symbol	Parameter	12 MHz Osc		Variable Oscillator		Units
		Min	Max	Min	Max	
t_{XLXL}	Serial Port Clock Cycle Time	1.0		$12t_{CLCL}$		µs
t_{QVXH}	Output Data Setup to Clock Rising Edge	700		$10t_{CLCL}$-133		ns
t_{XHQX}	Output Data Hold After Clock Rising Edge	50		$2t_{CLCL}$-117		ns
t_{XHDX}	Input Data Hold After Clock Rising Edge	0		0		ns
t_{XHDV}	Clock Rising Edge to Input Data Valid		700		$10t_{CLCL}$-133	ns

Shift Register Mode Timing Waveforms

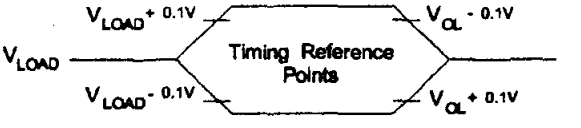


AC Testing Input/Output Waveforms(1)



Note: 1. AC Inputs during testing are driven at V_{CC} - 0.5V for a logic 1 and 0.45V for a logic 0. Timing measurements are made at V_{IH} min. for a logic 1 and V_{IL} max. for a logic 0.

Float Waveforms(1)



Note: 1. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when 100 mV change from the loaded V_{OH}/V_{OL} level occurs.

Ordering Information

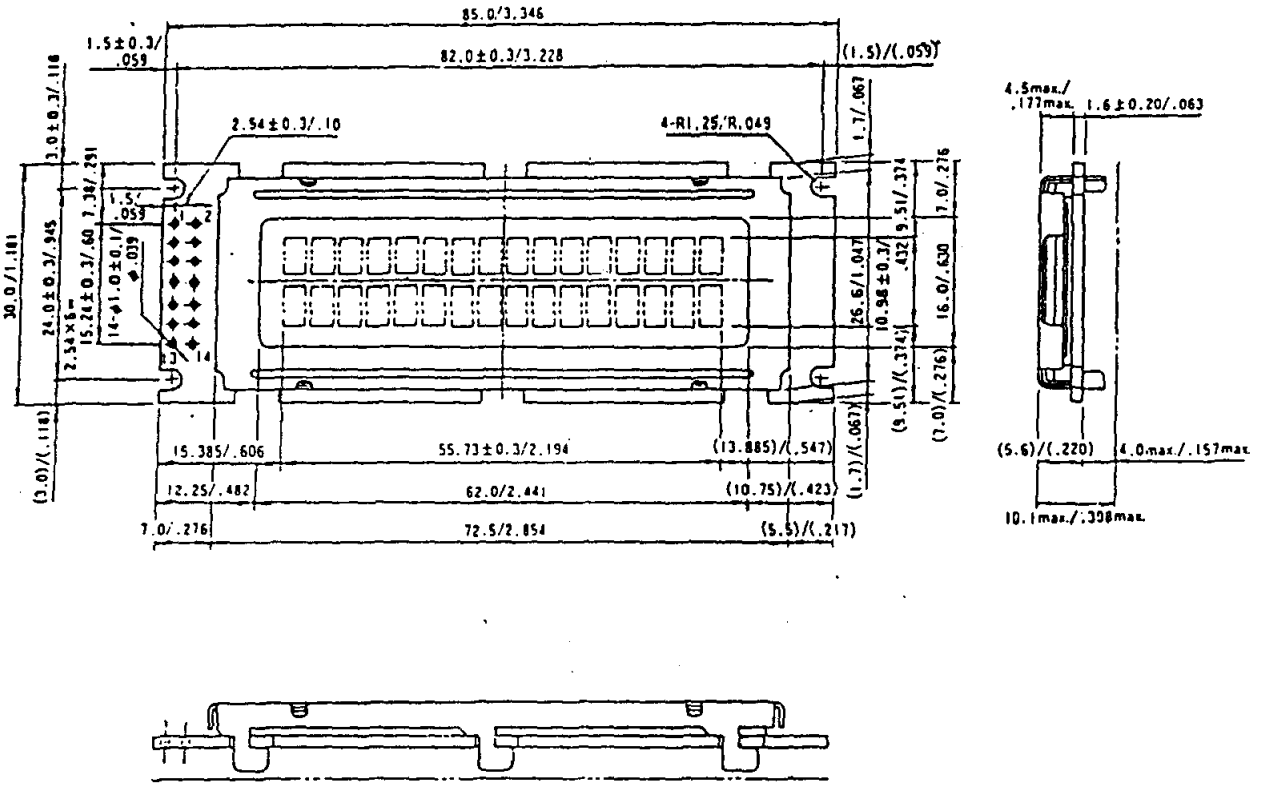
Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
12	5V ± 20%	AT89C51-12AC	44A	Commercial
		AT89C51-12JC	44J	(0°C to 70°C)
		AT89C51-12PC	40P6	
		AT89C51-12QC	44Q	
		AT89C51-12AI	44A	Industrial
		AT89C51-12JI	44J	(-40°C to 85°C)
		AT89C51-12PI	40P6	
		AT89C51-12QI	44Q	
		AT89C51-12AA	44A	Automotive
		AT89C51-12JA	44J	(-40°C to 105°C)
		AT89C51-12PA	40P6	
		AT89C51-12QA	44Q	
16	5V ± 20%	AT89C51-16AC	44A	Commercial
		AT89C51-16JC	44J	(0°C to 70°C)
		AT89C51-16PC	40P6	
		AT89C51-16QC	44Q	
		AT89C51-16AI	44A	Industrial
		AT89C51-16JI	44J	(-40°C to 85°C)
		AT89C51-16PI	40P6	
		AT89C51-16QI	44Q	
		AT89C51-16AA	44A	Automotive
		AT89C51-16JA	44J	(-40°C to 105°C)
		AT89C51-16PA	40P6	
		AT89C51-16QA	44Q	
20	5V ± 20%	AT89C51-20AC	44A	Commercial
		AT89C51-20JC	44J	(0°C to 70°C)
		AT89C51-20PC	40P6	
		AT89C51-20QC	44Q	
		AT89C51-20AI	44A	Industrial
		AT89C51-20JI	44J	(-40°C to 85°C)
		AT89C51-20PI	40P6	
		AT89C51-20QI	44Q	

Ordering Information

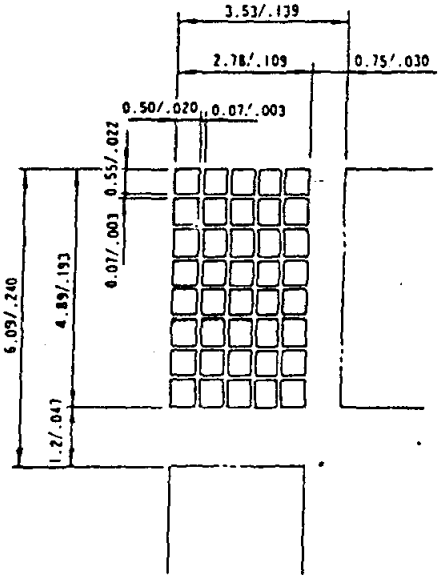
Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
24	5V ± 20%	AT89C51-24AC	44A	Commercial
		AT89C51-24JC	44J	(0°C to 70°C)
		AT89C51-24PC	44P6	
		AT89C51-24QC	44Q	
		AT89C51-24AI	44A	Industrial
		AT89C51-24JI	44J	(-40°C to 85°C)
		AT89C51-24PI	44P6	
		AT89C51-24QI	44Q	

Package Type	
44A	44 Lead, Thin Plastic Gull Wing Quad Flatpack (TQFP)
44J	44 Lead, Plastic J-Leaded Chip Carrier (PLCC)
40P6	40 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
44Q	44 Lead, Plastic Gull Wing Quad Flatpack (PQFP)

Dimensions Diagram



Unit : mm/inch
General tolerance : ± 0.5 mm



No.	Symbol	Level	Function	
1	Vss	-	Power Supply	0V (GND)
2	Vcc	-		5V ±10%
3	Vcc	-		for LCD Drive
4	RS	H/L	H: Data Input L: Instruction Input	
5	R/W	H/L	H:READ L:WRITE	
6	E	H, ↴	Enable Signal	
7	DB0	H/L	| Data Bus	
8	DB1	H/L		
9	DB2	H/L		
10	DB3	H/L		
11	DB4	H/L		
12	DB5	H/L		
13	DB6	H/L		
14	DB7	H/L		
15	V+ BL	-	Back Light Supply	4 - 4.2V 50-200mA
16	V- BL	-		0V (GND)

Figure 1 Dimensions diagram

OPERATING INSTRUCTIONS

INTRODUCTION

Seiko Instruments intelligent dot matrix liquid crystal display modules have on-board controller and LSI drivers, which display alpha numerics, Japanese KATA KANA characters and a wide variety of other symbols in either 5 x 7 dot matrix.

The internal operation in the KS0066 controller chip is determined by signals sent from the MPU. The signals include: 1) Register select RS input consisting of instruction register (IR) when RS = 0 and data register (DR) when RS = 1; 2) Read/write (R/W); 3) Data bus (DB7~ DB0); and 4) Enable strobe (E) depending on the MPU or through an external parallel I/O port. Details on instructions data entry, execution times, etc. are explained in the following sections.

READ AND WRITE TIMING DIAGRAMS AND TABLES

The following timing characteristics are applicable for all of Seiko's LCD dot matrix character modules.

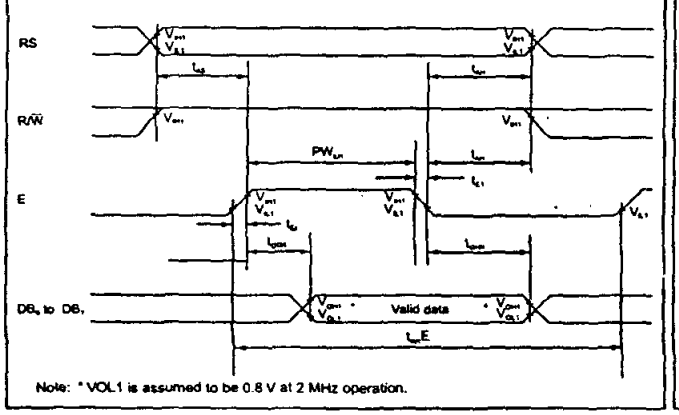
READ TIMING CHARACTERISTICS
V_{DD}=5.0V±5%, V_{SS}=0V, T_A=0°C TO 50°C

Item	Symbol	Standard		Unit
		Min.	Max.	
Enable cycle time	$t_{CYC}E$	500	—	ns
Enable pulse width High Level	PW_{EH}	230	—	ns
Enable rise and fall time	t_{ER}, t_{EF}	—	20	ns
Address setup time RS,R/W—E	t_{AS}	40	—	ns
Address hold time	t_{AH}	10	—	ns
Data delay time	t_{DDR}	—	160	ns
Data hold time	t_H	5	—	ns

WRITE TIMING CHARACTERISTICS
V_{DD}=5.0V±5%, V_{SS}=0V, T_A=0°C TO 50°C

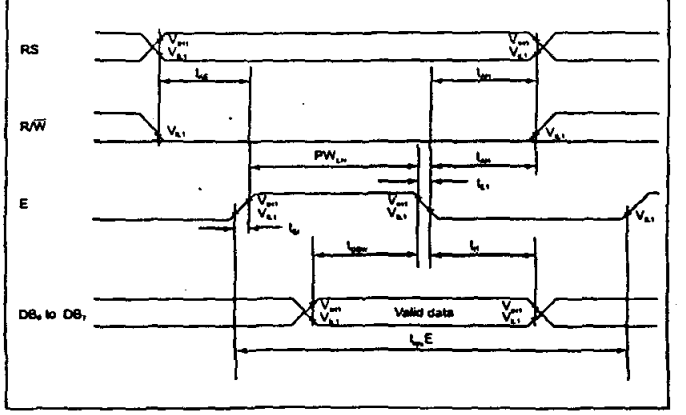
Item	Symbol	Standard		Unit
		Min.	Max.	
Enable cycle time	$t_{CYC}E$	500	—	ns
Enable pulse width High Level	PW_{EH}	230	—	ns
Enable rise and fall time	t_{ER}, t_{EF}	—	20	ns
Address setup time RS,R/W—E	t_{AS}	40	—	ns
Address hold time	t_{AH}	10	—	ns
Data setup time	t_{DSW}	80	—	ns
Data hold time	t_H	10	—	ns

READ OPERATION



DATA READ FROM MODULE TO MPU

WRITE OPERATION



DATA WRITE FROM MPU TO MODULE

OPERATING INSTRUCTIONS

INTRODUCTION CODES

Instruction	Set RS	R/W	Instruction Code DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Description	Execution Time (when f_{cp} or f_{osc} is 250 kHz)
Clear Display	0	0	0	0	0	0	0	0	0	1	Clears all display memory and returns the cursor to the home position (Address 0).	82 μs - 1.64ms
Return Home	0	0	0	0	0	0	0	0	1	*	Returns the cursor to the home position (Address 0) shifted to the original position. DD RAM contents remain unchanged.	40 μs - 1.6ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Sets the cursor move direction and specifies to or not to shift the display. These operations write and read.	40 μs - 1.64ms
Display ON/OFF Control	0	0	0	0	0	0	1	D	C	B	(D) is display ON/OFF control; memory remains unchanged in OFF condition. (C) cursor ON/OFF (B) blinking cursor.	40 μs
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	*	*	Moves the cursor and shifts the display without changing DD RAM contents.	40 μs
Function Set	0	0	0	0	1	DL	N	F	*	*	Sets interface data length (DL), number of display lines (N), and character font (F).	40 μs
Set CG RAM Address	0	0	0	1	A_{CG}						Sets the CG RAM address. CG RAM data is sent and received after this setting.	40 μs
Set DD RAM Address	0	0	1	A_{DD}							Sets the DD RAM address. DD RAM data is sent and received after this setting.	40 μs
Read Busy Flag & Address	0	1	BF	AC							Reads Busy Flag (BF) indicating internal operation is being performed and reads address counter contents.	1 μs
Write Data to CG or to DD RAM	1	0	Write Data								Writes data into DD RAM or CG RAM.	40 μs
Read Data from CG or DD RAM	1	1	Read Data								Reads data from DD RAM or CG RAM.	40 μs

* Doesn't matter

DD RAM: Display data RAM
CG RAM: Character generator RAM
A_{CG}: CG RAM address
A_{DD}: DD RAM address corresponds to cursor address
AC: Address counter used for both DD RAM and CG RAM address

I/D = 1: Increment
I/D = 0: Decrement

S = 1: Display shift
S = 0: No display shift

D = 1: Display ON
D = 0: Display OFF

C = 1: Cursor ON
C = 0: Cursor OFF

B = 1: Blink ON
B = 0: Blink OFF

S/C = 1: Display shift
S/C = 0: Cursor movement

BF = 1: Internal operation in progress
BF = 0: Instruction can be accepted

R/L = 1: Right shift
R/L = 0: Left shift

DL = 1: 8 bits
DL = 0: 4 bits

N = 1: 2 lines (L1671)

F = 0: 5 x 7 dot matrix

Execution times in the above table indicate the minimum values when operating frequency is 250 kHz.

When f_{osc} is 270 kHz: 40μs x 250/250 = 37μs

OPERATING INSTRUCTIONS

INTRODUCTION CODE EXPLANATIONS

The two registers 1) Instruction Register (IR) and the 2) Data Register (DR) in the KS0066 controller chip are directly controlled by the MPU. Control information is temporarily stored in these registers prior to internal operation start. This allows interface to various types of MPUs which operate at different speeds from that of the KS0066, and allows interface from peripheral control ICs. Internal operations of the KS0066 are determined from the signals sent from the MPU. These signals, including register selection signals (RS), Read/Write (R/W) and data bus signals (DB0 - DB7) are polled instructions.

REGISTER SELECTION

RS	R/W	Operation
0	0	IR selection, IR write. Internal operation: Display clear
0	1	Busy flag (DB7) and address counter (DB0 to DB6) read
1	0	DR selection, DR write. Internal operation: DR to DD RAM or CG RAM
1	1	DR selection, DR read. Internal operation: DD RAM or CG RAM to DR

ADDRESS COUNTER (AC)

The counter specifies an address when data is written into DD RAM or CG RAM and the data stored in DD RAM or CG RAM is read out. If an Address Set instruction (for DD RAM or CG RAM) is written in the IR, the address information is transferred from the IR to the AC. When display data is written into or read from DD RAM or CG RAM, the AC is automatically incremented or decremented by one according to the Entry Mode Set. The contents of the AC are output to DB0 to DB6; refer to above "Register Selection Table" when RS = 0 and R/W = 1.

CLEAR DISPLAY

	RS	R/W	DB7							DB0
Code	0	0	0	0	0	0	0	0	0	1

Clear all display memory and return the cursor to the home position. In other words, the cursor returns to the first character block on the first line on all 1, 2, and 4 line character modules except L4044. I the above is entered on E2 (the second controller for lines 3 and 4), the cursor will return to the first character on the third line.

CURSOR HOME

	RS	R/W	DB7							DB0
Code	0	0	0	0	0	0	0	0	1	*

*Doesn't matter

Returns cursor to home position. First line first character blocks on all 1, 2 and 4 line display; except L4044 refer "clear display": (Address 0; A_{DD} "80"). The contents of the DD RAM remain unchanged.

RESTRICTIONS ON EXECUTION OF DISPLAY CLEAR AND CURSOR HOME INSTRUCTIONS

Conditions of use	Restrictions
When executing the Display Clear or Cursor Home instruction when the display is shifted (after execution of Display Shift instruction).	The Cursor Home instruction should be executed again immediately after the Display Clear or Cursor Home instruction is executed. Do not leave an interval of a multiple of $400/f_{osc}$* second after the first execution. • L4052: f_{osc} = 250 kHz • The other modules: f_{osc} = 270 kHz *f_{osc}: Oscillation frequency
When 23_H, 27_H, 63_H, or 67_H is used as a DD RAM address to execute Cursor Home instruction.	Before executing the Cursor Home instruction, the data of the four DD RAM addresses given at the left should be read and saved. After execution, write the data again in DD RAM. (This restriction is necessary to prevent the contents of the DD RAM addresses from being destroyed after the Cursor Home instruction has been executed.)

OPERATING INSTRUCTIONS

ENTRY MODE SET

	RS	R/W	DB7						DB0
Code	0	0	0	0	0	0	0	1	I/D	S

I/D: Increments (I/D = 1) or decrements (I/D = 0) the DD RAM address by one block when writing or reading a character code from DD RAM or CG RAM. The cursor automatically moves to the right when incremented by one or to the left if decremented by one.

S: Shifts the entire display to either the right or left when S = 1 (high). When S = 1 and I/D = 1 the display shifts one position to the left. When S = 1 and 1/D = 0 the display shifts one position to the right. This right or left shift occurs after each data write to DD RAM. Display is not shifted when reading from DD RAM. Display is not shifted when S = 0.

DISPLAY AND CURSOR ON/OFF CONTROL

	RS	R/W	DB7						DB0
Code	0	0	0	0	0	0	1	D	C	B

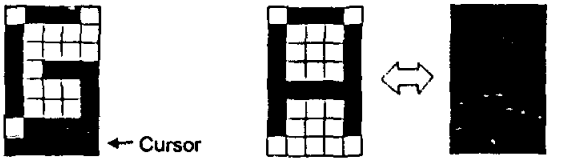
D: Display is turned ON when D = 1 and OFF when D = 0. When display is OFF, display data in DD RAM remains unchanged. Information comes back immediately when D = 1 is entered.

C: Cursor is displayed when C = 1 and not displayed when C = 0. If the cursor disappears, function of I/D etc. does not change during display data write. In a 5 x 7 dot matrix there is an eighth line which functions as the cursor.

B: When B = 1, the character at the cursor position starts blinking. When B = 0 the cursor does not blink. The blink is done by stiching between the all black dot matrix and displayed character at 0.4 seconds intervals. The cursor and the blink can be set at the same time (fosc = 250 kHz).

5 x 7 DOT MATRIX

C = 1 (cursor display) B = 1 (blinking)



CURSOR OR DISPLAY SHIFT

	RS	R/W	DB7						DB0
Code	0	0	0	0	0	1	S/C	R/L	*	*

* Doesn't Matter

Cursor/Display Shift moves the cursor or shifts the display without changing the DD RAM contents.

The cursor position and the AC contents match. This instruction is available for display correction and retrieval because the cursor position or display can be shifted without writing or reading display data. In case of a 2-line display, the cursor is shifted from character block 40 of line 1 to character block 1 of line 2. Displays of lines 1 and 2 are shifted at the same time. In case of a 4-line display, the cursor does not move continuously from line 2 to line 3. The cursor is shifted from character block 40 of line 3 to character block 1 of line 4. Displays of lines 3 and 4 are shifted at the same time. The display pattern of line 2 or 4 is not shifted to line 1 or 3.

S/C	R/L	Operation
0	0	The cursor position is shifted to the left (the AC decrements one)
0	1	The cursor position is shifted to the right (the AC increments one)
1	0	The entire display is shifted to the left with the cursor
1	1	The entire display is shifted to the right with the cursor

OPERATING INSTRUCTIONS

FUNCTION SET

	RS	R/W	DB7							DB0
Code	0	0	0	0	1	DL	N	F	*	*

* Doesn't Matter

Function Set sets the interface data length, the number of display lines and the character font.

DL: Interface data length

When DL = 1, the data length is set at 8 bits (DB7 to DB0).

When DL = 0, the data length is set at 4 bits (DB7 to DB4).

The upper 4 bits are transferred first, then the lower 4 bits follow.

N: Number of display lines

F: Sets character font

N	F	Number of display lines	Character font	Duty Cycle	LCD Module
1	0	2	5 x 7 dot matrix	1/16	All character LCD modules

The Function Set instruction must be executed prior to all other instructions except for Busy Flag/Address Read. If another instruction is executed first, no function instruction except changing the interface data lenght can be executied.

CG RAM ADDRESS SET

	RS	R/W	DB7							DB0
Code	0	0	0	1	A	A	A	A	A	A
				← Upper bit					Lower bit →	

CG RAM addresses, expressed as binary AAAAAA, are set to the AC. Then data in CG RAM is written from or read to the MPU.

DD RAM ADDRESS SET

	RS	R/W	DB7							DB0
Code	0	0	1	A	A	A	A	A	A	A
				← Upper bit					Lower bit →	

DD RAM addresses expressed as binary AAAAAA are set to the AC. Then data in DD RAM is written from or read to the MPU.

BUSY FLAG/ADDRESS READ

	RS	R/W	DB7							DB0
Code	0	0	BF	A	A	A	A	A	A	A
				← Upper bit					Lower bit →	

The BF signal can be read to verify if the controller is indicating that the module is working on a current instruction.

When BF = 1, the module is working internally and the next instruction cannot be accepted until the BF value becomes 0.

When BF = 0, the next instruction can be accepted.

Therefore, make sure that BF = 0 before writing the next instruction. The AC values of binary AAAAAA are read out at the same time as reading the busy flag. The AC addresses are used for both CG RAM and DD RAM but the address set before execution of the instruction determines which address is to be used.

DATA WRITE TO CG RAM OR DD RAM

	RS	R/W	DB7							DB0
Code	1	0	D	D	D	D	D	D	D	D
				← Upper bit					Lower bit →	

Binary eight-bit data DDDDDDDD is written into CG RAM or DD RAM. The CG RAM Address Set instruction or the DD RAM Address Set instruction before this instruction selects either RAM. After the write operation, the address and display shift are determined by the entry mode setting.

DATA READ TO CG RAM OR DD RAM

	RS	R/W	DB7							DB0
Code	1	1	D	D	D	D	D	D	D	D
				← Upper bit					Lower bit →	

Binary eight-bit data DDDDDDDD is read from CG RAM or DD RAM. The CG RAM Address Set instruction or the DD RAM Address Set instruction before this instruction selects either RAM. In addition, either instruction is executed immediately before this instruction. If no Address Set instruction is executed before a read instruction, the first data read becomes invalid. If read instructions are executed consecutively, data is normally read from the second time. However, if the cursor is shifted by the Cursor Shift instruction when reading DD RAM, there is no need to execute an address set instruction because the Cursor Shift instruction does this.

After the read operation, the address is automatically incremented or decremented by one according to the entry mode, but the display is not shifted.

Note: The AC is automatically incremented or decremented by one according to the entry mode after a write instruction is excecuted to write data in CG RAM or DD RAM. However, the data of the RAM selected by the AC are not read out even if a read instruction is executed immediately afterwards.

OPERATING INSTRUCTIONS

5 x 7 + CURSOR

Relationships between CG RAM addresses and character codes (DD RAM) and character patterns (CG RAM data), (5 x 7 dot matrix).5 X 7 Table

Character code (DD RAM data)								CG RAM address						Character pattern (CG RAM data)								
7	6	5	4	3	2	1	0	5	4	3	2	1	0	7	6	5	4	3	2	1	0	
Upper bit						Lower bit		Upper bit			Lower bit			Upper bit					Lower bit			
0	0	0	0	*	0	0	0	0	0	0	0	0	0	•	•	•	1	1	1	1	0	
											0	0	1				1	0	0	0	1	
											0	1	0				1	0	0	0	1	
											0	1	1				1	1	1	1	0	
											1	0	0				1	0	1	0	0	
											1	0	1				1	0	0	1	0	
											1	1	0				1	0	0	0	1	
											1	1	1	•	•	•	0	0	0	0	0	Cursor position
0	0	0	0	*	0	0	1	0	0	1	0	0	0	•	•	•	1	0	0	0	1	
											0	0	1				0	1	0	1	0	
											0	1	0				1	0	1	1	1	
											0	1	1				0	0	1	0	0	
											1	0	0				1	1	1	1	1	
											1	0	1				0	0	1	0	0	
											1	1	0				0	0	1	0	0	
											1	1	1	•	•	•	0	0	0	0	0	
											0	0	0	•	•	•						
											0	0	1									
0	0	0	0	*	1	1	1	1	1	1												
											1	0	0									
											1	0	1									
											1	1	0									
											1	1	1	•	•	•						

Example of character pattern (R)

Example of character pattern (¥)

NOTES:

- In CG RAM data, 1 corresponds to Selection and 0 to Non-selection on the display.
- Character code bits 0 to 2 and CG RAM address bits 3 to 5 correspond with each other (three bits, eight types).
- CG RAM address bits 0 to 2 specify a line position for a character pattern. Line 8 of a character pattern is the cursor position where the logical sum of the cursor and CG RAM data is displayed. Set the data of line 8 to 0 to display the cursor. If the data is charged to 1, one bit lights, regardless of the cursor.
- The character pattern column position corresponds to CG RAM data bits 0 to 4 and bit 4 comes to the left end. CG RAM data bits 5 to 7 are not displayed but can be used as general data RAM.
- When reading a character pattern from CG RAM, set to 0 all of character code bits 4 to 7. Bits 0 to 2 determine which pattern will be read out. Since bit 3 is not valid, 00_H and 08_H select the same character.

OPERATING INSTRUCTIONS

PROGRAMMING THE CHARACTER GENERATOR RAM (CG RAM)

The character generator RAM (CG RAM) allows the user to create up to eight custom 5 x 7 characters + cursor (5 x 8). Once programmed, the custom characters or symbols are accessed exactly as if they were in ROM. However since the RAM is a volatile memory, power must be continually maintained. Otherwise, the custom characters/symbols must be programmed into non-volatile external ROM and sent to the display after each display initialization. All dots in the 5 x 8 dot matrix can be programmed, which includes the cursor position.

The modules RAM are divided into two parts: data display RAM (DD RAM) and custom character generator RAM (CG RAM). This is not to be confused programming the custom character generator RAM with the 192 character generator ROM. The CG RAM is located between hex 40 and 7F and is contiguous. Locations 40 thru 47 hold the first custom character (5 x 8), 48 thru 4F hold the second custom character, 50 thru 57 hold the third CG, and so forth to 78 thru 7F for the eighth CG character/symbol.

If during initialization the display was programmed to automatically increment, then only the single initial address, 40, need be sent. Consecutive row data will automatically appear at 41, 42, etc. until the completed character is formed. All eight custom CG characters can be programmed in 64 consecutive "writes" after sending the single initial 40 address.

The CG RAM is 8 bits wide, although only the right-most 5-bits are used for a custom CG character row. The left-most dot of programming the CG RAM character corresponds to D4 in the most significant nibble (XXXD4) of the data bus code, with the remaining 4 dots in the row corresponding to the least significant nibble (D3 thru D0), D0 being the right-most dot. Thus, hex 1F equals all dots on and hex 00 equals all dots off. Examples include hex 15 (10101) equal to 3 dots on the hex 0A (01010) equal 2 dots on. In each case the key 5-bits of the 8-bit code program one row of a custom CG character. When all 7 or 8 rows are programmed, the character is complete. A graphic example is shown below:

RS	R/W	Data	Display	Description
0	0	40	—	addresses 1st row, 1st CG character
1	0	11	* *	result of 11, 1st row
1	0	0A	**	result of 0A, 2nd row
1	0	1F	*****	result of 1F, 3rd row
1	0	04	*	result of 04, 4th row
1	0	1F	*****	result of 1F, 5th row
1	0	04	*	result of 04, 6th row
1	0	04	*	result of 04, 7th row
1	0	00	—	result of 00, 8th row (cursor position)
1	0	15	***	1st row, 2nd CG character. **Note:** Addressing not now required; hex 48 is next in the sequence.

OPERATING INSTRUCTIONS

ADDRESS LOCATIONS

1) L1671-SERIES (16 characters x 1 line)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Line 1	80	81	82	83	84	85	86	87	C0	C1	C2	C3	C4	C5	C6	C7

NOTE: L1671 series is initialized as a 2 line display, because of the absence of an LCD driver. You must address character no. 9 as you would the first position on the 2nd line which is (C0).

2) L1672-SERIES (16 characters x 2 lines)
L1682-SERIES
L1692-SERIES

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Line 1	80	81	82	83	84	85	86	87	88	89	8A	8B	8C	8D	8E	8F
Line 2	C0	C1	C2	C3	C4	C5	C6	C7	C8	C9	CA	CB	CC	CD	CE	CF

3) L1634-SERIES (16 characters x 4 lines)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Line 1	80	81	82	83	84	85	86	87	88	89	8A	8B	8C	8D	8E	8F
Line 2	C0	C1	C2	C3	C4	C5	C6	C7	C8	C9	CA	CB	CC	CD	CE	CF
Line 3	90	91	92	93	94	95	96	97	98	99	9A	9B	9C	9D	9E	9F
Line 4	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	DA	DB	DC	DD	DE	DF

4) L2032-SERIES (20 characters x 2 lines)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
Line 1	80	81	82	83	84	85	86	87	88	89	8A	8B	8C	8D	8E	8F	90	91	92	93
Line 2	C0	C1	C2	C3	C4	C5	C6	C7	C8	C9	CA	CB	CC	CD	CE	CF	D0	D1	D2	D3

5) L2034-SERIES (20 characters x 4 lines)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
Line 1	80	81	82	83	84	85	86	87	88	89	8A	8B	8C	8D	8E	8F	90	91	92	93
Line 2	C0	C1	C2	C3	C4	C5	C6	C7	C8	C9	CA	CB	CC	CD	CE	CF	D0	D1	D2	D3
Line 3	94	95	96	97	98	99	9A	9B	9C	9D	9E	9F	A0	A1	A2	A3	A4	A5	A6	A7
Line 4	D4	D5	D6	D7	D8	D9	DA	DB	DC	DD	DE	DF	E0	E1	E2	E3	E4	E5	E6	E7

6) L2462-SERIES (24 characters x 2 lines)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
Line 1	80	81	82	83	84	85	86	87	88	89	8A	8B	8C	8D	8E	8F	90	91	92	93	94	95	96	97
Line 2	C0	C1	C2	C3	C4	C5	C6	C7	C8	C9	CA	CB	CC	CD	CE	CF	D0	D1	D2	D3	D4	D5	D6	D7

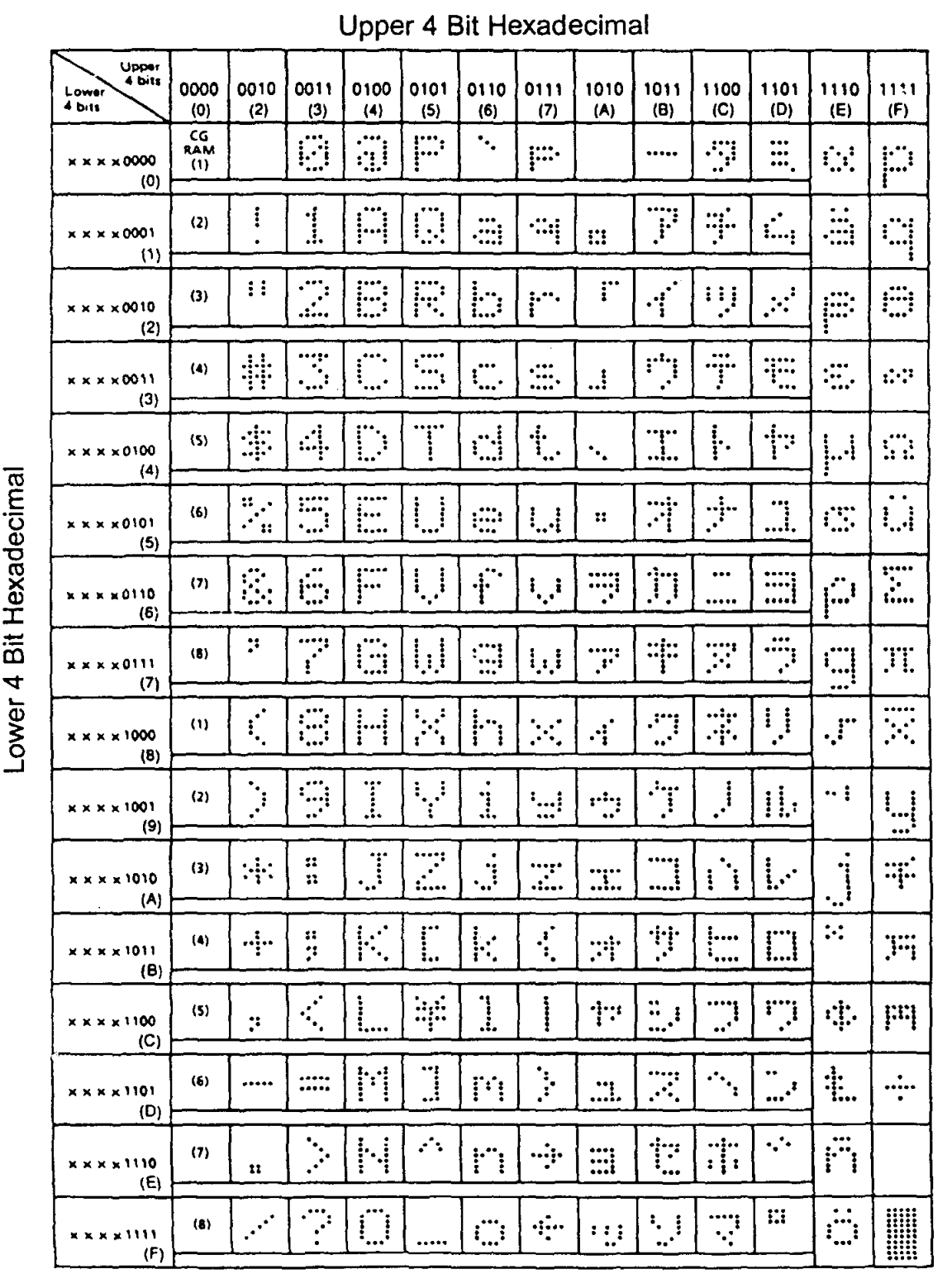
7) L4052-SERIES (40 characters x 2 lines)
L4044-SERIES (40 characters x 4 lines)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40
Line 1	80	81	82	83	84	85	86	87	88	89	8A	8B	8C	8D	8E	8F	90	91	92	93	94	95	96	97	98	99	9A	9B	9C	9D	9E	9F	A0	A1	A2	A3	A4	A5	A6	A7
Line 2	C0	C1	C2	C3	C4	C5	C6	C7	C8	C9	CA	CB	CC	CD	CE	CF	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	DA	DB	DC	DD	DE	DF	E0	E1	E2	E3	E4	E5	E6	E7
Line 3	80	81	82	83	84	85	86	87	88	89	8A	8B	8C	8D	8E	8F	90	91	92	93	94	95	96	97	98	99	9A	9B	9C	9D	9E	9F	A0	A1	A2	A3	A4	A5	A6	A7
Line 4	C0	C1	C2	C3	C4	C5	C6	C7	C8	C9	CA	CB	CC	CD	CE	CF	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	DA	DB	DC	DD	DE	DF	E0	E1	E2	E3	E4	E5	E6	E7

Note: Address locations on lines 1 & 2 are controlled by enabling E1. Address locations on lines 3 & 4 are controlled by enabling E2.

OPERATING INSTRUCTIONS

CHARACTER FONT CODES (5 x 7 DOT MATRIX)



OPERATING INSTRUCTIONS

EXAMPLES OF 8-BIT AND 4-BIT DATA TRANSFER OPERATION

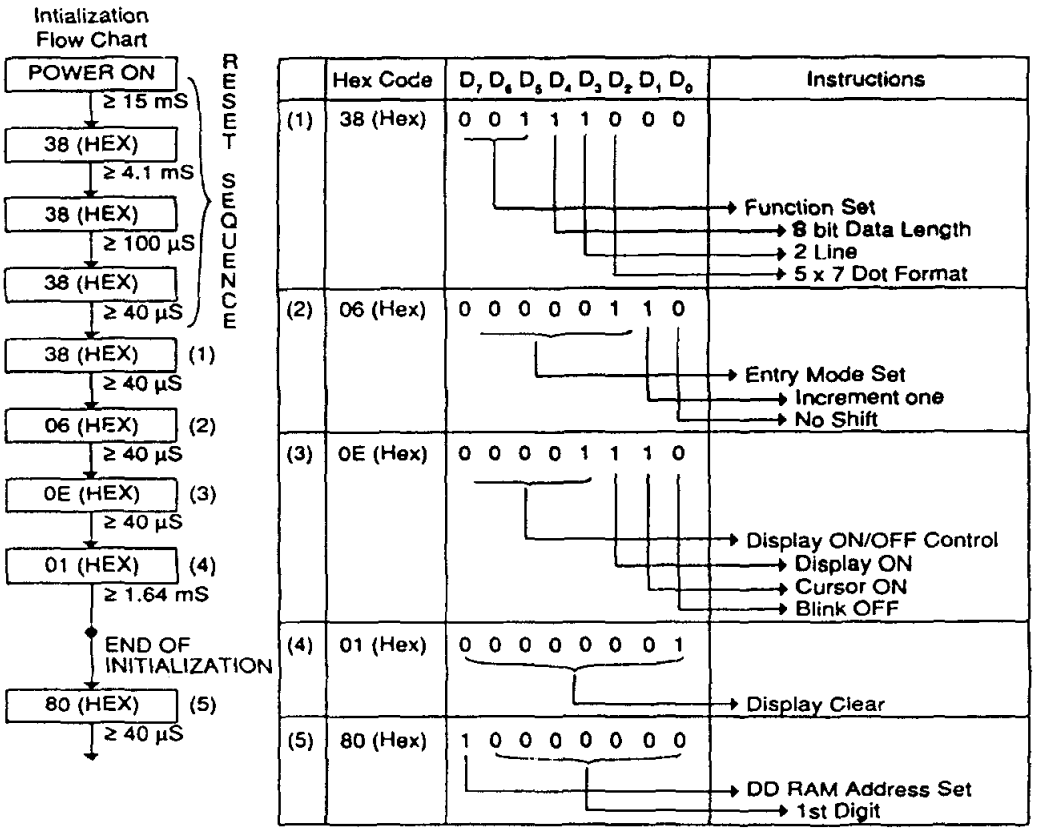
DISPLAY INITIALIZATION

Each time the module is turned on or reset, an initialization procedure must be executed. The procedure consists of sending a sequence of hex codes from the microprocessor or parallel I/O port. The initialization sequence turns on the cursor, clears the display, and sets the module onto an auto-increment mode.

The initial hex code 30, 34, or 38 is sent two or more times to ensure the module enters the 8-bit or 4-bit data mode. All the initialization sequences are performed under the condition of Register Select (RS) = 0 (low) and Read/Write (R/W) = 0 (low).

The 4-bit data bus microcontroller may operate the display module by sending the initialization sequence in 4-bit format. Since 4-bit operation requires the data to be sent twice over the higher 4-bit bus lines (D4-D7), memory requirements are doubled.

A. EXAMPLE FOR THE MODULE WITH 5 x 7 Character Format Under 8-Bit Data Transfer



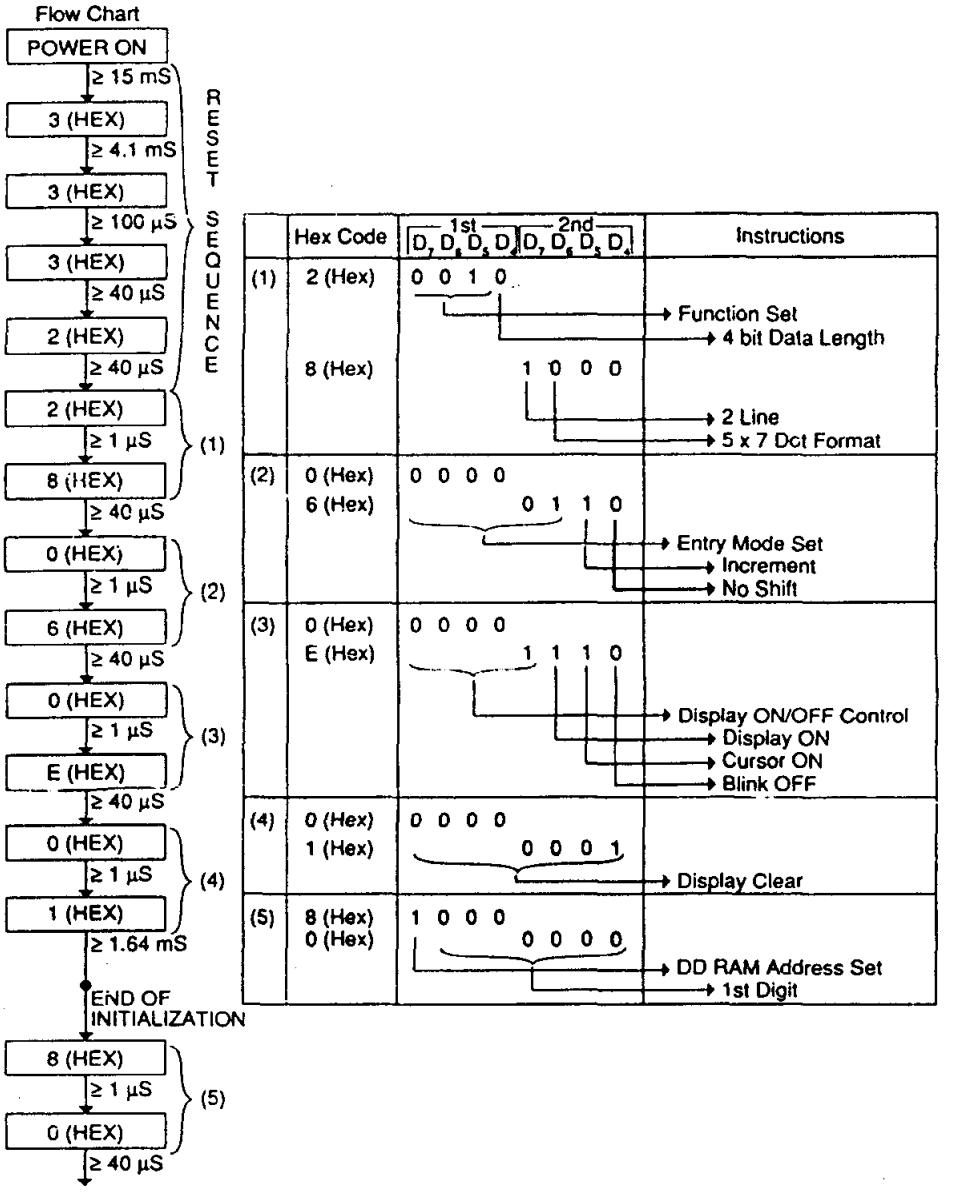
Note:

1) Both RS and R/W terminals shall be "0" in this sequence.
2) RS, R/W and Data are latched at the falling edge of the Enable signal, (falling edge is typically 10nSec; Max: 20nSec).
3) L4044 has t obe initialized on E1 and E2 respectively.

OPERATING INSTRUCTIONS

EXAMPLES OF 8-BIT AND 4-BIT DATA TRANSFER OPERATION

B. EXAMPLE FOR THE MODULE WITH 5 x 7 Character Format Under 4-Bit Data Transfer



Note:
1) Both RS and R/W terminals shall be "0" in this sequence.
2) RS, R/W and Data are latched at the falling edge of the Enable signal,
3) Enable signal has to be sent after every 4-bit Data transfer.

Timer — NE/SA/SE555/SE555C

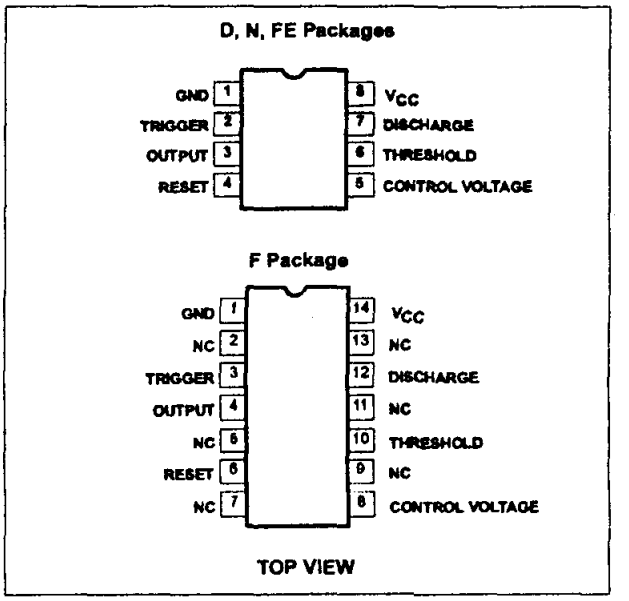
DESCRIPTION

The 555 monolithic timing circuit is a highly stable controller capable of producing accurate time delays, or oscillation. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For a stable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output structure can source or sink up to 200mA.

FEATURES

- Turn-off time less than 2µs
- Max. operating frequency greater than 500kHz
- Timing from microseconds to hours
- Operates in both astable and monostable modes
- High output current
- Adjustable duty cycle
- TTL compatible
- Temperature stability of 0.005% per °C

PIN CONFIGURATIONS



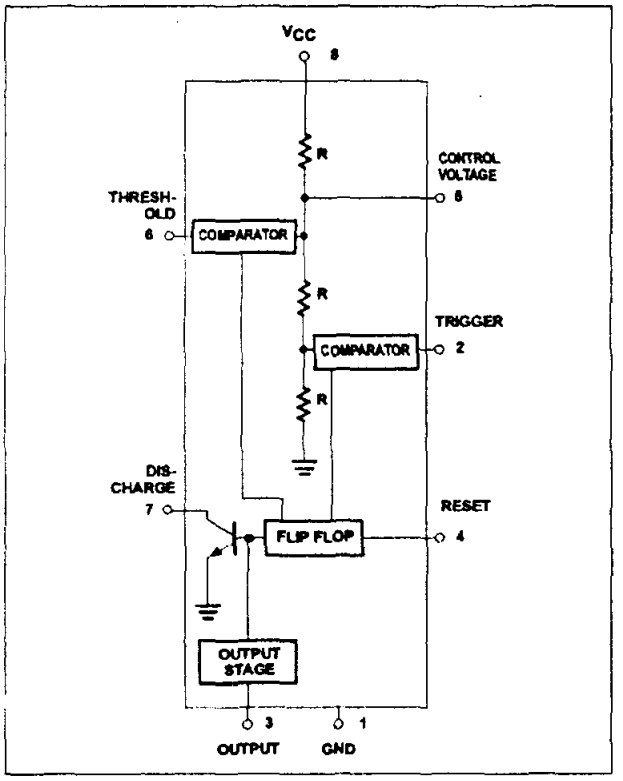
APPLICATIONS

- Precision timing
- Pulse generation
- Sequential timing
- Time delay generation
- Pulse width modulation

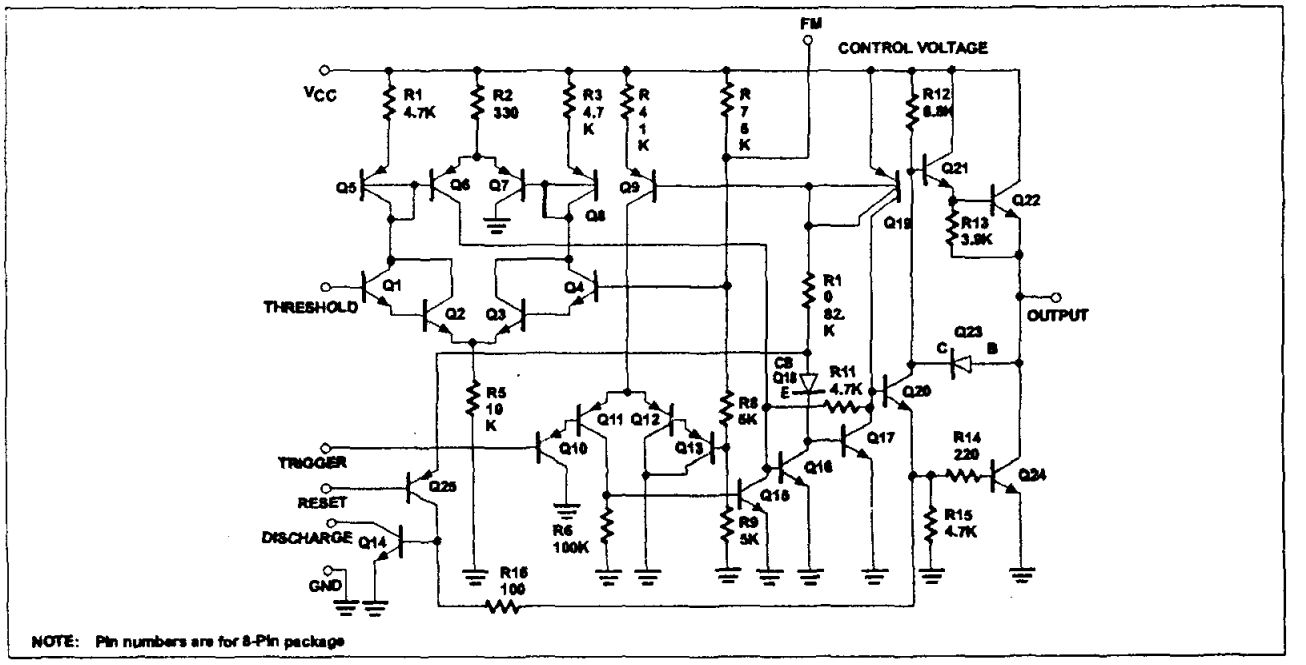
ORDERING INFORMATION

DESCRIPTION	TEMPERATURE RANGE	ORDER CODE	DWG #
8-Pin Plastic Small Outline (SO) Package	0 to +70°C	NE555D	0174C
8-Pin Plastic Dual In-Line Package (DIP)	0 to +70°C	NE555N	0404B
8-Pin Plastic Dual In-Line Package (DIP)	-40°C to +85°C	SA555N	0404B
8-Pin Plastic Small Outline (SO) Package	-40°C to +85°C	SA555D	0174C
8-Pin Hermetic Ceramic Dual In-Line Package (CERDIP)	-55°C to +125°C	SE555CFE	
8-Pin Plastic Dual In-Line Package (DIP)	-55°C to +125°C	SE555CN	0404B
14-Pin Plastic Dual In-Line Package (DIP)	-55°C to +125°C	SE555N	0405B
8-Pin Hermetic Cerdip	-55°C to +125°C	SE555FE	
14-Pin Ceramic Dual In-Line Package (CERDIP)	0 to +70°C	NE555F	0581B
14-Pin Ceramic Dual In-Line Package (CERDIP)	-55°C to +125°C	SE555F	0581B
14-Pin Ceramic Dual In-Line Package (CERDIP)	-55°C to +125°C	SE555CF	0581B

BLOCK DIAGRAM



EQUIVALENT SCHEMATIC



NOTE: Pin numbers are for 8-Pin package

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage		
	SE555	+18	V
	NE555, SE555C, SA555	+16	V
P_D	Maximum allowable power dissipation[1]	600	mW
T_A	Operating ambient temperature range		
	NE555	0 to +70	°C
	SA555	-40 to +85	°C
	SE555, SE555C	-55 to +125	°C
T_{STG}	Storage temperature range	-65 to +150	°C
T_{SOLD}	Lead soldering temperature (10sec max)	+300	°C

NOTES:

1. The junction temperature must be kept below 125°C for the D package and below 150°C for the FE, N and F packages. At ambient temperatures above 25°C, where this limit would be derated by the following factors:
   D package 160°C/W
   FE package 150°C/W
   N package 100°C/W
   F package 105°C/W

DC AND AC ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = +5V to +15 unless otherwise specified.

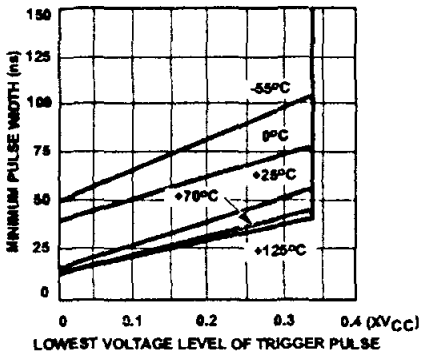
SYMBOL	PARAMETER	TEST CONDITIONS	SE555			NE555/SE555C			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply voltage		4.5		18	4.5		16	V
I_{CC}	Supply current (low state)[1]	V_{CC}=5V, R_L=∞		3	5		3	6	mA
		V_{CC}=15V, R_L=∞		10	12		10	15	mA
	Timing error (monostable)	R_A=2kΩ to 100kΩ							
t_M	Initial accuracy[2]	C=0.1µF		0.5	2.0		1.0	3.0	%
$\Delta t_M/\Delta T$	Drift with temperature			30	100		50	150	ppm/°C
$\Delta t_M/\Delta V_S$	Drift with supply voltage			0.05	0.2		0.1	0.5	%/V
	Timing error (astable)	R_A, R_B=1kΩ to 100kΩ							
t_A	Initial accuracy[2]	C=0.1µF		4	6		5	13	%
$\Delta t_A/\Delta T$	Drift with temperature	V_{CC}=15V			500			500	ppm/°C
$\Delta t_A/\Delta V_S$	Drift with supply voltage			0.15	0.6		0.3	1	%/V
V_C	Control voltage level	V_{CC}=15V	9.6	10.0	10.4	9.0	10.0	11.0	V
		V_{CC}=5V	2.9	3.33	3.8	2.6	3.33	4.0	V
V_{TH}	Threshold voltage	V_{CC}=15V	9.4	10.0	10.6	8.8	10.0	11.2	V
		V_{CC}=5V	2.7	3.33	4.0	2.4	3.33	4.2	V
I_{TH}	Threshold current[3]			0.1	0.25		0.1	0.25	µA
V_{TRIG}	Trigger voltage	V_{CC}=15V	4.8	5.0	5.2	4.5	5.0	5.6	V
		V_{CC}=5V	1.45	1.67	1.9	1.1	1.67	2.2	V
I_{TRIG}	Trigger current	V_{TRIG}=0V		0.5	0.9		0.5	2.0	µA
V_{RESET}	Reset voltage[4]	V_{CC}=15V, V_{TH}=10.5V	0.3		1.0	0.3		1.0	V
I_{RESET}	Reset current	V_{RESET}=0.4V		0.1	0.4		0.1	0.4	mA
	Reset current	V_{RESET}=0V		0.4	1.0		0.4	1.5	mA
V_{OL}	Output voltage (low)	V_{CC}=15V							
		I_{SINK}=10mA		0.1	0.15		0.1	0.25	V
		I_{SINK}=50mA		0.4	0.5		0.4	0.75	V
		I_{SINK}=100mA		2.0	2.2		2.0	2.5	V
		I_{SINK}=200mA		2.5			2.5		V
		V_{CC}=5V							
		I_{SINK}=8mA		0.1	0.25		0.3	0.4	V
		I_{SINK}=5mA		0.05	0.2		0.25	0.35	V
V_{OH}	Output voltage (high)	V_{CC}=15V							
		I_{SOURCE}=200mA		12.5			12.5		V
		I_{SOURCE}=100mA	13.0	13.3		12.75	13.3		V
		V_{CC}=5V							
		I_{SOURCE}=100mA	3.0	3.3		2.75	3.3		V
t_{OFF}	Turn-off time[5]	V_{RESET}=V_{CC}		0.5	2.0		0.5	2.0	µs
t_R	Rise time of output			100	200		100	300	ns
t_F	Fall time of output			100	200		100	300	ns
	Discharge leakage current			20	100		20	100	nA

NOTES:

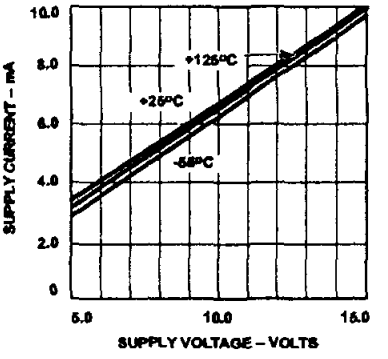
1. Supply current when output high typically 1mA less.
2. Tested at V_{CC}=5V and V_{CC}=15V.
3. This will determine the max value of R_A+R_B, for 15V operation, the max total R=10MΩ, and for 5V operation, the max. total R=3.4MΩ.
4. Specified with trigger input high.
5. Time measured from a positive going input pulse from 0 to 0.8×V_{CC} into the threshold to the drop from high to low of the output. Trigger is tied to threshold.

TYPICAL PERFORMANCE CHARACTERISTICS

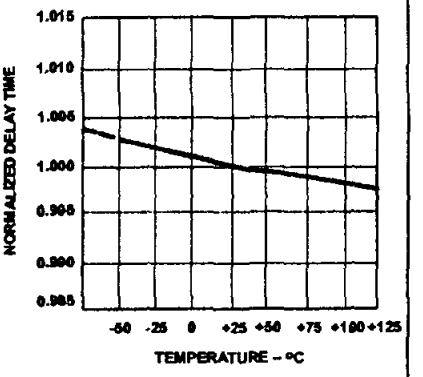
Minimum Pulse Width Required for Triggering



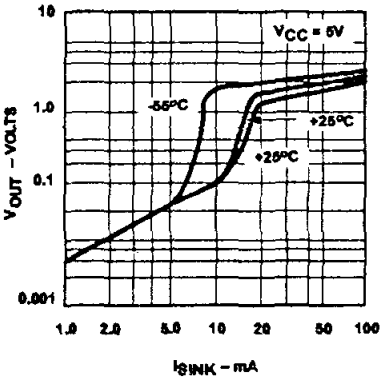
Supply Current vs Supply Voltage



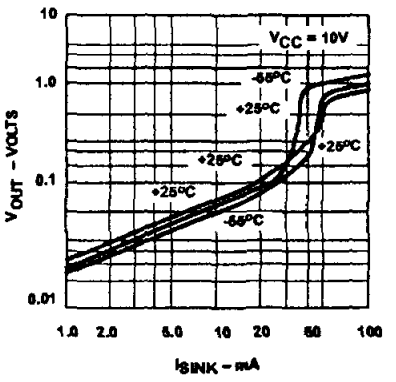
Delay Time vs Temperature



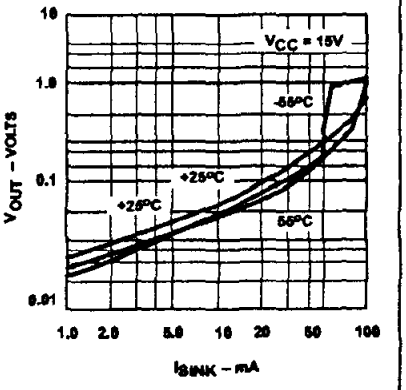
Low Output Voltage vs Output Sink Current



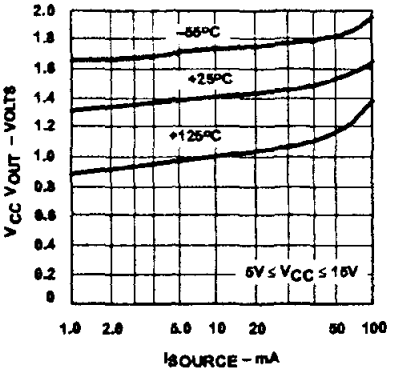
Low Output Voltage vs Output Sink Current



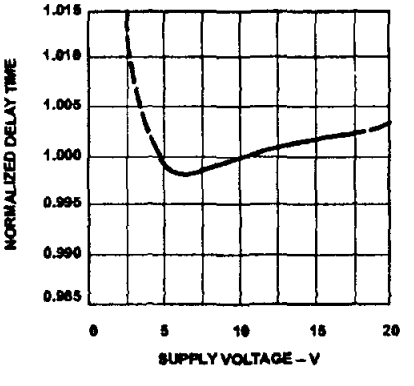
Low Output Voltage vs Output Sink Current



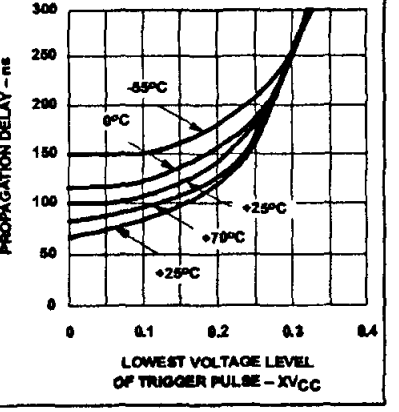
High Output Voltage Drop vs Output Source Current



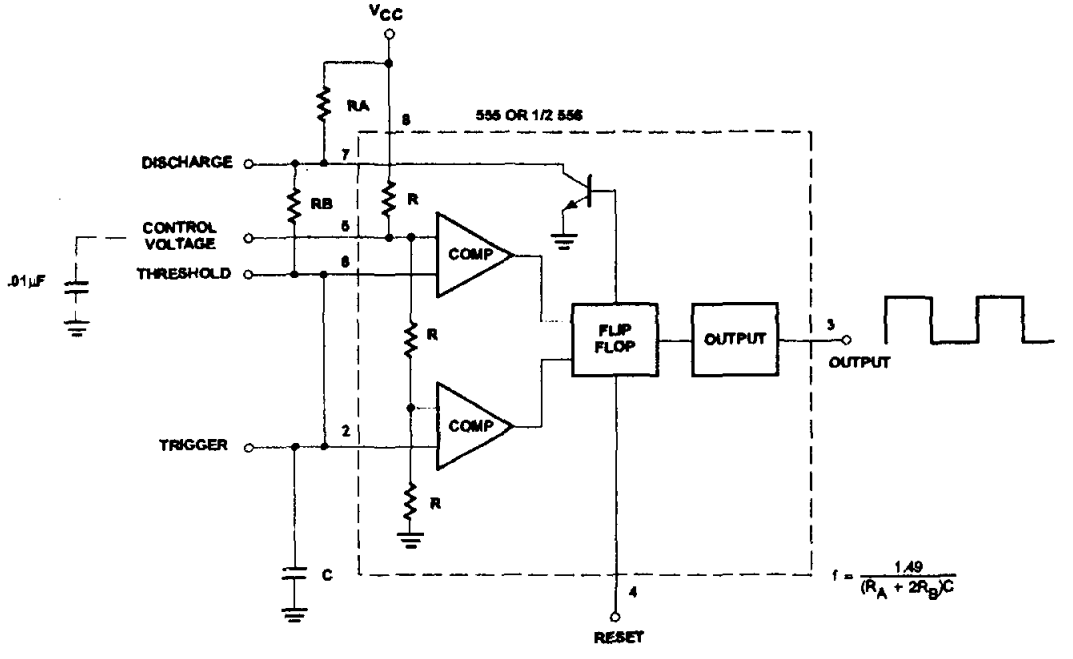
Delay Time vs Supply Voltage



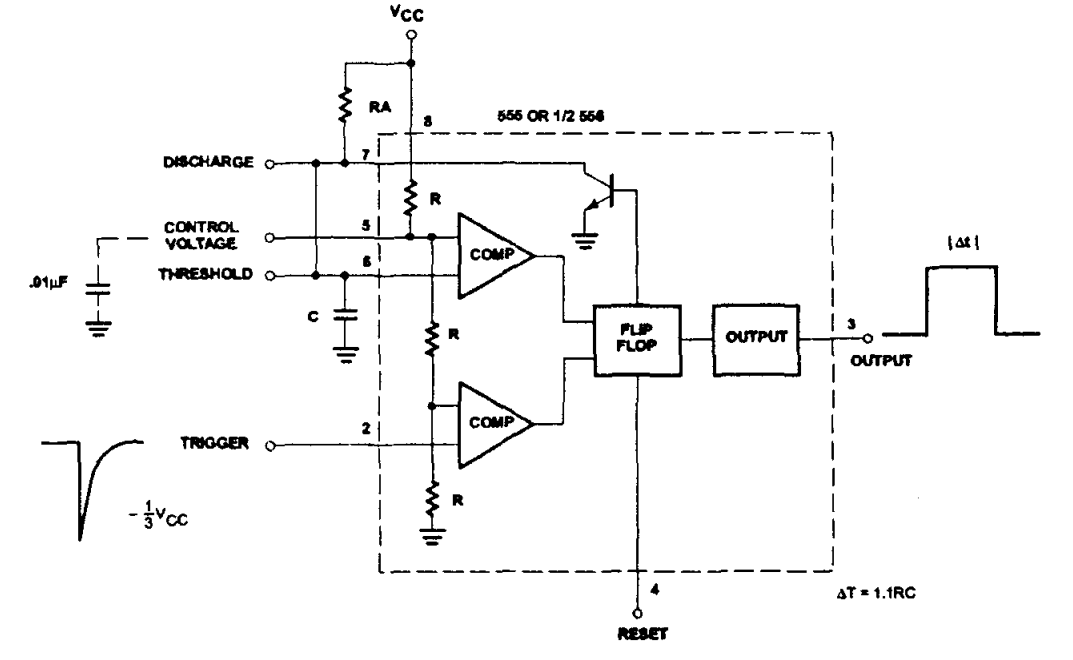
Propagation Delay vs Voltage Level of Trigger Pulse



TYPICAL APPLICATIONS



Astable Operation



Monostable Operation

TYPICAL APPLICATIONS

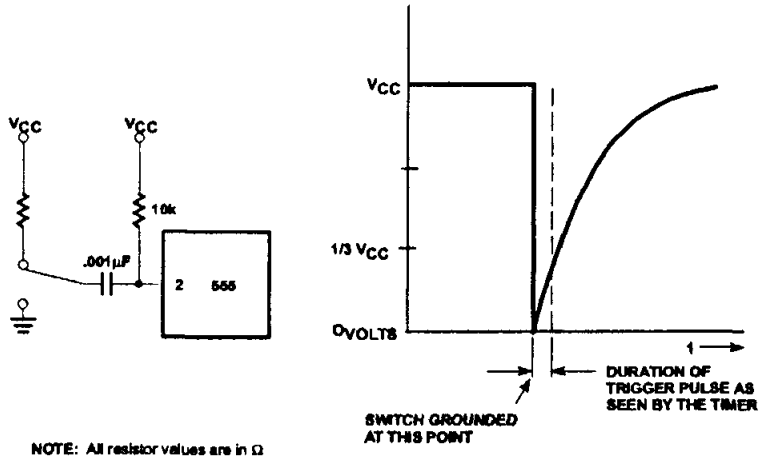


Figure 1. AC Coupling of the Trigger Pulse

Trigger Pulse Width Requirements and Time Delays

Due to the nature of the trigger circuitry, the timer will trigger on the negative going edge of the input pulse. For the device to time out properly, it is necessary that the trigger voltage level be returned to some voltage greater than one third of the supply before the time out period. This can be achieved by making either the trigger pulse sufficiently short or by AC coupling into the trigger. By AC coupling the trigger, see Figure 1, a short negative going pulse is achieved when the trigger signal goes to ground. AC coupling is most frequently used in conjunction with a switch or a signal that goes to ground which initiates the timing cycle. Should the trigger be held low, without AC coupling, for a longer duration than the timing cycle the output will remain in a high state for the duration of the low trigger signal, without regard to the threshold comparator state. This is due to the predominance of Q_{15} on the base of Q_{16}, controlling the state of the bi-stable flip-flop. When the trigger signal then returns to a high level, the output will fall immediately. Thus, the output signal will follow the trigger signal in this case.

Another consideration is the "turn-off time". This is the measurement of the amount of time required after the threshold reaches 2/3 V_{CC} to turn the output low. To explain further, Q_1 at the threshold input turns on after reaching 2/3 V_{CC}, which then turns on Q_5, which turns on Q_6. Current from Q_6 turns on Q_{16} which turns Q_{17} off. This allows current from Q_{19} to turn on Q_{20} and Q_{24} to given an output low. These steps cause the 2µs max. delay as stated in the data sheet.

Also, a delay comparable to the turn-off time is the trigger release time. When the trigger is low, Q_{10} is on and turns on Q_{11} which turns on Q_{15}. Q_{15} turns off Q_{16} and allows Q_{17} to turn on. This turns off current to Q_{20} and Q_{24}, which results in output high. When the trigger is released, Q_{10} and Q_{11} shut off, Q_{15} turns off, Q_{16} turns on and the circuit then follows the same path and time delay explained as "turn off time". This trigger release time is very important in designing the trigger pulse width so as not to interfere with the output signal as explained previously.

FAIRCHILD
SEMICONDUCTOR™

BD135/137/139

Medium Power Linear and Switching Applications

- Complement to BD136, BD138 and BD140 respectively

1 TO-126
1. Emitter 2.Collector 3.Base

NPN Epitaxial Silicon Transistor

Absolute Maximum Ratings T_C=25°C unless otherwise noted

Symbol	Parameter		Value	Units
V_{CBO}	Collector-Base Voltage	: BD135	45	V
		: BD137	60	V
		: BD139	80	V
V_{CEO}	Collector-Emitter Voltage	: BD135	45	V
		: BD137	60	V
		: BD139	80	V
V_{EBO}	Emitter-Base Voltage		5	V
I_C	Collector Current (DC)		1.5	A
I_{CP}	Collector Current (Pulse)		3.0	A
I_B	Base Current		0.5	A
P_C	Collector Dissipation (T_C=25°C)		12.5	W
P_C	Collector Dissipation (T_a=25°C)		1.25	W
T_J	Junction Temperature		150	°C
T_{STG}	Storage Temperature		- 55 ~ 150	°C

Electrical Characteristics T_C=25°C unless otherwise noted

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V_{CEO}(sus)	Collector-Emitter Sustaining Voltage					
	: BD135	I_C = 30mA, I_B = 0	45			V
	: BD137		60			V
	: BD139		80			V
I_{CBO}	Collector Cut-off Current	V_{CB} = 30V, I_E = 0			0.1	µA
I_{EBO}	Emitter Cut-off Current	V_{EB} = 5V, I_C = 0			10	µA
h_{FE1}	DC Current Gain : ALL DEVICE	V_{CE} = 2V, I_C = 5mA	25			
h_{FE2}	: ALL DEVICE	V_{CE} = 2V, I_C = 0.5A	25			
h_{FE3}	: BD135	V_{CE} = 2V, I_C = 150mA	40		250	
	: BD137, BD139		40		160	
V_{CE}(sat)	Collector-Emitter Saturation Voltage	I_C = 500mA, I_B = 50mA			0.5	V
V_{BE}(on)	Base-Emitter ON Voltage	V_{CE} = 2V, I_C = 0.5A			1	V

h_{FE} Classification

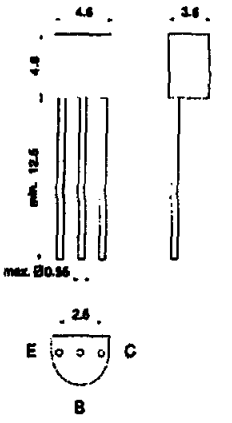
Classification	6	10	16
h_{FE3}	40 ~ 100	63 ~ 160	100 ~ 250

HN 9014

NPN Silicon Expitaxial Planar Transistor
for switching and AF amplifier applications.

The transistor is subdivided into four groups, A, B, C, and D, according to its DC current gain. As complementary type the PNP transistor HN 9015 is recommended.

On special request, these transistors can be manufactured in different pin configurations. Please refer to the "TO-92 TRANSISTOR PACKAGE OUTLINE" on page 80 for the available pin options.



TO-92 Plastic Package
Weight approx. 0.18 g
Dimensions in mm

Absolute Maximum Ratings

	Symbol	Value	Unit
Collector Base Voltage	V_{CBO}	30	V
Collector Emitter Voltage	V_{CES}	30	V
Collector Emitter Voltage	V_{CEO}	30	V
Emitter Base Voltage	V_{EBO}	5	V
Collector Current	I_C	100	mA
Peak Collector Current	I_{CM}	200	mA
Peak Base Current	I_{BM}	200	mA
Peak Emitter Current	$-I_{EM}$	200	mA
Power Dissipation at T_{amb} = 25 °C	P_{tot}	500[1)]	mW
Junction Temperature	T_j	150	°C
Storage Temperature Range	T_S	-65 to +150	°C

1) Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case

G S P FORM A AVAILABLE

Characteristics at T_{amb} = 25 °C

		Symbol	Min.	Typ.	Max.	Unit
DC Current Gain at V_{CE} = 5 V, I_C = 1 mA						
Current Gain Group	A	h_{FE}	60	-	150	-
	B	h_{FE}	100	-	300	-
	C	h_{FE}	200	-	600	-
	D	h_{FE}	400	-	1000	-
Collector Saturation Voltage at I_C = 10 mA, I_B = 0.5 mA at I_C = 100 mA, I_B = 5 mA		 V_{CEsat} V_{CEsat}	 - -	 80 200	 200 600	 mV mV
Base Saturation Voltage at I_C = 10 mA, I_B = 0.5 mA at I_C = 100 mA, I_B = 5 mA		 V_{BEsat} V_{BEsat}	 - -	 700 900	 - -	 mV mV
Base Emitter Voltage at V_{CE} = 5 V, I_C = 2 mA at V_{CE} = 5 V, I_C = 10 mA		 V_{BE} V_{BE}	 580 -	 660 -	 700 750	 mV mV
Collector Cutoff Current at V_{CE} = 30 V at V_{CE} = 30 V, T_j = 125 °C at V_{CB} = 30 V at V_{CB} = 30 V, T_j = 150 °C		 I_{CES} I_{CES} I_{CBO} I_{CBO}	 - - - -	 0.2 - - -	 15 4 15 5	 nA µA nA µA
Gain Bandwidth Product at V_{CE} = 5 V, I_C = 10 mA, f = 100 MHz		f_T	-	300	-	MHz
Collector Base Capacitance at V_{CB} = 10 V, f = 1 MHz		C_{CBO}	-	3.5	6	pF
Emitter Base Capacitance at V_{EB} = 0.5 V, f = 1 MHz		C_{EBO}	-	9	-	pF
Noise Figure at V_{CE} = 5 V, I_C = 200 µA, R_G = 2 kΩ f = 1 kHz, Δf = 200 Hz		F	-	2	10	dB
Thermal Resistance Junction to Ambient		R_{thA}	-	-	250[1]	K/W

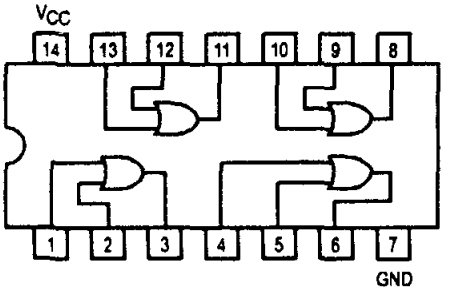
[1] Valid provided that leads are kept at ambient temperature at a distance of 2 mm from case

G S P FORM A AVAILABLE

MOTOROLA

QUAD 2-INPUT OR GATE

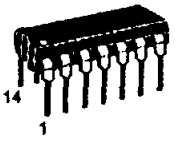
SN54/74LS32



QUAD 2-INPUT OR GATE

LOW POWER SCHOTTKY

J SUFFIX
CERAMIC
CASE 632-08



N SUFFIX
PLASTIC
CASE 646-06

D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

SN54LSXXJ	Ceramic
SN74LSXXN	Plastic
SN74LSXXD	SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Limits Min	Typ	Max	Unit	Test Conditions	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.7	3.5		V		
V_{OL}	Output LOW Voltage	54, 74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Short Circuit Current (Note 1)		−20		−100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current Total, Output HIGH				6.2	mA	V_{CC} = MAX	
	Total, Output LOW				9.8			

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS (T_A = 25°C)

Symbol	Parameter	Limits Min	Typ	Max	Unit	Test Conditions
t_{PLH}	Turn-Off Delay, Input to Output		14	22	ns	V_{CC} = 5.0 V, C_L = 15 pF
t_{PHL}	Turn-On Delay, Input to Output		14	22	ns	

MT8888C

Integrated DTMF Transceiver with Intel Micro Interface

Features

- Central office quality DTMF transmitter/receiver
- Low power consumption
- High speed Intel micro interface
- Adjustable guard time
- Automatic tone burst mode
- Call progress tone detection to -30dBm

Applications

- Credit card systems
- Paging systems
- Repeater systems/mobile radio
- Interconnect dialers
- Personal computers

ISSUE 6 March 1997

Ordering Information

MT8888CE	20 Pin Plastic DIP
MT8888CS	20 Pin SOIC
MT8888CN	24 Pin SSOP

-40°C to +85°C

Description

The MT8888C is a monolithic DTMF transceiver with call progress filter. It is fabricated in CMOS technology offering low power consumption and high reliability.

The receiver section is based upon the industry standard MT8870 DTMF receiver while the transmitter utilizes a switched capacitor D/A converter for low distortion, high accuracy DTMF signalling. Internal counters provide a burst mode such that tone bursts can be transmitted with precise timing. A call progress filter can be selected allowing a microprocessor to analyze call progress tones.

The MT8888C utilizes an Intel micro interface, which allows the device to be connected to a number of popular microcontrollers with minimal external logic.

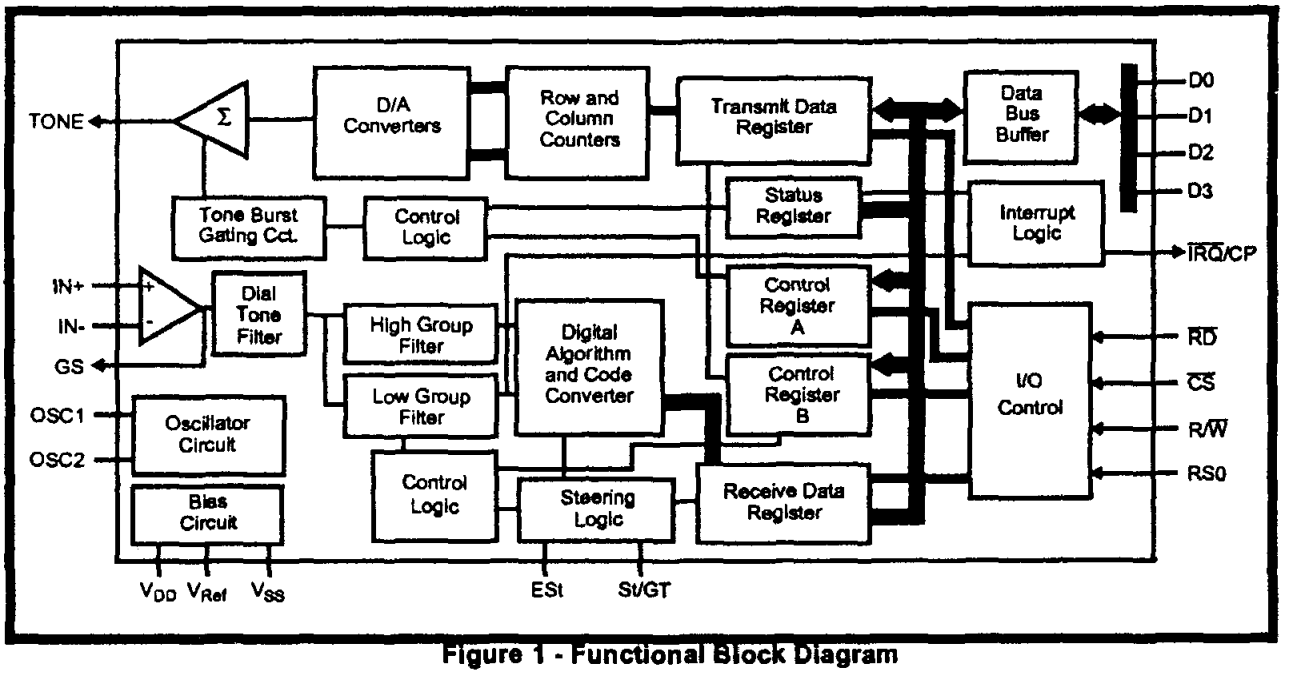


Figure 1 - Functional Block Diagram

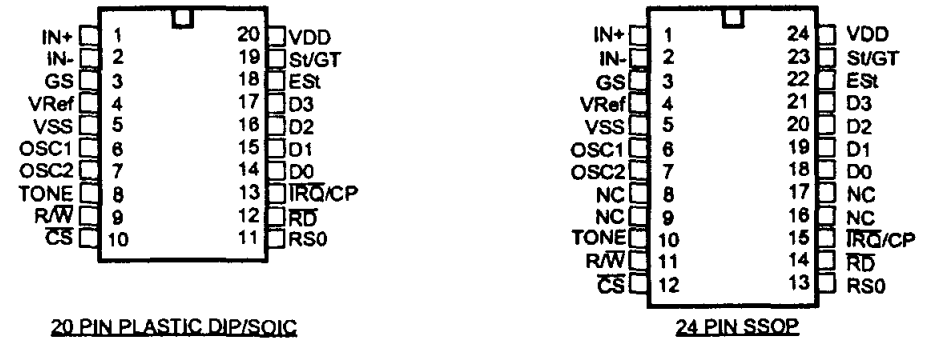


Figure 2 - Pin Connections

Pin Description

Pin #		Name	Description
20	24		
1	1	IN+	**Non-inverting** op-amp input.
2	2	IN-	**Inverting** op-amp input.
3	3	GS	**Gain Select**. Gives access to output of front end differential amplifier for connection of feedback resistor.
4	4	V_{Ref}	**Reference Voltage** output ($V_{DD}/2$).
5	5	V_{SS}	Ground (0V).
6	6	OSC1	**Oscillator** input. This pin can also be driven directly by an external clock.
7	7	OSC2	**Oscillator** output. A 3.579545 MHz crystal connected between OSC1 and OSC2 completes the internal oscillator circuit. Leave open circuit when OSC1 is driven externally.
8	10	TONE	Output from internal DTMF transmitter.
9	11	$\overline{WR}$	**Write** microprocessor input. TTL compatible.
10	12	$\overline{CS}$	**Chip Select** input. Active Low. This signal must be qualified externally by address latch enable (ALE) signal, see Figure 12.
11	13	RS0	**Register Select** input. Refer to Table 3 for bit interpretation. TTL compatible.
12	14	$\overline{RD}$	**Read** microprocessor input. TTL compatible.
13	15	$\overline{IRQ}$/ CP	**Interrupt Request/Call Progress** (open drain) output. In interrupt mode, this output goes low when a valid DTMF tone burst has been transmitted or received. In call progress mode, this pin will output a rectangular signal representative of the input signal applied at the input op-amp. The input signal must be within the bandwidth limits of the call progress filter, see Figure 8.
14-17	18-21	D0-D3	Microprocessor Data Bus. High impedance when $\overline{CS}$ = 1 or $\overline{RD}$ = 1. TTL compatible.
18	22	ESt	**Early Steering** output. Presents a logic high once the digital algorithm has detected a valid tone pair (signal condition). Any momentary loss of signal condition will cause ESt to return to a logic low.
19	23	St/GT	**Steering Input/Guard Time** output (bidirectional). A voltage greater than V_{TSt} detected at St causes the device to register the detected tone pair and update the output latch. A voltage less than V_{TSt} frees the device to accept a new tone pair. The GT output acts to reset the external steering time-constant; its state is a function of ESt and the voltage on St.
20	24	V_{DD}	Positive power supply (5V typ.).
	8,9 16,17	NC	No Connection.

Functional Description

The MT8888C Integrated DTMF Transceiver consists of a high performance DTMF receiver with an internal gain setting amplifier and a DTMF generator which employs a burst counter to synthesize precise tone bursts and pauses. A call progress mode can be selected so that frequencies within the specified passband can be detected. The Intel micro interface allows microcontrollers, such as the 8080, 80C31/51 and 8085, to access the MT8888C internal registers.

Input Configuration

The input arrangement of the MT8888C provides a differential-input operational amplifier as well as a bias source (V_{Ref}), which is used to bias the inputs at $V_{DD}/2$. Provision is made for connection of a feedback resistor to the op-amp output (GS) for gain adjustment. In a single-ended configuration, the input pins are connected as shown in Figure 3.

Figure 4 shows the necessary connections for a differential input configuration.

Receiver Section

Separation of the low and high group tones is achieved by applying the DTMF signal to the inputs of two sixth-order switched capacitor bandpass filters, the bandwidths of which correspond to the low and high group frequencies (see Table 1). These filters incorporate notches at 350 Hz and 440 Hz for exceptional dial tone rejection. Each filter output is followed by a single order switched capacitor filter section, which smooths the signals prior to limiting. Limiting is performed by high-gain comparators which are provided with hysteresis to prevent detection of unwanted low-level signals. The outputs of the comparators provide full rail logic swings at the frequencies of the incoming DTMF signals.

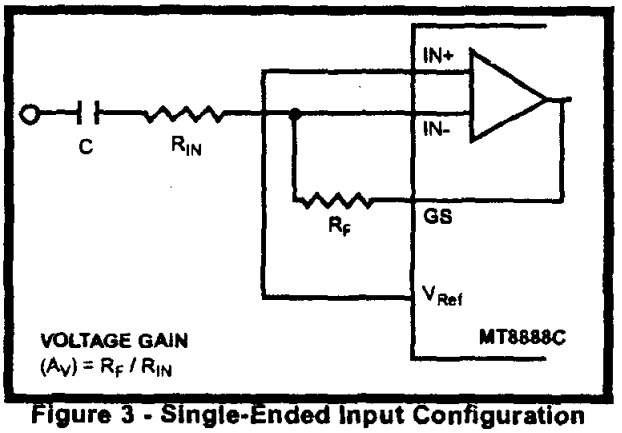


Figure 3 - Single-Ended Input Configuration

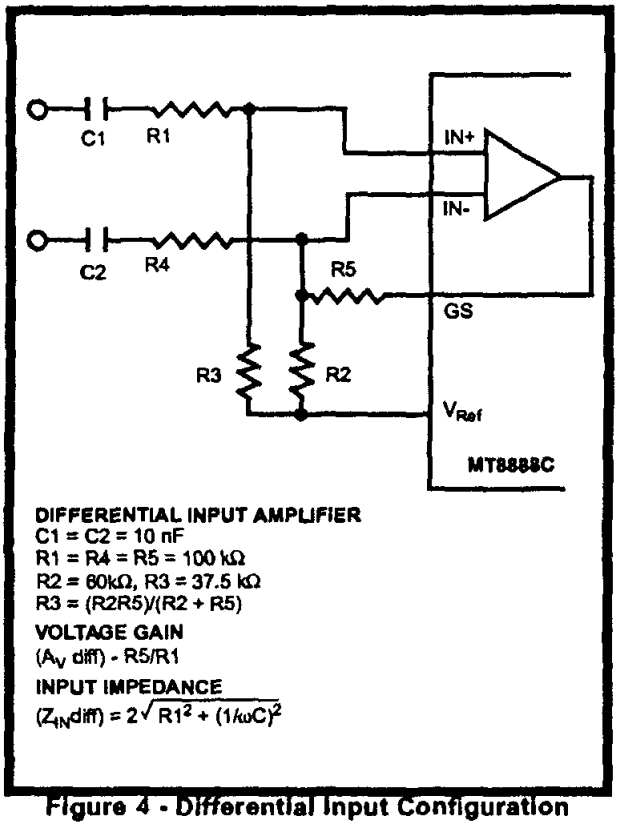


Figure 4 - Differential Input Configuration

F_{LOW}	F_{HIGH}	DIGIT	D_3	D_2	D_1	D_0
697	1209	1	0	0	0	1
697	1336	2	0	0	1	0
697	1477	3	0	0	1	1
770	1209	4	0	1	0	0
770	1336	5	0	1	0	1
770	1477	6	0	1	1	0
852	1209	7	0	1	1	1
852	1336	8	1	0	0	0
852	1477	9	1	0	0	1
941	1336	0	1	0	1	0
941	1209	*	1	0	1	1
941	1477	#	1	1	0	0
697	1633	A	1	1	0	1
770	1633	B	1	1	1	0
852	1633	C	1	1	1	1
941	1633	D	0	0	0	0

0= LOGIC LOW, 1= LOGIC HIGH

Table 1. Functional Encode/Decode Table

Following the filter section is a decoder employing digital counting techniques to determine the frequencies of the incoming tones and to verify that they correspond to standard DTMF frequencies. A complex averaging algorithm protects against tone simulation by extraneous signals such as voice while providing tolerance to small frequency deviations and variations. This averaging algorithm has been developed to ensure an optimum combination of immunity to talk-off and tolerance to the presence of interfering frequencies (third tones) and noise. When the detector recognizes the presence of two valid tones (this is referred to as the "signal condition" in some industry specifications) the "Early Steering" (ESt) output will go to an active state. Any subsequent loss of signal condition will cause ESt to assume an inactive state.

Steering Circuit

Before registration of a decoded tone pair, the receiver checks for a valid signal duration (referred to as character recognition condition). This check is performed by an external RC time constant driven by ESt. A logic high on ESt causes v_c (see Figure 5) to rise as the capacitor discharges. Provided that the signal condition is maintained (ESt remains high) for the validation period (t_{GTP}), v_c reaches the threshold (V_{TSt}) of the steering logic to register the tone pair, latching its corresponding 4-bit code (see Table 1) into the Receive Data Register. At this point the GT output is activated and drives v_c to V_{DD}. GT continues to drive high as long as ESt remains high. Finally, after a short delay to allow the output latch to settle, the delayed steering output flag goes high, signalling that a received tone pair has been registered. The status of the delayed steering flag can be monitored by checking the appropriate bit in the status register. If Interrupt mode has been selected, the $\overline{IRQ}$/CP pin will pull low when the delayed steering flag is active.

The contents of the output latch are updated on an active delayed steering transition. This data is presented to the four bit bidirectional data bus when the Receive Data Register is read. The steering circuit works in reverse to validate the interdigit pause between signals. Thus, as well as rejecting signals too short to be considered valid, the receiver will tolerate signal interruptions (drop out) too short to be considered a valid pause. This facility, together with the capability of selecting the steering time constants externally, allows the designer to tailor performance to meet a wide variety of system requirements.

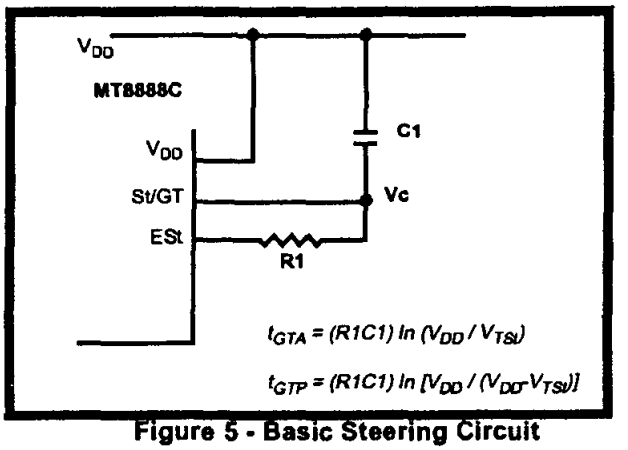


Figure 5 - Basic Steering Circuit

Guard Time Adjustment

The simple steering circuit shown in Figure 5 is adequate for most applications. Component values are chosen according to the following inequalities (see Figure 7):

$$t_{REC} \geq t_{DPmax} + t_{GTPmax} - t_{DAmin}$$
$$t_{REC} \leq t_{DPmin} + t_{GTPmin} - t_{DAmax}$$
$$t_{ID} \geq t_{DAmax} + t_{GTAmax} - t_{DPmin}$$
$$t_{DO} \leq t_{DAmin} + t_{GTAmin} - t_{DPmax}$$

The value of t_{DP} is a device parameter (see AC Electrical Characteristics) and t_{REC} is the minimum signal duration to be recognized by the receiver. A value for C1 of 0.1 µF is recommended for most

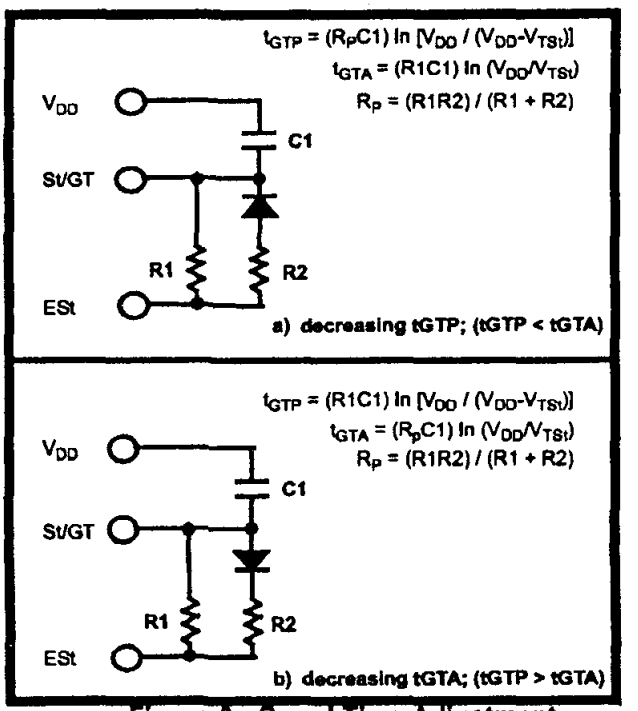


Figure 6 - Guard Time Adjustment

applications, leaving R1 to be selected by the designer. Different steering arrangements may be used to select independent tone present (t_{GTP}) and tone absent (t_{GTA}) guard times. This may be necessary to meet system specifications which place both accept and reject limits on tone duration and interdigital pause. Guard time adjustment also allows the designer to tailor system parameters such as talk off and noise immunity.

Increasing t_{REC} improves talk-off performance since it reduces the probability that tones simulated by speech will maintain a valid signal condition long enough to be registered. Alternatively, a relatively short t_{REC} with a long t_{DO} would be appropriate for extremely noisy environments where fast acquisition time and immunity to tone drop-outs are required. Design information for guard time adjustment is shown in Figure 6. The receiver timing is shown in Figure 7 with a description of the events in Figure 9.

Call Progress Filter

A call progress mode, using the MT8888C, can be selected allowing the detection of various tones, which identify the progress of a telephone call on the network. The call progress tone input and DTMF input are common, however, call progress tones can only be detected when CP mode has been selected. DTMF signals cannot be detected if CP mode has been selected (see Table 7). Figure 8 indicates the useful detect bandwidth of the call progress filter. Frequencies presented to the input, which are within the 'accept' bandwidth limits of the filter, are hard-limited by a high gain comparator with the $\overline{IRQ}$/CP pin serving as the output. The squarewave output obtained from the schmitt trigger can be analyzed by a microprocessor or counter arrangement to determine the nature of the call progress tone being detected. Frequencies which are in the 'reject' area will not be detected and consequently the $\overline{IRQ}$/CP pin will remain low.

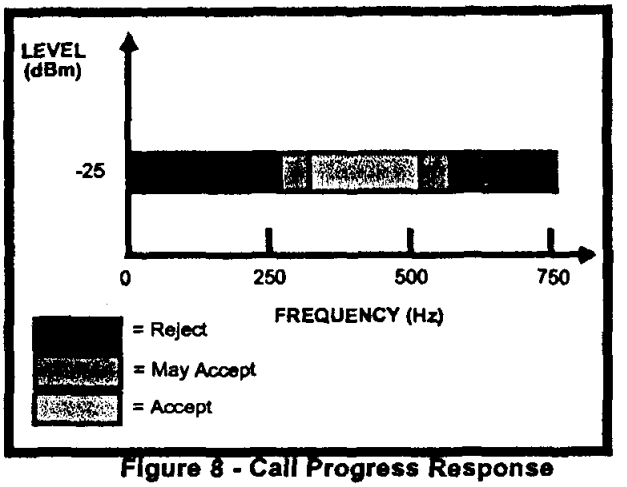


Figure 8 - Call Progress Response

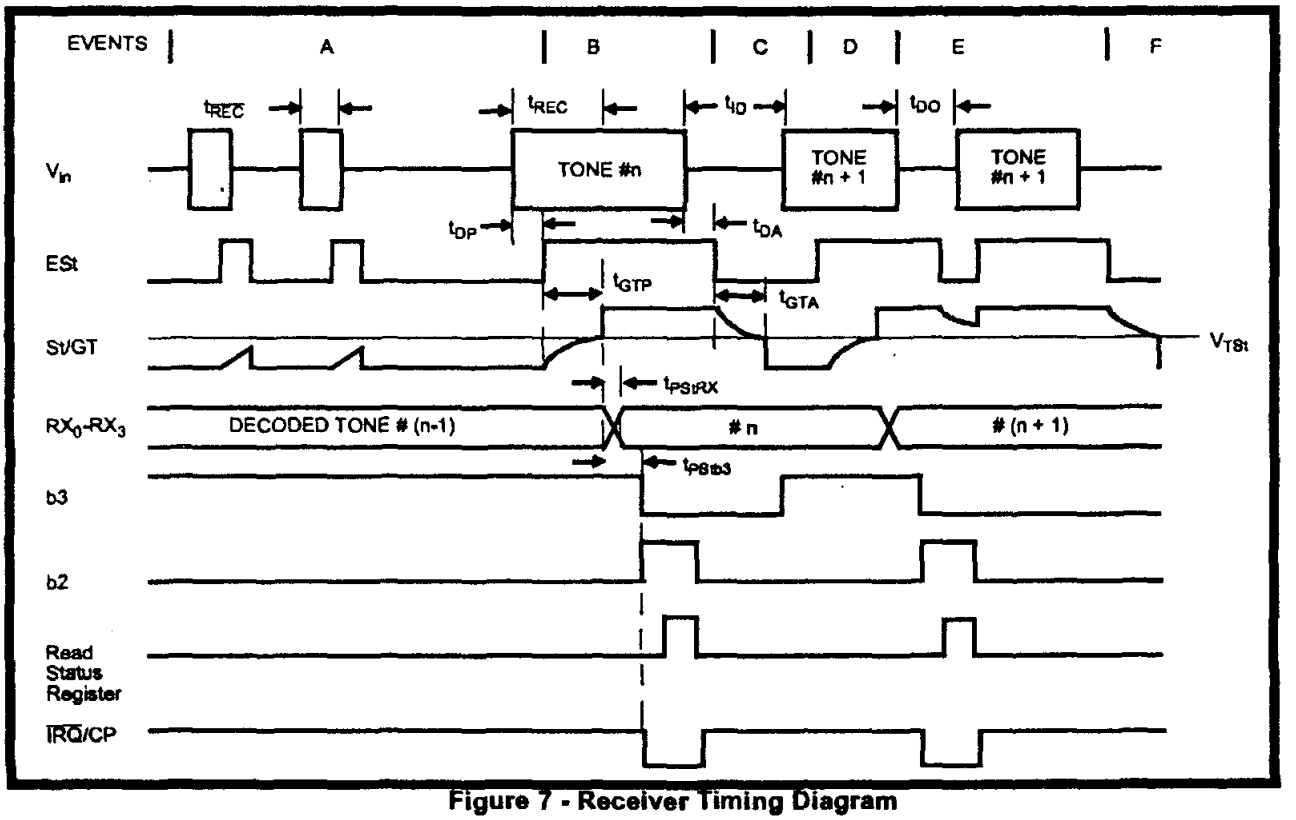


Figure 7 - Receiver Timing Diagram

EXPLANATION OF EVENTS

A) TONE BURSTS DETECTED, TONE DURATION INVALID, RX DATA REGISTER NOT UPDATED.
B) TONE #n DETECTED, TONE DURATION VALID, TONE DECODED AND LATCHED IN RX DATA REGISTER.
C) END OF TONE #n DETECTED, TONE ABSENT DURATION VALID, INFORMATION IN RX DATA REGISTER RETAINED UNTIL NEXT VALID TONE PAIR.
D) TONE #n+1 DETECTED, TONE DURATION VALID, TONE DECODED AND LATCHED IN RX DATA REGISTER.
E) ACCEPTABLE DROPOUT OF TONE #n+1, TONE ABSENT DURATION INVALID, DATA REMAINS UNCHANGED.
F) END OF TONE #n+1 DETECTED, TONE ABSENT DURATION VALID, INFORMATION IN RX DATA REGISTER RETAINED UNTIL NEXT VALID TONE PAIR.

EXPLANATION OF SYMBOLS

V_{in}	DTMF COMPOSITE INPUT SIGNAL.
ESt	EARLY STEERING OUTPUT. INDICATES DETECTION OF VALID TONE FREQUENCIES.
St/GT	STEERING INPUT/GUARD TIME OUTPUT. DRIVES EXTERNAL RC TIMING CIRCUIT.
RX_0-RX_3	4-BIT DECODED DATA IN RECEIVE DATA REGISTER
b3	DELAYED STEERING. INDICATES THAT VALID FREQUENCIES HAVE BEEN PRESENT/ABSENT FOR THE REQUIRED GUARD TIME THUS CONSTITUTING A VALID SIGNAL. ACTIVE LOW FOR THE DURATION OF A VALID DTMF SIGNAL.
b2	INDICATES THAT VALID DATA IS IN THE RECEIVE DATA REGISTER. THE BIT IS CLEARED AFTER THE STATUS REGISTER IS READ.
$\overline{IRQ}$/CP	INTERRUPT IS ACTIVE INDICATING THAT NEW DATA IS IN THE RX DATA REGISTER. THE INTERRUPT IS CLEARED AFTER THE STATUS REGISTER IS READ.
t_{REC}	MAXIMUM DTMF SIGNAL DURATION NOT DETECTED AS VALID.
$t_{\overline{REC}}$	MINIMUM DTMF SIGNAL DURATION REQUIRED FOR VALID RECOGNITION.
t_{ID}	MINIMUM TIME BETWEEN VALID SEQUENTIAL DTMF SIGNALS.
t_{DO}	MAXIMUM ALLOWABLE DROPOUT DURING VALID DTMF SIGNAL.
t_{DP}	TIME TO DETECT VALID FREQUENCIES PRESENT.
t_{DA}	TIME TO DETECT VALID FREQUENCIES ABSENT.
t_{GTP}	GUARD TIME, TONE PRESENT.
t_{GTA}	GUARD TIME, TONE ABSENT.

Figure 9 - Description of Timing Events

DTMF Generator

The DTMF transmitter employed in the MT8888C is capable of generating all sixteen standard DTMF tone pairs with low distortion and high accuracy. All frequencies are derived from an external 3.579545 MHz crystal. The sinusoidal waveforms for the individual tones are digitally synthesized using row and column programmable dividers and switched capacitor D/A converters. The row and column tones are mixed and filtered providing a DTMF signal with low total harmonic distortion and high accuracy. To specify a DTMF signal, data conforming to the encoding format shown in Table 1 must be written to the transmit Data Register. Note that this is the same as the receiver output code. The individual tones which are generated (f_{LOW} and f_{HIGH}) are referred to as Low Group and High Group tones. As seen from the table, the low group frequencies are 697, 770, 852 and 941 Hz. The high group frequencies are 1209, 1336, 1477 and 1633 Hz. Typically, the high group to low group amplitude ratio (twist) is 2 dB to com-pensate for high group attenuation on long loops.

The period of each tone consists of 32 equal time segments. The period of a tone is controlled by varying the length of these time segments. During write operations to the Transmit Data Register the 4 bit data on the bus is latched and converted to 2 of 8 coding for use by the programmable divider circuitry. This code is used to specify a time segment length, which will ultimately determine the frequency of the tone. When the divider reaches the appropriate count, as determined by the input code, a reset pulse is issued and the counter starts again. The number of time segments is fixed at 32, however, by varying the segment length as described above the frequency can also be varied. The divider output clocks another counter, which addresses the sinewave lookup ROM.

The lookup table contains codes which are used by the switched capacitor D/A converter to obtain discrete and highly accurate DC voltage levels. Two identical circuits are employed to produce row and column tones, which are then mixed using a low noise summing amplifier. The oscillator described needs no "start-up" time as in other DTMF generators since the crystal oscillator is running continuously thus providing a high degree of tone burst accuracy. A bandwidth limiting filter is incorporated and serves to attenuate distortion products above 8 kHz. It can be seen from Figure 8 that the distortion products are very low in amplitude.

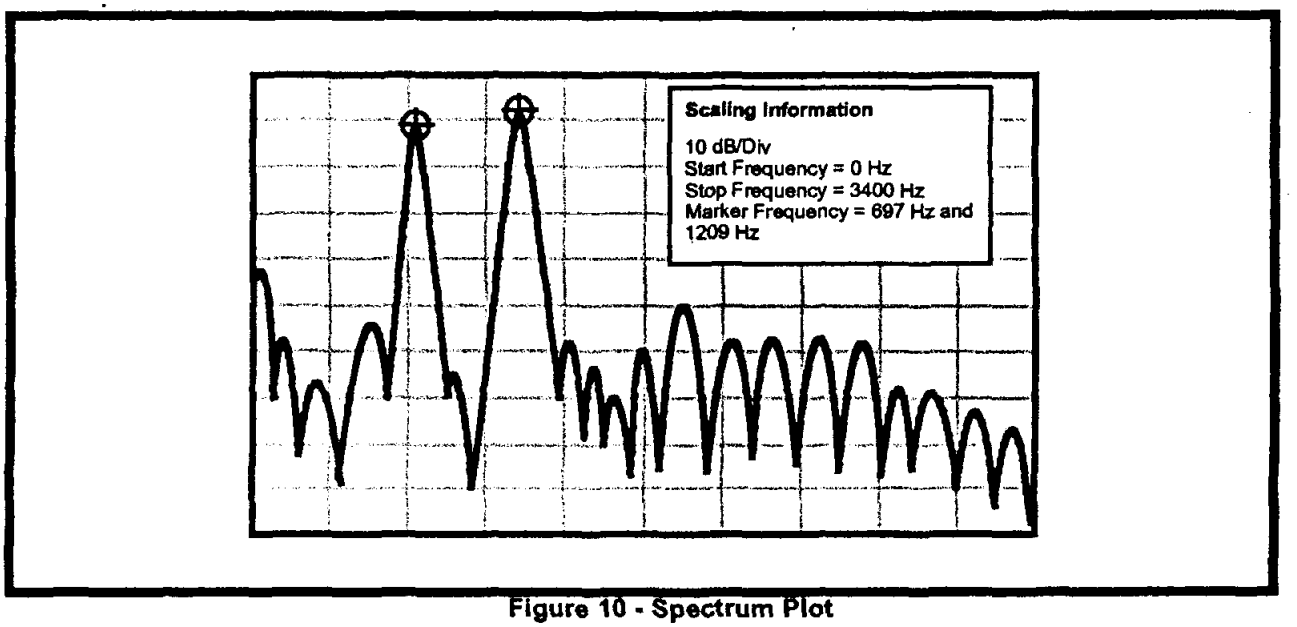


Figure 10 - Spectrum Plot

Burst Mode

In certain telephony applications it is required that DTMF signals being generated are of a specific duration determined either by the particular application or by any one of the exchange transmitter specifications currently existing. Standard DTMF signal timing can be accomplished by making use of the Burst Mode. The transmitter is capable of issuing symmetric bursts/pauses of predetermined duration. This burst/pause duration is 51 ms±1 ms, which is a standard interval for autodialer and central office applications. After the burst/pause has been issued, the appropriate bit is set in the Status Register indicating that the transmitter is ready for more data. The timing described above is available when DTMF mode has been selected. However, when CP mode (Call Progress mode) is selected, the burst/pause duration is doubled to 102 ms ±2 ms. Note that when CP mode and Burst mode have been selected, DTMF tones may be transmitted only and *not* received. In applications where a non-standard burst/pause time is desirable, a software timing loop or external timer can be used to provide the timing pulses when the burst mode is disabled by enabling and disabling the transmitter.

Single Tone Generation

A single tone mode is available whereby individual tones from the low group or high group can be generated. This mode can be used for DTMF test equipment applications, acknowledgment tone generation and distortion measurements. Refer to Control Register B description for details.

ACTIVE INPUT	OUTPUT FREQUENCY (Hz)		%ERROR
	SPECIFIED	ACTUAL	
L1	697	699.1	+0.30
L2	770	766.2	-0.49
L3	852	847.4	-0.54
L4	941	948.0	+0.74
H1	1209	1215.9	+0.57
H2	1336	1331.7	-0.32
H3	1477	1471.9	-0.35
H4	1633	1645.0	+0.73

Table 2. Actual Frequencies Versus Standard Requirements

Distortion Calculations

The MT8888C is capable of producing precise tone bursts with minimal error in frequency (see Table 2). The internal summing amplifier is followed by a first-order lowpass switched capacitor filter to minimize harmonic components and intermodulation products. The total harmonic distortion for a *single tone* can be calculated using Equation 1, which is the ratio of the total power of all the extraneous frequencies to the power of the fundamental frequency expressed as a percentage.

$$THD\ (\%) = 100 \frac{\left(\sqrt{V_{2f}^2 + V_{3f}^2 + V_{4f}^2 + \ldots . V_{nf}^2}\right)}{V_{fundamental}}$$

Equation 1. THD (%) For a Single Tone

The Fourier components of the tone output correspond to V_{2f}.... V_{nf} as measured on the output waveform. The total harmonic distortion for a *dual tone* can be calculated using Equation 2. V_L and V_H correspond to the low group amplitude and high group amplitude, respectively and V^2_{IMD} is the sum of all the intermodulation components. The internal switched-capacitor filter following the D/A converter keeps distortion products down to a very low level as shown in Figure 10.

$$THD\ (\%) = 100 \frac{\sqrt{V^2_{2L} + V^2_{3L} + ... V^2_{nL} + V^2_{2H} + V^2_{3H} + .. V^2_{nH} + V^2_{IMD}}}{\sqrt{V^2_L + V^2_H}}$$

Equation 2. THD (%) For a Dual Tone

DTMF Clock Circuit

The internal clock circuit is completed with the addition of a standard television colour burst crystal. The crystal specification is as follows:

Frequency:	3.579545 MHz
Frequency Tolerance:	±0.1%
Resonance Mode:	Parallel
Load Capacitance:	18pF
Maximum Series Resistance:	150 ohms
Maximum Drive Level:	2mW

e.g. CTS Knights MP036S
Toyocom TQC-203-A-9S

A number of MT8888C devices can be connected as shown in Figure 11 such that only one crystal is required. Alternatively, the OSC1 inputs on all devices can be driven from a TTL buffer with the OSC2 outputs left unconnected.

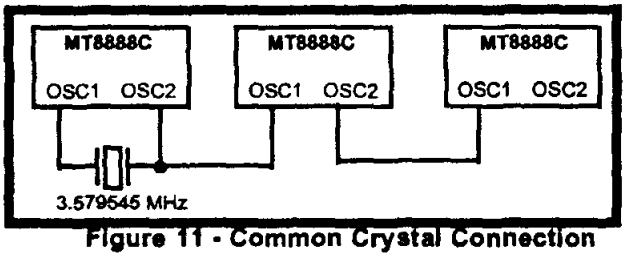


Figure 11 - Common Crystal Connection

Microprocessor Interface

The MT8888C incorporates an Intel microprocessor interface which is compatible with fast versions (16 MHz) of the 80C51. No wait cycles need to be inserted.

Figures 17 and 18 are the timing diagrams for the Intel 8031, 8051 and 8085 (5 MHz) microcontrollers. By NANDing the address latch enable (ALE) output with the high-byte address (P2) decode output, $\overline{CS}$ is generated. Figure 12 summarizes the connection of these Intel processors to the MT8888C transceiver.

The microprocessor interface provides access to five internal registers. The read-only Receive Data Register contains the decoded output of the last valid DTMF digit received. Data entered into the write-only Transmit Data Register will determine which tone pair is to be generated (see Table 1 for coding details). Transceiver control is accomplished with two control registers (see Tables 6 and 7), CRA and CRB, which have the same address. A write operation to CRB is executed by first setting the most significant bit (b3) in CRA. The following write operation to the same address will then be directed to CRB, and subsequent write cycles will be directed back to CRA. The read-only status register indicates the current transceiver state (see Table 8).

A software reset must be included at the beginning of all programs to initialize the control registers upon power-up or power reset (see Figure 17). Refer to Tables 4-7 for bit descriptions of the two control registers.

The multiplexed $\overline{IRQ}$/CP pin can be programmed to generate an interrupt upon validation of DTMF signals or when the transmitter is ready for more data (burst mode only). Alternatively, this pin can be configured to provide a squarewave output of the call progress signal. The $\overline{IRQ}$/CP pin is an open drain output and requires an external pull-up resistor (see Figure 13).

RS0	$\overline{WR}$	$\overline{RD}$	FUNCTION
0	0	1	Write to Transmit Data Register
0	1	0	Read from Receive Data Register
1	0	1	Write to Control Register
1	1	0	Read from Status Register

Table 3. Internal Register Functions

b3	b2	b1	b0
RSEL	IRQ	CP/DTMF	TOUT

Table 4. CRA Bit Positions

b3	b2	b1	b0
C/R	S/D	TEST	BURST ENABLE

Table 5. CRB Bit Positions

BIT	NAME	DESCRIPTION
b0	TOUT	Tone Output Control. A logic high enables the tone output; a logic low turns the tone output off. This bit controls all transmit tone functions.
b1	CP/$\overline{\text{DTMF}}$	Call Progress or DTMF Mode Select. A logic high enables the receive call progress mode; a logic low enables DTMF mode. In DTMF mode the device is capable of receiving and transmitting DTMF signals. In CP mode a rectangular wave representation of the received tone signal will be present on the $\overline{\text{IRQ}}$/CP output pin if IRQ has been enabled (control register A, b2=1). In order to be detected, CP signals must be within the bandwidth specified in the AC Electrical Characteristics for Call Progress. Note: DTMF signals cannot be detected when CP mode is selected.
b2	IRQ	Interrupt Enable. A logic high enables the interrupt function; a logic low de-activates the interrupt function. When IRQ is enabled and DTMF mode is selected (control register A, b1=0), the $\overline{\text{IRQ}}$/CP output pin will go low when either 1) a valid DTMF signal has been received for a valid guard time duration, or 2) the transmitter is ready for more data (burst mode only).
b3	RSEL	Register Select. A logic high selects control register B for the next write cycle to the control register address. After writing to control register B, the following control register write cycle will be directed to control register A.

Table 6. Control Register A Description

BIT	NAME	DESCRIPTION
b0	$\overline{\text{BURST}}$	Burst Mode Select. A logic high de-activates burst mode; a logic low enables burst mode. When activated, the digital code representing a DTMF signal (see Table 1) can be written to the transmit register, which will result in a transmit DTMF tone burst and pause of equal durations (typically 51 msec.). Following the pause, the status register will be updated (b1 - Transmit Data Register Empty), and an interrupt will occur if the interrupt mode has been enabled. When CP mode (control register A, b1) is enabled the normal tone burst and pause durations are extended from a typical duration of 51 msec to 102 msec. When $\overline{\text{BURST}}$ is high (de-activated) the transmit tone burst duration is determined by the TOUT bit (control register A, b0).
b1	TEST	Test Mode Control. A logic high enables the test mode; a logic low de-activates the test mode. When TEST is enabled and DTMF mode is selected (control register A, b1=0), the signal present on the $\overline{\text{IRQ}}$/CP pin will be analogous to the state of the DELAYED STEERING bit of the status register (see Figure 7, signal b3).
b2	S/$\overline{\text{D}}$	Single or Dual Tone Generation. A logic high selects the single tone output; a logic low selects the dual tone (DTMF) output. The single tone generation function requires further selection of either the row or column tones (low or high group) through the C/$\overline{\text{R}}$ bit (control register B, b3).
b3	C/$\overline{\text{R}}$	Column or Row Tone Select. A logic high selects a column tone output; a logic low selects a row tone output. This function is used in conjunction with the S/$\overline{\text{D}}$ bit (control register B, b2).

Table 7. Control Register B Description

BIT	NAME	STATUS FLAG SET	STATUS FLAG CLEARED
b0	IRQ	Interrupt has occurred. Bit one (b1) or bit two (b2) is set.	Interrupt is inactive. Cleared after Status Register is read.
b1	TRANSMIT DATA REGISTER EMPTY (BURST MODE ONLY)	Pause duration has terminated and transmitter is ready for new data.	Cleared after Status Register is read or when in non-burst mode.
b2	RECEIVE DATA REGISTER FULL	Valid data is in the Receive Data Register.	Cleared after Status Register is read.
b3	$\overline{\text{DELAYED STEERING}}$	Set upon the valid detection of the absence of a DTMF signal.	Cleared upon the detection of a valid DTMF signal.

Table 8. Status Register Description

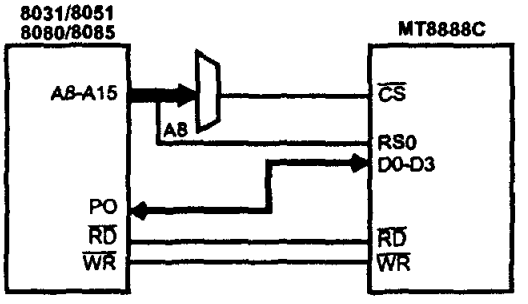
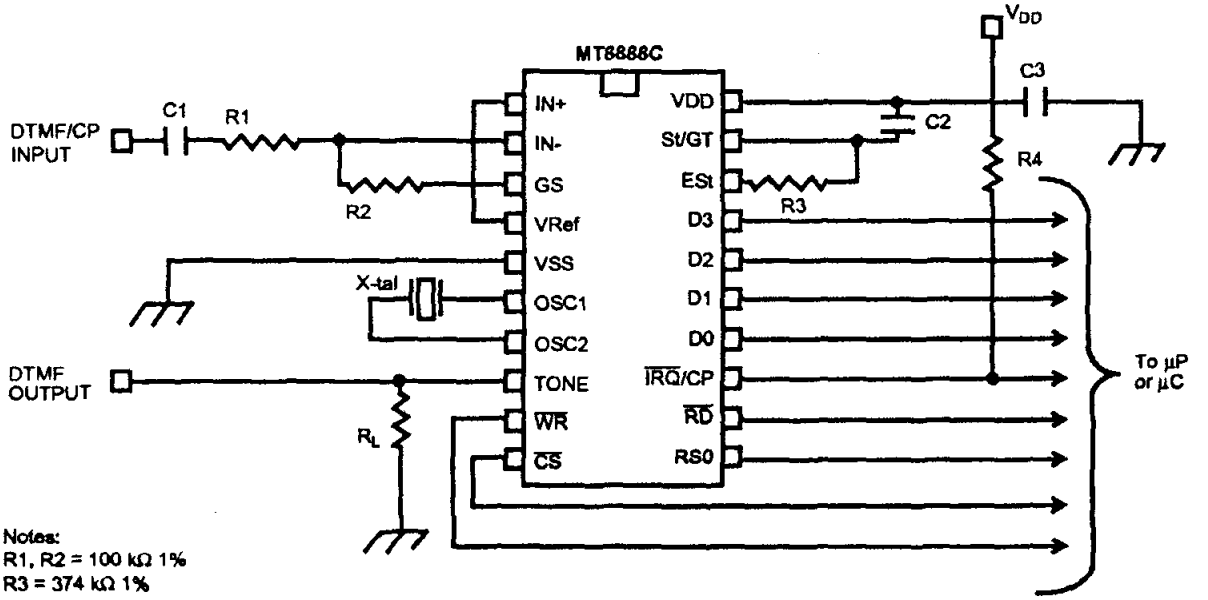


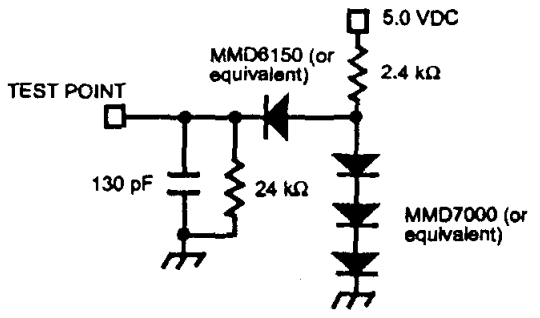
Figure 12 - MT8888C Interface Connections for Various Intel Micros



Notes:
R1, R2 = 100 kΩ 1%
R3 = 374 kΩ 1%
R4 = 3.3 kΩ 10%
R_L = 10 k Ω (min.)
C1 = 100 nF 5%
C2 = 100 nF 5%
C3 = 100 nF 10%*
X-tal = 3.579545 MHz

* Microprocessor based systems can inject undesirable noise into the supply rails. The performance of the MT8888C can be optimized by keeping noise on the supply rails to a minimum. The decoupling capacitor (C3) should be connected close to the device and ground loops should be avoided.

Figure 13 - Application Circuit (Single-Ended Input)



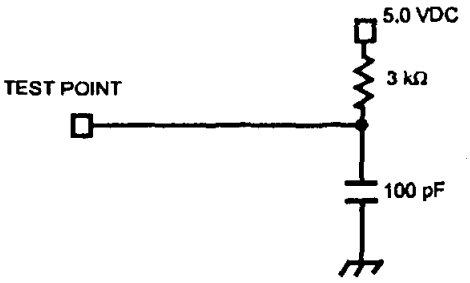


Figure 14 - Test Circuits

INITIALIZATION PROCEDURE

A software reset must be included at the beginning of all programs to initialize the control registers after power up. The initialization procedure should be implemented 100ms after power up.

Description:	**Control**			**Data**			
	RS0	**$\overline{WR}$**	**$\overline{RD}$**	**b3**	**b2**	**b1**	**b0**
1) Read Status Register	1	1	0	X	X	X	X
2) Write to Control Register	1	0	1	0	0	0	0
3) Write to Control Register	1	0	1	0	0	0	0
4) Write to Control Register	1	0	1	1	0	0	0
5) Write to Control Register	1	0	1	0	0	0	0
6) Read Status Register	1	1	0	X	X	X	X

TYPICAL CONTROL SEQUENCE FOR BURST MODE APPLICATIONS

Transmit DTMF tones of 50 ms burst/50 ms pause and Receive DTMF Tones.

Sequence:

	RS0	**$\overline{WR}$**	**$\overline{RD}$**	**b3**	**b2**	**b1**	**b0**
1) Write to Control Register A (tone out, DTMF, $\overline{IRQ}$, Select Control Register B)	1	0	1	1	1	0	1
2) Write to Control Register B (burst mode)	1	0	1	0	0	0	0
3) Write to Transmit Data Register (send a digit 7)	0	0	1	0	1	1	1
4) Wait for an interrupt or poll Status Register							
5) Read the Status Register	1	1	0	X	X	X	X
-if bit 1 is set, the Tx is ready for the next tone, in which case...							
Write to Transmit Register (send a digit 5)	0	0	1	0	1	0	1
-if bit 2 is set, a DTMF tone has been received, in which case....							
Read the Receive Data Register	0	1	0	X	X	X	X
-if both bits are set...							
Read the Receive Data Register	0	1	0	X	X	X	X
Write to Transmit Data Register	0	0	1	0	1	0	1

NOTE: IN THE TX BURST MODE, STATUS REGISTER BIT 1 WILL NOT BE SET UNTIL 100 ms (±2 ms) AFTER THE DATA IS WRITTEN TO THE TX DATA REGISTER. IN EXTENDED BURST MODE THIS TIME WILL BE DOUBLED TO 200 ms (± 4 ms).

Figure 15 - Application Notes

Absolute Maximum Ratings*

	Parameter	Symbol	Min	Max	Units
1	Power supply voltage V_{DD}-V_{SS}	V_{DD}		6	V
2	Voltage on any pin	V_I	V_{SS}-0.3	V_{DD}+0.3	V
3	Current at any pin (Except V_{DD} and V_{SS})			10	mA
4	Storage temperature	T_{ST}	-65	+150	°C
5	Package power dissipation	P_D		1000	mW

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Parameter	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Positive power supply	V_{DD}	4.75	5.00	5.25	V	
2	Operating temperature	T_O	-40		+85	°C	
3	Crystal clock frequency	f_{CLK}	3.575965	3.579545	3.583124	MHz	

‡ Typical figures are at 25 °C and for design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics† - V_{SS}=0 V.

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	SUP	Operating supply voltage	V_{DD}	4.75	5.0	5.25	V	
2		Operating supply current	I_{DD}		7.0	11	mA	
3		Power consumption	P_C			57.8	mW	
4	INPUTS	High level input voltage (OSC1)	V_{IHO}	3.5			V	Note 9*
5		Low level input voltage (OSC1)	V_{ILO}			1.5	V	Note 9*
6		Steering threshold voltage	V_{TSt}	2.2	2.3	2.5	V	V_{DD}=5V
7	OUTPUTS	Low level output voltage (OSC2)	V_{OLO}			0.1	V	No load Note 9*
8		High level output voltage (OSC2)	V_{OHO}	4.9			V	No load Note 9*
9		Output leakage current (IRQ)	I_{OZ}		1	10	µA	V_{OH}=2.4 V
10		V_{Ref} output voltage	V_{Ref}	2.4	2.5	2.6	V	No load, V_{DD}=5V
11		V_{Ref} output resistance	R_{OR}		1.3		kΩ	
12	Digital	Low level input voltage	V_{IL}			0.8	V	
13		High level input voltage	V_{IH}	2.0			V	
14		Input leakage current	I_{IZ}			10	µA	V_{IN}=V_{SS} to V_{DD}
15	Data Bus	Source current	I_{OH}	-1.4	-6.6		mA	V_{OH}=2.4V
16		Sink current	I_{OL}	2.0	4.0		mA	V_{OL}=0.4V
17	ESt and St/Gt	Source current	I_{OH}	-0.5	-3.0		mA	V_{OH}=4.6V
18		Sink current	I_{OL}	2	4		mA	V_{OL}=0.4V
19	IRQ/CP	Sink current	I_{OL}	4	16		mA	V_{OL}=0.4V

† Characteristics are over recommended operating conditions unless otherwise stated.
‡ Typical figures are at 25 °C, V_{DD} =5V and for design aid only: not guaranteed and not subject to production testing.
* See "Notes" following AC Electrical Characteristics Tables.

Electrical Characteristics

Gain Setting Amplifier - Voltages are with respect to ground (V_{SS}) unless otherwise stated, V_{SS}= 0V.

	Characteristics	Sym	Min	Typ	Max	Units	Test Conditions
1	Input leakage current	I_{IN}			100	nA	$V_{SS} \le V_{IN} \le V_{DD}$
2	Input resistance	R_{IN}	10			MΩ	
3	Input offset voltage	V_{OS}			25	mV	
4	Power supply rejection	PSRR	50			dB	1 kHz
5	Common mode rejection	CMRR	40			dB	
6	DC open loop voltage gain	A_{VOL}	40			dB	C_L = 20p
7	Unity gain bandwidth	BW	1.0			MHz	C_L = 20p
8	Output voltage swing	V_O	0.5		V_{DD}-0.5	V	$R_L \ge 100$ kΩ to V_{SS}
9	Allowable capacitive load (GS)	C_L			100	pF	PM>40°
10	Allowable resistive load (GS)	R_L	50			kΩ	V_O = 4Vpp
11	Common mode range	V_{CM}	1.0		V_{DD}-1.0	V	R_L = 50kΩ

Figures are for design aid only: not guaranteed and not subject to production testing.
Characteristics are over recommended operating conditions unless otherwise stated.

MT8888C AC Electrical Characteristics† - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

		Characteristics	Sym	Min	Typ‡	Max	Units	Notes*
1	RX	Valid input signal levels (each tone of composite signal)		-29		+1	dBm	1,2,3,5,6
				27.5		869	mV_{RMS}	1,2,3,5,6

† Characteristics are over recommended operating conditions (unless otherwise stated) using the test circuit shown in Figure 13.

AC Electrical Characteristics† - Voltages are with respect to ground (V_{SS}) unless otherwise stated. f_C=3.579545 MHz

		Characteristics	Sym	Min	Typ‡	Max	Units	Notes*
1	RX	Positive twist accept				8	dB	2,3,6,9
2		Negative twist accept				8	dB	2,3,6,9
3		Freq. deviation accept		±1.5%± 2Hz				2,3,5
4		Freq. deviation reject		±3.5%				2,3,5
5		Third tone tolerance			-16		dB	2,3,4,5,9,10
6		Noise tolerance			-12		dB	2,3,4,5,7,9,10
7		Dial tone tolerance			22		dB	2,3,4,5,8,9

† Characteristics are over recommended operating conditions unless otherwise stated.
‡ Typical figures are at 25°C, V_{DD} = 5V, and for design aid only: not guaranteed and not subject to production testing.
* *See "Notes" following AC Electrical Characteristics Tables.

AC Electrical Characteristics†- Call Progress - Voltages are with respect to ground (V_{SS}), unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Conditions
1	Accept Bandwidth	f_A	310		500	Hz	@ -25 dBm, Note 9
2	Lower freq. (REJECT)	f_{LR}		290		Hz	@ -25 dBm
3	Upper freq. (REJECT)	f_{HR}		540		Hz	@ -25 dBm
4	Call progress tone detect level (total power)		-30			dBm	

† Characteristics are over recommended operating conditions unless otherwise stated
‡ Typical figures are at 25°C, V_{DD}=5V, and for design aid only: not guaranteed and not subject to production testing

AC Electrical Characteristics†- DTMF Reception - Typical DTMF tone accept and reject requirements. Actual values are user selectable as per Figures 5, 6 and 7.

	Characteristics	Sym	Min	Typ‡	Max	Units	Conditions
1	Minimum tone accept duration	t_{REC}		40		ms	
2	Maximum tone reject duration	$t_{\overline{REC}}$		20		ms	
3	Minimum interdigit pause duration	t_{ID}		40		ms	
4	Maximum tone drop-out duration	t_{OD}		20		ms	

† Characteristics are over recommended operating conditions unless otherwise stated
‡ Typical figures are at 25°C, V_{DD}=5V, and for design aid only: not guaranteed and not subject to production testing

AC Electrical Characteristics† - Voltages are with respect to ground (V_{SS}), unless otherwise stated.

		Characteristics	Sym	Min	Typ‡	Max	Units	Conditions
1	TONE IN	Tone present detect time	t_{DP}	3	11	14	ms	Note 11
2		Tone absent detect time	t_{DA}	0.5	4	8.5	ms	Note 11
3		Delay St to b3	t_{PStb3}		13		µs	See Figure 7
4		Delay St to RX_0-RX_3	t_{PStRX}		8		µs	See Figure 7
5	TONE OUT	Tone burst duration	t_{BST}	50		52	ms	DTMF mode
6		Tone pause duration	t_{PS}	50		52	ms	DTMF mode
7		Tone burst duration (extended)	t_{BSTE}	100		104	ms	Call Progress mode
8		Tone pause duration (extended)	t_{PSE}	100		104	ms	Call Progress mode
9		High group output level	V_{HOUT}	-6.1		-2.1	dBm	R_L=10kΩ
10		Low group output level	V_{LOUT}	-8.1		-4.1	dBm	R_L=10kΩ
11		Pre-emphasis	dB_P	0	2	3	dB	R_L=10kΩ
12		Output distortion (Single Tone)	THD		-35		dB	25 kHz Bandwidth
13								R_L=10kΩ
14		Frequency deviation	f_D		±0.7	±1.5	%	f_C=3.579545 MHz
15		Output load resistance	R_{LT}	10		50	kΩ	
16	XTAL	Crystal/clock frequency	f_C	3.5759	3.5795	3.5831	MHz	
17		Clock input rise and fall time	t_{CLRF}			110	ns	Ext. clock
18		Clock input duty cycle	DC_{CL}	40	50	60	%	Ext. clock
19		Capacitive load (OSC2)	C_{LO}			30	pF	

† Timing is over recommended temperature & power supply voltages.
‡ Typical figures are at 25°C and for design aid only: not guaranteed and not subject to production testing.

AC Electrical Characteristics† - MPU Interface - Voltages are with respect to ground (V_{SS}), unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Conditions
1	$\overline{RD}/\overline{WR}$ clock frequency	f_{CYC}		4.0		MHz	Figure 16
2	$\overline{RD}/\overline{WR}$ cycle period	t_{CYC}		250		ns	Figure 16
3	$\overline{RD}/\overline{WR}$ rise and fall time	t_R, t_F			20	ns	Figure 16
4	Address setup time	t_{AS}	23			ns	Figures 17 & 18
5	Address hold time	t_{AH}	26			ns	Figures 17 & 18
6	Data hold time (read)	t_{DHR}	22			ns	Figures 17 & 18
7	$\overline{RD}$ to valid data delay (read)	t_{DDR}			100	ns	Figures 17 & 18
8	$\overline{RD}$, $\overline{WR}$ pulse width low	t_{PWL}	150			ns	Figures 16, 17 & 18
9	$\overline{RD}$, $\overline{WR}$ pulse width high	t_{PWH}		100		ns	Figures 16, 17 & 18
10	Data setup time (write)	t_{DSW}	45			ns	Figures 17 & 18
11	Data hold time (write)	t_{DHW}	10			ns	Figures 17 & 18
12	Input Capacitance (data bus)	C_{IN}		5		pF	
13	Output Capacitance ($\overline{IRQ}$/CP)	C_{OUT}		5		pF	

† Characteristics are over recommended operating conditions unless otherwise stated
‡ Typical figures are at 25°C, V_{DD}=5V, and for design aid only: not guaranteed and not subject to production testing

NOTES: 1) dBm=decibels above or below a reference power of 1 mW into a 600 ohm load.
2) Digit sequence consists of all 16 DTMF tones.
3) Tone duration=40 ms. Tone pause=40 ms.
4) Nominal DTMF frequencies are used.
5) Both tones in the composite signal have an equal amplitude.
6) The tone pair is deviated by ± 1.5%±2 Hz.
7) Bandwidth limited (3 kHz) Gaussian noise.
8) The precise dial tone frequencies are 350 and 440 Hz (±2%).
9) Guaranteed by design and characterization. Not subject to production testing.
10) Referenced to the lowest amplitude tone in the DTMF signal.
11) For guard time calculation purposes.

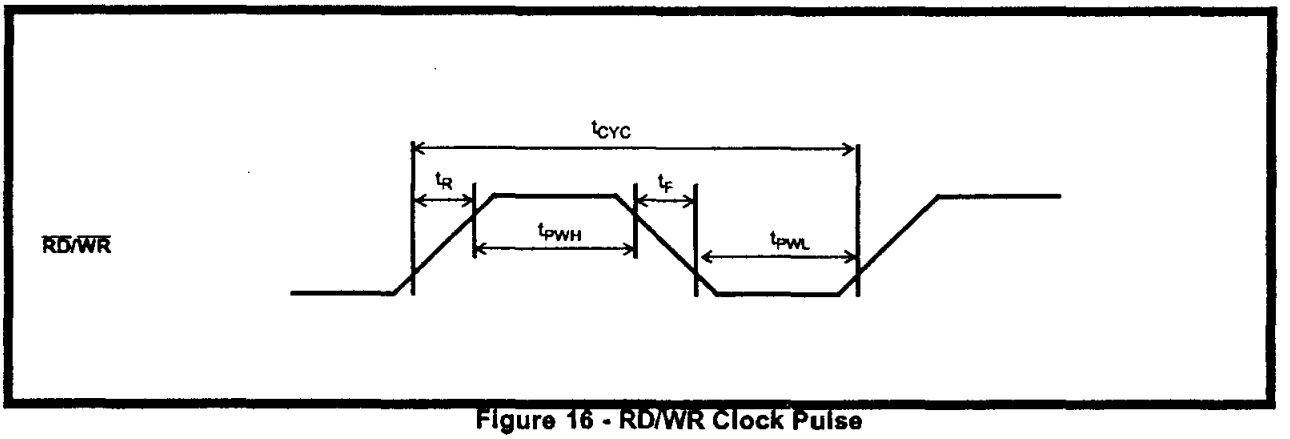


Figure 16 - RD/WR Clock Pulse

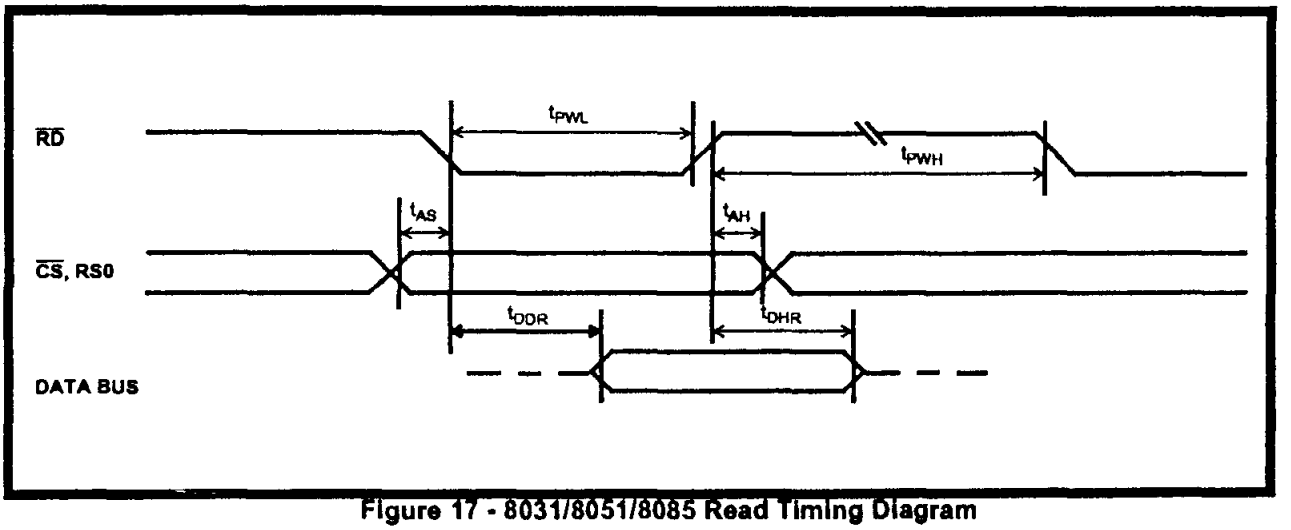


Figure 17 - 8031/8051/8085 Read Timing Diagram

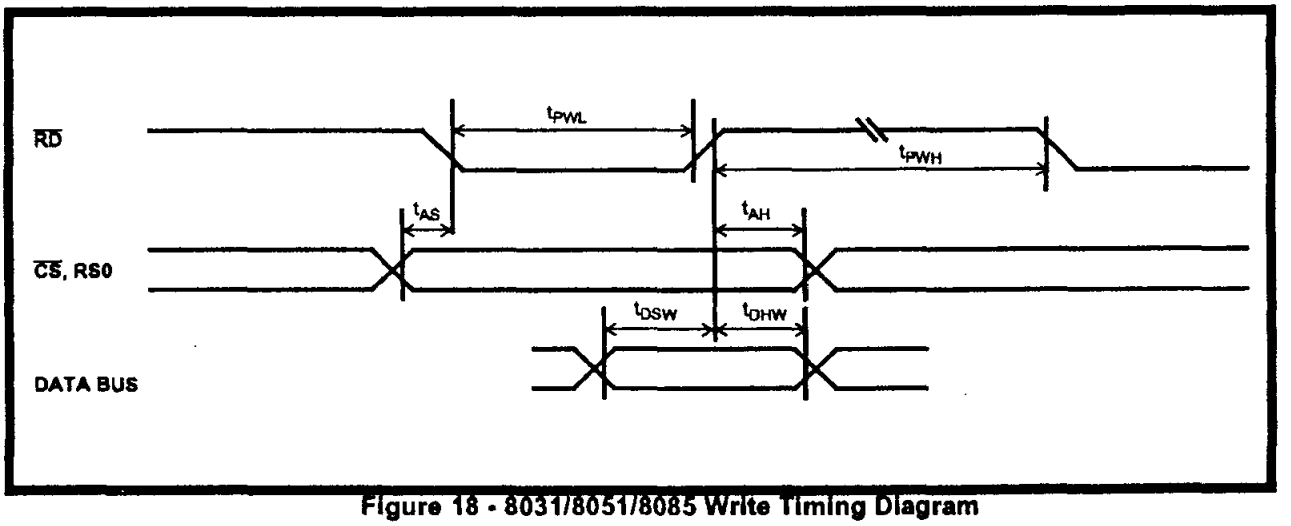


Figure 18 - 8031/8051/8085 Write Timing Diagram

BIODATA

Nama	:	Rudianto Tjahyono
NRP	:	5103000030
Tempat, Tgl. Lahir	:	Surabaya, 30-10-1981
Agama	:	Katolik
Alamat rumah	:	Jl. Ploso I / 24 A
		Surabaya

Riwayat Pendidikan :

- Tahun 1994 Lulus SDK St XAVERIUS I, Surabaya.
- Tahun 1997 Lulus SLTPK AC I, Surabaya.
- Tahun 2000 Lulus SMUK FRATERAN, Surabaya.