LAMPIRAN

Prosedure Penggunaan Alat

1. Pastikan *equipment* yang akan digunakan dalam posisi 'On'
2. Switch Power On
3. Tekan tombol mode VCR pada *Universal Remote Control* BC-9950
4. Tekan tombol Power On (keluar tampilan LCD)
5. Tekan tombol 4/5/6 (untuk menghidupkan *equipment*)
   - Tombol 4 : untuk menghidupkan *equipment Audio* 1 (A1→ lampu nyala)
   - Tombol 5 : untuk menghidupkan *equipment Audio* 2 (A2→ lampu nyala)
   - Tombol 6 : untuk menghidupkan *equipment Audio Video* (AV→ lampu nyala)

   Jika salah satu tombol 4/5/6 ditekan (1dari 3 lampu led menyala) maka :

   - Tombol 4 → Memilih *equipment* A1 (SELECT 1 → tampilan LCD)
   - Tombol 5 → Memilih *equipment* A2 (SELECT 2 → tampilan LCD)
   - Tombol 6 → Memilih *equipment* AV (SELECT 3 → tampilan LCD)
6. Tekan tombol 1/2/3 (memilih *equipment* yang akan digunakan)
   - Tombol 1 → Memilih *equipment* A1 (SELECT 1 → tampilan LCD)
   - Tombol 2 → Memilih *equipment* A2 (SELECT 2 → tampilan LCD)
   - Tombol 3 → Memilih *equipment* AV (SELECT 3 → tampilan LCD)

   SELECT 1 : *Equipment A1* terhubung pada output (amplifier)

   SELECT 2 : *Equipment A2* terhubung pada output (amplifier)

   SELECT 3 : *Equipment AV* terhubung pada output (*Television*)

Pemilihan *equipment* dapat dilakukan jika 2-3 lampu Led menyala

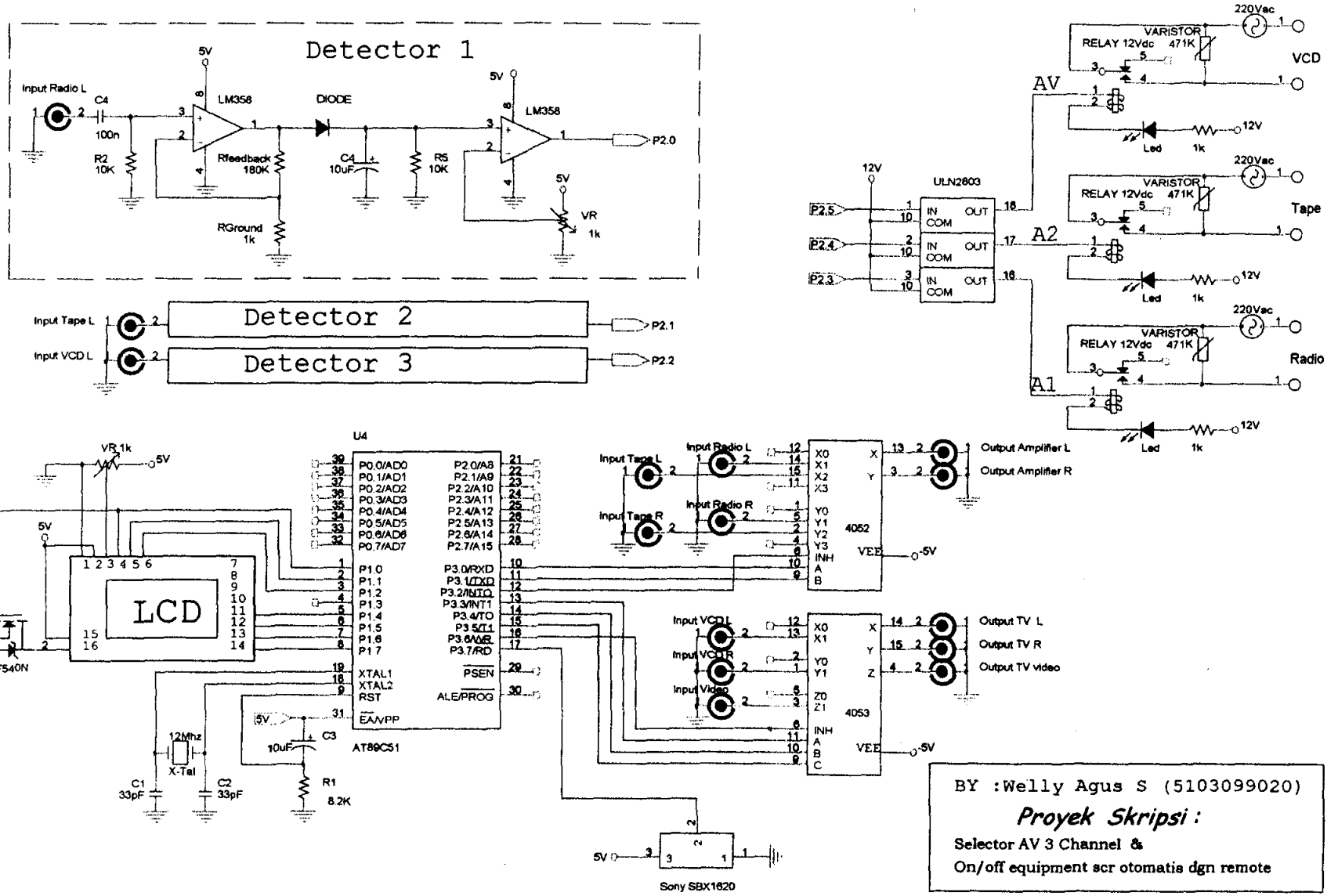
Contoh : Lampu A1 menyala, lampu A2 menyala, lampu AV mati, maka pemilihan *equipment* dapat dilakukan pada tombol 1 dan 2

7. Jika *equipment* tidak digunakan lagi dapat dimatikan secara langsung pada tombol 4/5/6, tergantung pada *equipment* mana yang akan dimatikan
   - Tombol 4 : untuk mematikan *equipment Audio* 1 (A1→ lampu mati)
   - Tombol 5 : untuk mematikan *equipment Audio* 2 (A2→ lampu mati)
   - Tombol 6 : untuk mematikan *equipment Audio Video* (AV→ lampu mati)
8. Jika semua equipment tidak digunakan lagi dapat secara langsung dimatikan dengan menekan tombol Power.

Jika pada tampilan LCD tercetak "ON" berarti *equipment* tersebut siap untuk digunakan.

Jika pada tampilan LCD tercetak "OFF" berarti *equipment* yang akan digunakan tersebut dalam keadaan mati (tidak ada sumber tegangan Vac).

SELAMAT MENCOBA


Detector 1
Input Radio L
C4
100n
R2
10K
LM358
Rfeedback
180K
RGround
1k
DIODE
C4
10uF
R5
10K
LM358
P2.0
VR
1k
5V
Detector 2
Input Tape L
P2.1
Detector 3
Input VCD L
P2.2
ULN2803
P2.5
P2.4
P2.3
IN
OUT
COM
AV
A2
A1
220Vac
VARISTOR
RELAY 12Vdc 471K
VCD
Tape
Radio
Led
1k
12V
U4
AT89C51
LCD
IRF540N
VR 1k
12Mhz
X-Tal
C1
33pF
C2
33pF
C3
10uF
R1
8.2K
P0.0/AD0
P0.1/AD1
P0.2/AD2
P0.3/AD3
P0.4/AD4
P0.5/AD5
P0.6/AD6
P0.7/AD7
P2.0/A8
P2.1/A9
P2.2/A10
P2.3/A11
P2.4/A12
P2.5/A13
P2.6/A14
P2.7/A15
P1.0
P1.1
P1.2
P1.3
P1.4
P1.5
P1.6
P1.7
P3.0/RXD
P3.1/TXD
P3.2/INT0
P3.3/INT1
P3.4/T0
P3.5/T1
P3.6/WR
P3.7/RD
PSEN
ALE/PROG
XTAL1
XTAL2
RST
EA/VPP
Input Tape L
Input Tape R
Input Radio L
Input Radio R
4052
VEE
Output Amplifier L
Output Amplifier R
Input VCD L
Input VCD R
Input Video
4053
Output TV L
Output TV R
Output TV video
Sony SBX1620
BY :Welly Agus S (5103099020)
Proyek Skripsi :
Selector AV 3 Channel &
On/off equipment scr otomatis dgn remote

HASIL PENGUJIAN ALAT

Tombol Remote	Relay			*Analog Multiplexer*							*Display* LCD	Equipment yang dipilih		
	1	2	3	CMOS 4052			CMOS 4053					A1	A2	AV
				INH	B	A	INH	C	B	A				
Power On	OFF	OFF	OFF	4.35	4.35	4.35	4.35	4.35	4.35	4.35	SELECT - A1 OFF A2 OFF AV OFF	-	-	-
Equipment A1 dinyalakan											SELECT - A1 ON A2 OFF AV OFF	-	-	-
Equipment A2 dinyalakan											SELECT - A1 OFF A2 ON AV OFF	-	-	-
Equipment AV dinyalakan											SELECT - A1 OFF A2 OFF AV ON	-	-	-
Tombol 4	ON	OFF	OFF	0	0	4.35	4.35	0	0	0	SELECT 1 A1 ON A2 OFF AV OFF	RADIO	-	-
Tombol 5	OFF	ON	OFF	0	4.35	0	4.35	0	0	0	SELECT 2 A1 OFF A2 ON AV OFF	-	TAPE	-
Tombol 6	OFF	OFF	ON	4.35	0	0	0	4.35	4.35	4.35	SELECT 3 A1 OFF A2 OFF AV ON	-	-	VCD
Tombol 1	ON	ON	ON	0	0	4.35	4.35	0	0	0	SELECT 1 A1 ON A2 ON AV ON	RADIO	-	-
Tombol 2	ON	ON	ON	0	4.35	0	4.35	0	0	0	SELECT 2 A1 ON A2 ON AV ON	-	TAPE	-
Tombol 3	ON	ON	ON	4.35	0	0	0	4.35	4.35	4.35	SELECT 3 A1 ON A2 ON AV ON	-	-	VCD

```
        $MOD51

        CSEG
        ORG   00H
        JMP   START

        ORG   0BH
        CLR   TR0               ;Matikan Timer 0
        SETB  21H.0
        RETI

KATA:     DB    'SELECT - AV OFF',0,'A1 OFF   A2 OFF',0

;-------------
;Delay 4 mS
;-------------
D4mS:   MOV   R7,#20
D4mS01: MOV   R6,#100
        DJNZ  R6,$
        DJNZ  R7,D4mS01
        RET

;-------------
;    Delay 100 mS
;-------------
D100mS:     MOV   R7,#5
D100mS01:   MOV   R6,#100
D100mS02:   MOV   R5,#100
        DJNZ  R5,$
        DJNZ  R6,D100mS02
        DJNZ  R7,D100mS01
        RET

;---------------------
;           Enable Pulse Instruction
;---------------------
EPI:    ANL   A,#0F0H           ;4 Bit
        ORL   A,#00CH           ;Enable High, Instruction Input
        MOV   P1,A
        ANL   A,#0F8H           ;Enable Low, Instruction Input
        MOV   P1,A
        ACALL D4mS              ;Delay 4 mS
        RET

;---------------------
;LCD Control Instruction
;---------------------
LCI:    MOV   R5,A              ;Ambil 4 Bit (D7..D4)
        ACALL EPI               ;Enable Pulse Instruction
        MOV   A,R5
        SWAP  A                 ;Ambil 4 Bit (D3..D0)
        ACALL EPI               ;Enable Pulse Instruction
        RET

;---------------------
;           Inisialisasi LCD 4 Bit
;---------------------
IL4B:   MOV   R5,#3             ;Diulang 3 Kali
```

```
IL4B01:  MOV   A,#30H          ;Reset Sequence
         ACALL EPI             ;Enable Pulse Instruction
         DJNZ  R5,IL4B01
         MOV   A,#20H          ;Reset Sequence
         ACALL EPI             ;Enable Pulse Instruction
         MOV   A,#28H          ;Function Set
         ACALL LCI             ;(4 Bit, 2 Lines, 5 x 7 Dot Matrik)
         MOV   A,#06H          ;Entry Mode Set
         ACALL LCI             ;(Increment, No Display Shift)
         MOV   A,#0CH          ;Display On/Off Control
         ACALL LCI             ;(Display On, Cursor Off, Blink Off)
DC:      MOV   A,#01H          ;Display Clear
         ACALL LCI             ;LCD Control Instruction
         RET

;-----------------
;Enable Pulse Data
;-----------------
EPD:     ANL   A,#0F0H         ;4 Bit
         ORL   A,#00DH         ;Enable High, Data Input
         MOV   P1,A
         ANL   A,#0F9H         ;Enable Low, Data Input
         MOV   P1,A
         MOV   R7,#40          ;Delay 40 uS
         DJNZ  R7,$
         RET

;-----------------
;LCD Control Data
;-----------------
LCD:     MOV   R5,A            ;Ambil 4 Bit (D7..D4)
         ACALL EPD             ;Enable Pulse Data
         MOV   A,R5            ;Ambil 4 Bit (D3..D0)
         SWAP  A
         ACALL EPD             ;Enable Pulse Data
         RET

;---------------
;Tampilan Awal
;---------------
KDKL:    MOV   A,#0            ;Kirim Data ke LCD
         MOVC  A,@A+DPTR
         INC   DPTR
         JZ EscKDKL            ;Huruf sudah habis ?
         ACALL
         LCD                   ;LCD Control Data
         JMP   KDKL

EscKDKL: RET

TA:      MOV   A,#080H         ;Cursor Home Line 1 Colom 0
         ACALL LCI             ;LCD Control Instruction
         MOV   DPTR,#KATA
         ACALL KDKL            ;Kirim Data ke LCD
         MOV   A,#0C0H         ;Cursor Home Line 2 Colom 0
         ACALL LCI             ;LCD Control Instruction
         ACALL KDKL            ;Kirim Data ke LCD
         RET
```

```
;-------------
;Cek Remote
;-------------
CR:     MOV   3DH,A
        MOV   R0,#30H
CR01:   MOV   TH0,#0
        MOV   TL0,#0
        SETB  TR0           ;Aktifkan Timer 0
CR02a:  JB    P3.7,CR02b    ;Hitung periode (LO)
        JNB   21H.0,CR02a   ;Timer 0 overflow?
        JMP   CR07
CR02b:  JNB   P3.7,CR03     ;Hitung periode (HI)
        JNB   21H.0,CR02b   ;Timer 0 overflow?
        JMP   CR07
CR03:   CLR   TR1           ;Matikan Timer 0
        MOV   @R0,TH0
        INC   R0
        CJNE  R0,#3DH,CR01
        MOV   R0,#31H
CR04:   MOV   A,20H
        RR    A
        MOV   20H,A
        CJNE  @R0,#4,CR05   ;Logic 0?
        CLR   20H.7
        JMP   CR06
CR05:   CJNE  @R0,#7,CR07   ;Logic 1?
        SETB  20H.7
CR06:   INC   R0
        CJNE  R0,#39H,CR04
        MOV   A,3DH
        RET

CR07:   CLR   21H.0         ;Kode Remote tidak sesuai
        MOV   20H,#0
        MOV   A,3DH
        RET

;-----------------
; Cek Kondisi Relay
;-----------------
CKR:    ACALL  D100mS       ;Delay 100 mS
        MOV    A,P2         ;Cek kondisi relay
        ANL    A,#38H       ;AND dengan 00111000
        CJNE   A,#00H,CKR1  Semua relay off?
        MOV    A,#087H      ;Cursor Home Line 1 Colom 7
        ACALL  LCI          ;LCD Control Instruction
        MOV    R4,#2DH      ;ASCII -
        MOV    A,#2DH       ;ASCII -
        ACALL  LCD          ;LCD Control Data
        MOV    P3,#0C4H
        RET

CKR1:   CJNE   A,#08H,CKR2  ;Hanya relay 1 yang on?
        ACALL  SA1          ;Select Audio 1
        RET
CKR2:   CJNE   A,#10H,CKR3  ;Hanya relay 2 yang on?
        ACALL  SA2          ;Select Audio 2
```

```
        RET
CKR3:   CJNE  A,#20H,EscCKR   ;Hanya relay 3 yang on?
        ACALL SAV             ;Select Audio Video
EscCKR: RET

;-------------------------
; Cek Tombol Remote yang Ditekan
;-------------------------
CTRYD:  MOV   A,20H
        MOV   20H,#0
        CJNE  A,#80H,T2       ;Tombol 1 ditekan?
        JNB   P2.3,EscT1      ;Relay 1 Off?
SA1:    MOV   A,#087H         ;Cursor Home Line 1 Colom 7
        ACALL LCI             ;LCD Control Instruction
        MOV   R4,#31H         ;ASCII 1
        MOV   A,#31H          ;ASCII 1
        ACALL LCD             ;LCD Control Data
        MOV   P3,#0C1H
EscT1:  RET

T2:     CJNE  A,#81H,T3       Tombol 2 ditekan?
        JNB   P2.4,EscT2      Relay 2 Off?
SA2:    MOV   A,#087H         Cursor Home Line 1 Colom 7
        ACALL LCI             LCD Control Instruction
        MOV   R4,#32H         ASCII 2
        MOV   A,#32H          ASCII 2
        ACALL LCD             LCD Control Data
        MOV   P3,#0C2H
EscT2:  RET

T3:     CJNE  A,#82H,T4       Tombol 3 ditekan?
        JNB   P2.5,EscT3      Relay 3 Off?
SAV:    MOV   A,#087H         Cursor Home Line 1 Colom 7
        ACALL LCI             LCD Control Instruction
        MOV   R4,#33H         ASCII 3
        MOV   A,#33H          ASCII 3
        ACALL LCD             LCD Control Data
        MOV   P3,#0BCH
EscT3:  RET

T4:     CJNE  A,#83H,T5       Tombol 4 ditekan?
        CPL   P2.3            On/Off Relay 1
        ACALL CKR             Cek Kondisi Relay
        RET
T5:     CJNE  A,#84H,T6       Tombol 5 ditekan?
        CPL   P2.4            On/Off Relay 2
        ACALL CKR             Cek Kondisi Relay
        RET
T6:     CJNE  A,#85H,TPower   Tombol 6 ditekan?
        CPL   P2.5            On/Off Relay 3
        ACALL CKR             Cek Kondisi Relay
        RET

TPower: CJNE  A,#95H,EscCTRYD ;Tombol POWER ditekan?
        MOV   A,P2
        ORL   A,#0C7H
        MOV   R2,A
        MOV   A,P3
```

```
            ORL   A,#080H
            MOV   R3,A
            ACALL DC
            MOV   P2,#0C7H          Relay Off
            MOV   P3,#0C4H          Analog Multiplekser Off
TPower01:   JB    P3.7,$            Remote ditekan?
            ACALL CR                Cek Remote
            MOV   A,20H
            CJNE  A,#95H,TPower01   Tombol POWER ditekan?
            MOV   20H,#0
            ACALL D100mS            Delay 100 mS
            MOV   P2,R2
            MOV   P3,R3
            ACALL TA                Tampilan Awal
            ACALL CS                Cek Sinyal
            MOV   A,#087H           Cursor Home Line 1 Colom 7
            ACALL LCI               LCD Control Instruction
            MOV   A,R4
            ACALL LCD               LCD Control Data

EscCTRYD:   RET

;-----------------------
; Enable Pulse Instruction
;-----------------------
EPI02:      ANL   A,#0F0H           ;4 Bit
            ORL   A,#00CH           Enable High, Instruction Input
            MOV   P1,A
            ANL   A,#0F8H           Enable Low, Instruction Input
            MOV   P1,A
            MOV   R7,#40            Delay 40 uS
            DJNZ  R7,$
            RET

;-----------------------
; LCD Control Instruction
;-----------------------
LCI02:      MOV   R5,A              Ambil 4 Bit (D7..D4)
            ACALL EPI02             Enable Pulse Instruction
            MOV   A,R5
            SWAP  A                 Ambil 4 Bit (D3..D0)
            ACALL EPI02             Enable Pulse Instruction
            RET

;-----------
; Cek Sinyal
;-----------
SOff:       MOV   A,#46H            ASCII F (Sinyal off)
            ACALL LCD               LCD Control Data
            MOV   A,#46H            ASCII F (Sinyal off)
            ACALL LCD               LCD Control Data
            RET
SOn:        MOV   A,#4EH            ASCII N (Sinyal on)
            ACALL LCD               LCD Control Data
            MOV   A,#20H            ASCII spasi (Sinyal off)
            ACALL LCD               LCD Control Data
            RET
```

```
CS:     MOV   A,#0C4H       ;Cursor Home Line 2 Colom 4
        ACALL LCI02         ;LCD Control Instruction
        JB    P2.0,CSA1on
        ACALL SOff          ;(Sinyal off)
        JMP   CSA2
CSA1on: ACALL SOn           ;(Sinyal on)
CSA2:   MOV   A,#0CEH       ;Cursor Home Line 2 Colom 14
        ACALL LCI02         ;LCD Control Instruction
        JB    P2.1,CSA2on
        ACALL SOff          ;(Sinyal off)
        JMP   CSAV
CSA2on: ACALL SOn           ;(Sinyal on)
CSAV:   MOV   A,#08EH       ;Cursor Home Line 1 Colom 14
        ACALL LCI02         ;LCD Control Instruction
        JB    P2.2,CSAVon
        ACALL SOff          ;(Sinval off)
        RET
CSAVon: ACALL SOn           ;(Sinyal on)
        RET

;-------------
; Main Program
;-------------
START:  MOV   P2,#0C7H      ;Relay Off
        MOV   R4,#2DH       ;ASCII -
        MOV   TMOD,#01H     ;Timer 0 mode 1
        MOV   IE,#82H       ;Inisialisasi Interrupt
        ACALL IL4B          ;Inisialisasi LCD 4 Bit

MP00:   JB    P3.7,$        ;Remote ditekan?
        ACALL CR            ;Cek Remote
        MOV   A,20H
        CJNE  A,#95H,MP00   ;Tombol POWER ditekan?
        MOV   20H,#0
        ACALL D100mS        ;Delay 100 mS
        ACALL TA            ;Tampilan Awal
        ACALL CS            ;Cek Sinyal
        MOV   A,P2
        ANL   A,#07H
        MOV   R1,A

MP01:   MOV   A,20H
        JNZ   MP02          ;Ada data remote yang masuk?
        MOV   A,P2
        ANL   A,#07H
        CJNE  A,1H,MP03     ;Ada perubahan sinyal?
        JB    P3.7,MP01     ;Remote ditekan?
        ACALL CR            ;Cek Remote
        JMP   MP01
MP02:   ACALL CTRYD         ;Cek Tombol Remote yang Ditekan
        MOV   A,P2
        ANL   A,#07H
        MOV   R1,A
        JMP   MP01
MP03:   MOV   R1,A
        ACALL CS            ;Cek Sinyal
        JMP   MP01
        END
```

Features

- Compatible with MCS-51™ Products
- 4K Bytes of In-System Reprogrammable Flash Memory
  - Endurance: 1,000 Write/Erase Cycles
- Fully Static Operation: 0 Hz to 24 MHz
- Three-Level Program Memory Lock
- 128 x 8-Bit Internal RAM
- 32 Programmable I/O Lines
- Two 16-Bit Timer/Counters
- Six Interrupt Sources
- Programmable Serial Channel
- Low Power Idle and Power Down Modes

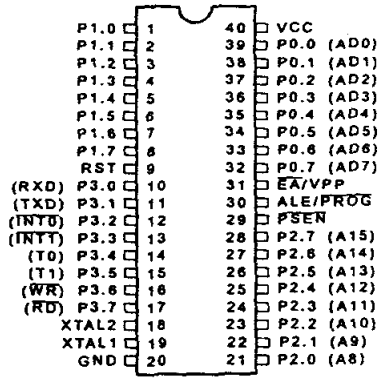
Description

The AT89C51 is a low-power, high-performance CMOS 8-bit microcomputer with 4K bytes of Flash Programmable and Erasable Read Only Memory (PEROM). The device is manufactured using Atmel's high density nonvolatile memory technology and is compatible with the industry standard MCS-51™ instruction set and pinout. The on-chip Flash allows the program memory to be reprogrammed in-system or by a conventional nonvolatile memory programmer. By combining a versatile 8-bit CPU with Flash on a monolithic chip, the Atmel AT89C51 is a powerful microcomputer which provides a highly flexible and cost effective solution to many embedded control applications.

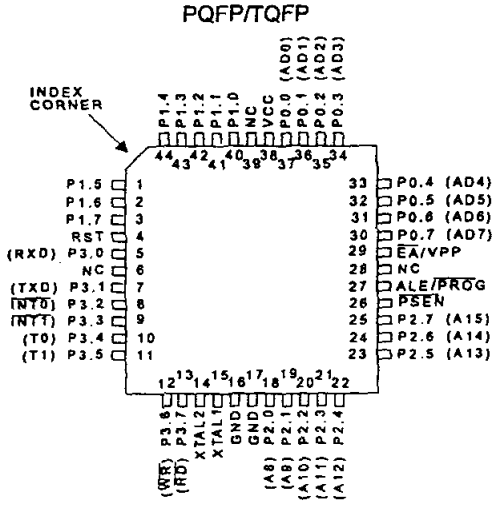
(continued)

Pin Configurations

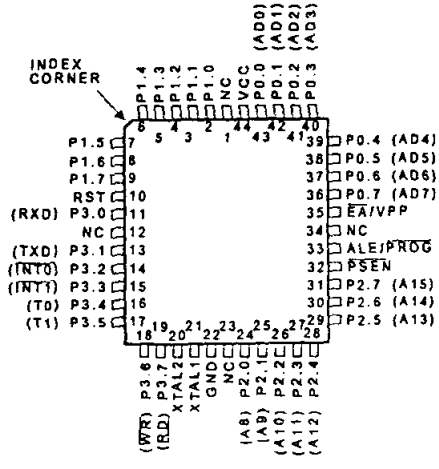
PDIP



PQFP/TQFP



PLCC

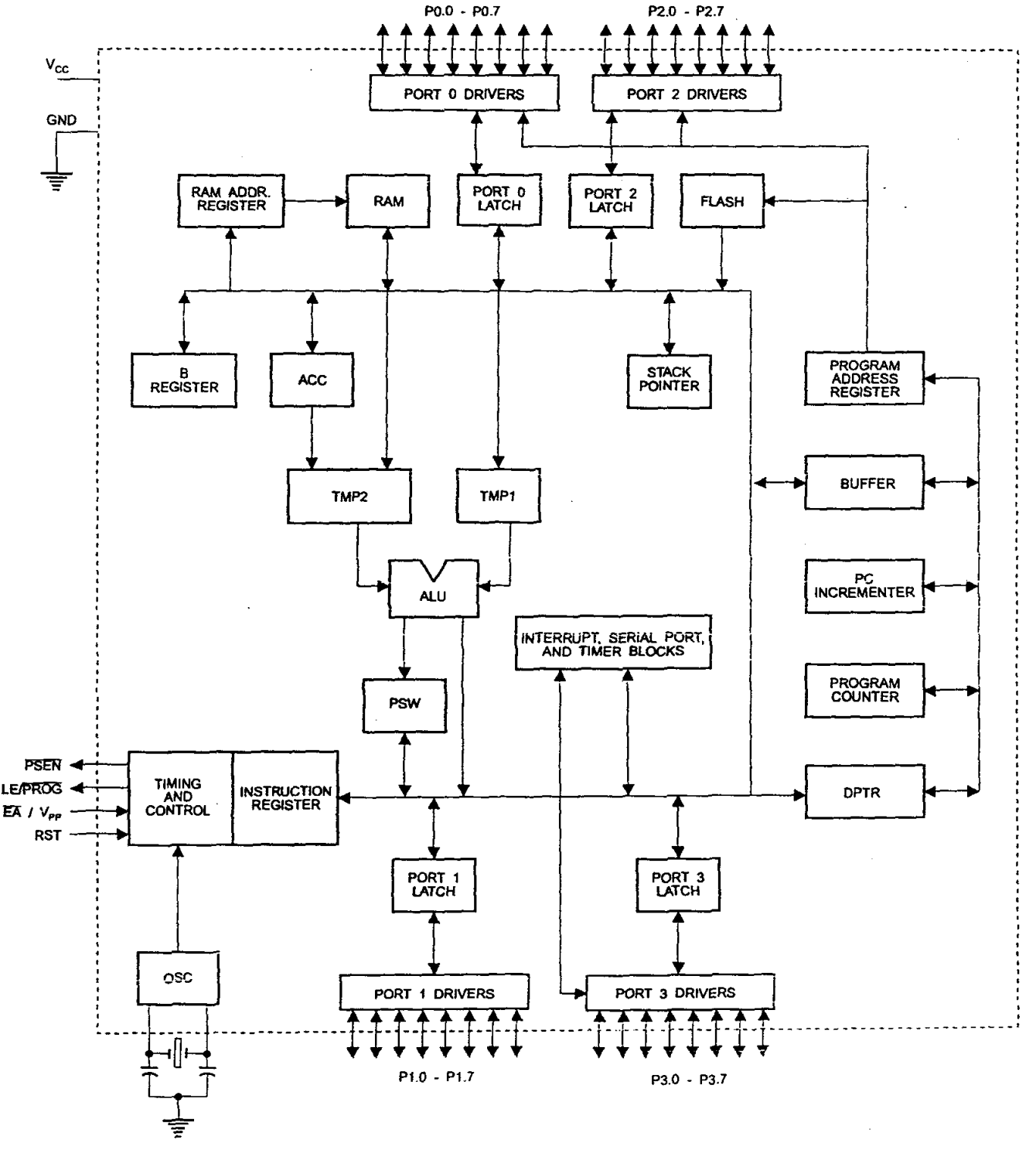


8-Bit Microcontroller with 4K Bytes Flash

AT89C51

0265F-A–12/97

ock Diagram


P0.0 - P0.7
P2.0 - P2.7
V_{CC}
GND
PORT 0 DRIVERS
PORT 2 DRIVERS
RAM ADDR. REGISTER
RAM
PORT 0 LATCH
PORT 2 LATCH
FLASH
B REGISTER
ACC
STACK POINTER
PROGRAM ADDRESS REGISTER
BUFFER
TMP2
TMP1
ALU
PC INCREMENTER
INTERRUPT, SERIAL PORT, AND TIMER BLOCKS
PROGRAM COUNTER
PSW
PSEN
ALE/PROG
EA / V_{PP}
RST
TIMING AND CONTROL
INSTRUCTION REGISTER
DPTR
PORT 1 LATCH
PORT 3 LATCH
OSC
PORT 1 DRIVERS
PORT 3 DRIVERS
P1.0 - P1.7
P3.0 - P3.7

The AT89C51 provides the following standard features: 4K bytes of Flash, 128 bytes of RAM, 32 I/O lines, two 16-bit timer/counters, a five vector two-level interrupt architecture, a full duplex serial port, on-chip oscillator and clock circuitry. In addition, the AT89C51 is designed with static logic for operation down to zero frequency and supports two software selectable power saving modes. The Idle Mode stops the CPU while allowing the RAM, timer/counters, serial port and interrupt system to continue functioning. The Power Down Mode saves the RAM contents but freezes the oscillator disabling all other chip functions until the next hardware reset.

Pin Description

V_{CC}
Supply voltage.

GND
Ground.

Port 0
Port 0 is an 8-bit open drain bidirectional I/O port. As an output port each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high-impedance inputs.

Port 0 may also be configured to be the multiplexed low-order address/data bus during accesses to external program and data memory. In this mode P0 has internal pullups.

Port 0 also receives the code bytes during Flash programming, and outputs the code bytes during program verification. External pullups are required during program verification.

Port 1
Port 1 is an 8-bit bidirectional I/O port with internal pullups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}) because of the internal pullups.

Port 1 also receives the low-order address bytes during Flash programming and verification.

Port 2
Port 2 is an 8-bit bidirectional I/O port with internal pullups. The Port 2 output buffers can sink/source four TTL inputs. When 1s are written to Port 2 pins they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL}) because of the internal pullups.

Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application it uses strong internal pullups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

Port 3
Port 3 is an 8-bit bidirectional I/O port with internal pullups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}) because of the pullups.

Port 3 also serves the functions of various special features of the AT89C51 as listed below:

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

Port 3 also receives some control signals for Flash programming and verification.

RST
Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device.

ALE/$\overline{PROG}$
Address Latch Enable output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input ($\overline{PROG}$) during Flash programming.

In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external Data Memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

$\overline{PSEN}$
Program Store Enable is the read strobe to external program memory.

When the AT89C51 is executing code from external program memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external data memory.

$\overline{EA}$/V_{PP}

External Access Enable. $\overline{EA}$ must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed, $\overline{EA}$ will be internally latched on reset.

$\overline{EA}$ should be strapped to V_{CC} for internal program executions.

This pin also receives the 12-volt programming enable voltage (V_{PP}) during Flash programming, for parts that require 12-volt V_{PP}.

XTAL1

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

XTAL2

Output from the inverting oscillator amplifier.

Oscillator Characteristics

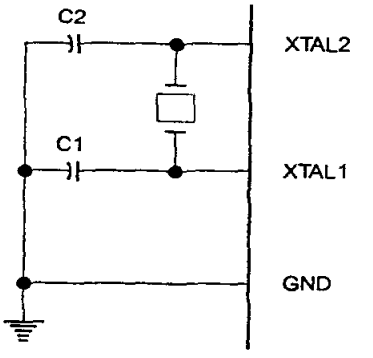
XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier which can be configured for use as an on-chip oscillator, as shown in Figure 1. Either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven as shown in Figure 2. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

Idle Mode

In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special functions registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

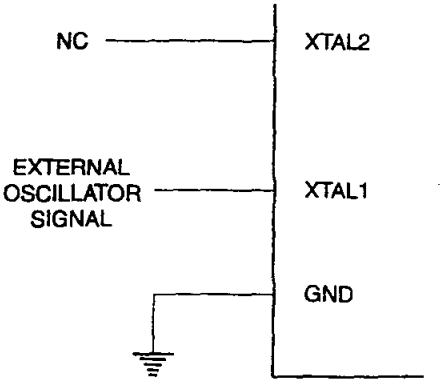
It should be noted that when idle is terminated by a hardware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.

Figure 1. Oscillator Connections



Note: C1, C2 = 30 pF ± 10 pF for Crystals
= 40 pF ± 10 pF for Ceramic Resonators

Figure 2. External Clock Drive Configuration



Status of External Pins During Idle and Power Down Modes

Mode	Program Memory	ALE	$\overline{PSEN}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power Down	Internal	0	0	Data	Data	Data	Data
Power Down	External	0	0	Float	Data	Data	Data

Power Down Mode

n the power down mode the oscillator is stopped, and the nstruction that invokes power down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the power down mode is terminated. The only exit from power down is a hardware reset. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

Program Memory Lock Bits

On the chip are three lock bits which can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in the table below:

When lock bit 1 is programmed, the logic level at the $\overline{EA}$ pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value, and holds that value until reset is activated. It is necessary that the latched value of $\overline{EA}$ be in agreement with the current logic level at that pin in order for the device to function properly.

Lock Bit Protection Modes

Program Lock Bits				Protection Type
	LB1	LB2	LB3	
1	U	U	U	No program lock features.
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, $\overline{EA}$ is sampled and latched on reset, and further programming of the Flash is disabled.
3	P	P	U	Same as mode 2, also verify is disabled.
4	P	P	P	Same as mode 3, also external execution is disabled.

Programming the Flash

The AT89C51 is normally shipped with the on-chip Flash memory array in the erased state (that is, contents = FFH) and ready to be programmed. The programming interface accepts either a high-voltage (12-volt) or a low-voltage (V_{CC}) program enable signal. The low voltage programming mode provides a convenient way to program the AT89C51 inside the user's system, while the high-voltage programming mode is compatible with conventional third party Flash or EPROM programmers.

The AT89C51 is shipped with either the high-voltage or low-voltage programming mode enabled. The respective top-side marking and device signature codes are listed in the following table.

	V_{PP} = 12V	V_{PP} = 5V
Top-Side Mark	AT89C51 xxxx yyww	AT89C51 xxxx-5 yyww
Signature	(030H)=1EH (031H)=51H (032H)=FFH	(030H)=1EH (031H)=51H (032H)=05H

The AT89C51 code memory array is programmed byte-by-byte in either programming mode. *To program any non-blank byte in the on-chip Flash Memory, the entire memory must be erased using the Chip Erase Mode.*

Programming Algorithm: Before programming the AT89C51, the address, data and control signals should be set up according to the Flash programming mode table and Figures 3 and 4. To program the AT89C51, take the following steps.

1. Input the desired memory location on the address lines.
2. Input the appropriate data byte on the data lines.
3. Activate the correct combination of control signals.
4. Raise $\overline{EA}/V_{PP}$ to 12V for the high-voltage programming mode.
5. Pulse ALE/$\overline{PROG}$ once to program a byte in the Flash array or the lock bits. The byte-write cycle is self-timed and typically takes no more than 1.5 ms. Repeat steps 1 through 5, changing the address and data for the entire array or until the end of the object file is reached.

$\overline{Data}$ Polling: The AT89C51 features $\overline{Data}$ Polling to indicate the end of a write cycle. During a write cycle, an attempted read of the last byte written will result in the complement of the written datum on PO.7. Once the write cycle has been completed, true data are valid on all outputs, and the next cycle may begin. $\overline{Data}$ Polling may begin any time after a write cycle has been initiated.

Ready/$\overline{Busy}$: The progress of byte programming can also be monitored by the RDY/$\overline{BSY}$ output signal. P3.4 is pulled low after ALE goes high during programming to indicate BUSY. P3.4 is pulled high again when programming is done to indicate READY.

Program Verify: If lock bits LB1 and LB2 have not been programmed, the programmed code data can be read back via the address and data lines for verification. The lock bits cannot be verified directly. Verification of the lock bits is achieved by observing that their features are enabled.

Chip Erase: The entire Flash array is erased electrically by using the proper combination of control signals and by holding ALE/$\overline{PROG}$ low for 10 ms. The code array is written with all "1"s. The chip erase operation must be executed before the code memory can be re-programmed.

Reading the Signature Bytes: The signature bytes are read by the same procedure as a normal verification of locations 030H,

031H, and 032H, except that P3.6 and P3.7 must be pulled to a logic low. The values returned are as follows.

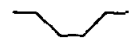
(030H) = 1EH indicates manufactured by Atmel
(031H) = 51H indicates 89C51
(032H) = FFH indicates 12V programming
(032H) = 05H indicates 5V programming

Programming Interface

Every code byte in the Flash array can be written and the entire array can be erased by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

All major programming vendors offer worldwide support for the Atmel microcontroller series. Please contact your local programming vendor for the appropriate software revision.

Flash Programming Modes

Mode		RST	$\overline{PSEN}$	ALE/$\overline{PROG}$	$\overline{EA}$/V_{PP}	P2.6	P2.7	P3.6	P3.7
Write Code Data		H	L		H/12V	L	H	H	H
Read Code Data		H	L	H	H	L	L	H	H
Write Lock	Bit - 1	H	L		H/12V	H	H	H	H
	Bit - 2	H	L		H/12V	H	H	L	L
	Bit - 3	H	L		H/12V	H	L	H	L
Chip Erase		H	L	 (1)	H/12V	H	L	L	L
Read Signature Byte		H	L	H	H	L	L	L	L

Note: 1. Chip Erase requires a 10-ms PROG pulse.

Figure 3. Programming the Flash

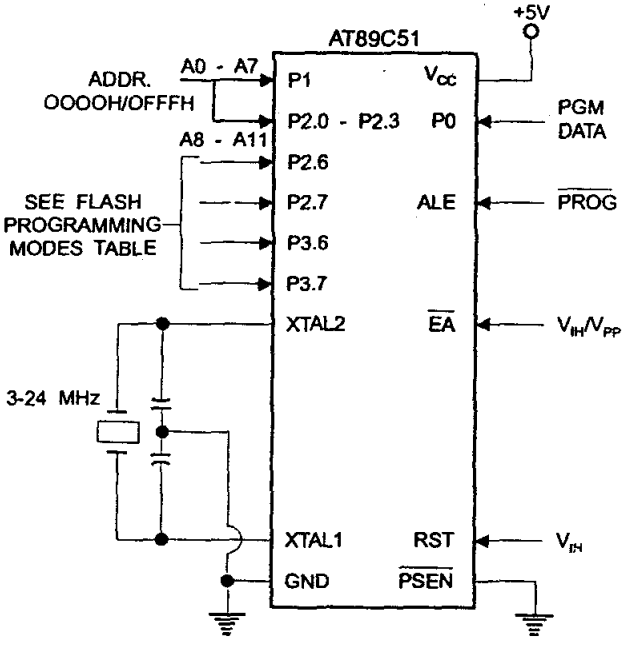
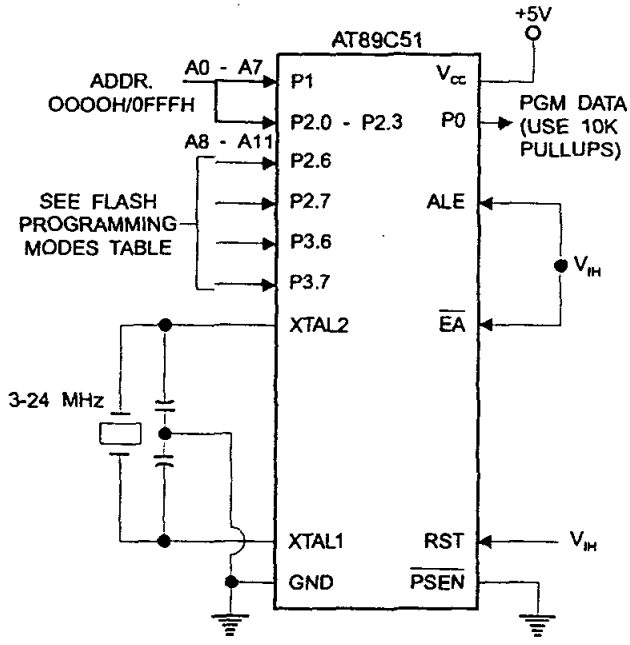


Figure 4. Verifying the Flash



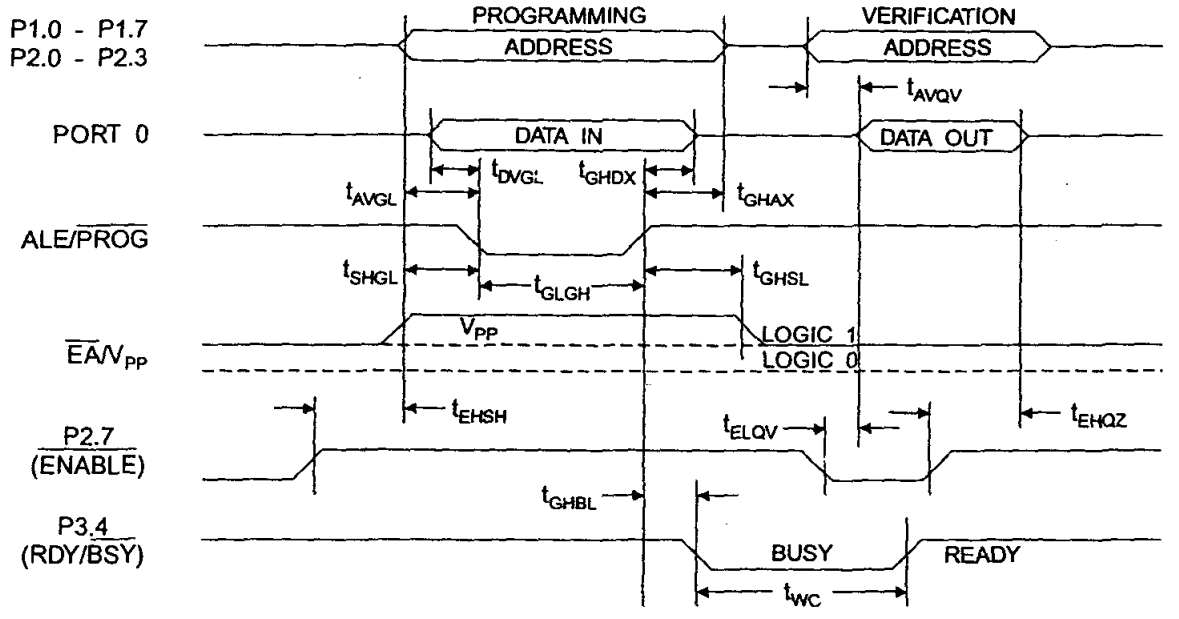
Flash Programming and Verification Characteristics

T_A = 0°C to 70°C, V_{CC} = 5.0 ± 10%

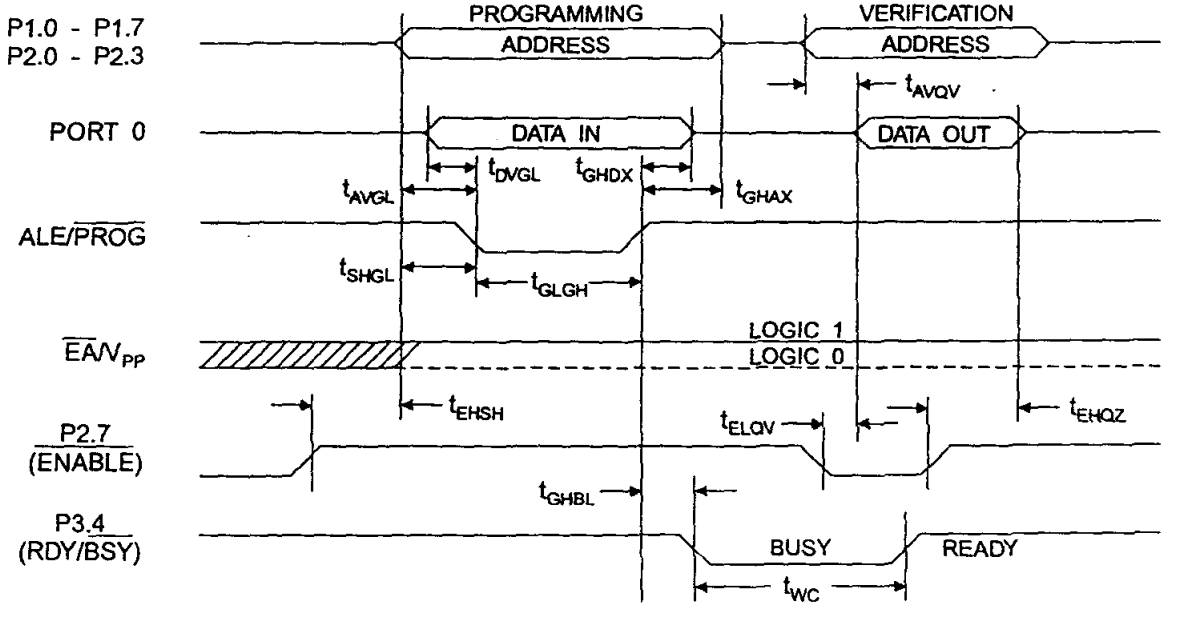
Symbol	Parameter	Min	Max	Units
V_{PP}[1]	Programming Enable Voltage	11.5	12.5	V
I_{PP}[1]	Programming Enable Current		1.0	mA
$1/t_{CLCL}$	Oscillator Frequency	3	24	MHz
t_{AVGL}	Address Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
t_{GHAX}	Address Hold After $\overline{PROG}$	$48t_{CLCL}$		
t_{DVGL}	Data Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
t_{GHDX}	Data Hold After $\overline{PROG}$	$48t_{CLCL}$		
t_{EHSH}	P2.7 ($\overline{ENABLE}$) High to V_{PP}	$48t_{CLCL}$		
t_{SHGL}	V_{PP} Setup to $\overline{PROG}$ Low	10		µs
t_{GHSL}[1]	V_{PP} Hold After $\overline{PROG}$	10		µs
t_{GLGH}	$\overline{PROG}$ Width	1	110	µs
t_{AVQV}	Address to Data Valid		$48t_{CLCL}$	
t_{ELQV}	$\overline{ENABLE}$ Low to Data Valid		$48t_{CLCL}$	
t_{EHQZ}	Data Float After $\overline{ENABLE}$	0	$48t_{CLCL}$	
t_{GHBL}	$\overline{PROG}$ High to $\overline{BUSY}$ Low		1.0	µs
t_{WC}	Byte Write Cycle Time		2.0	ms

Note: 1. Only used in 12-volt programming mode.

Flash Programming and Verification Waveforms - High Voltage Mode (V_{PP} = 12V)



Flash Programming and Verification Waveforms - Low Voltage Mode (V_{PP} = 5V)



Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0V to +7.0V
Maximum Operating Voltage	6.6V
DC Output Current	15.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_A = -40°C to 85°C, V_{CC} = 5.0V ± 20% (unless otherwise noted)

Symbol	Parameter	Condition	Min	Max	Units
V_{IL}	Input Low Voltage	(Except $\overline{EA}$)	-0.5	0.2 V_{CC} - 0.1	V
V_{IL1}	Input Low Voltage ($\overline{EA}$)		-0.5	0.2 V_{CC} - 0.3	V
V_{IH}	Input High Voltage	(Except XTAL1, RST)	0.2 V_{CC} + 0.9	V_{CC} + 0.5	V
V_{IH1}	Input High Voltage	(XTAL1, RST)	0.7 V_{CC}	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage[1] (Ports 1,2,3)	I_{OL} = 1.6 mA		0.45	V
V_{OL1}	Output Low Voltage[1] (Port 0, ALE, $\overline{PSEN}$)	I_{OL} = 3.2 mA		0.45	V
V_{OH}	Output High Voltage (Ports 1,2,3, ALE, $\overline{PSEN}$)	I_{OH} = -60 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -25 µA	0.75 V_{CC}		V
		I_{OH} = -10 µA	0.9 V_{CC}		V
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode)	I_{OH} = -800 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -300 µA	0.75 V_{CC}		V
		I_{OH} = -80 µA	0.9 V_{CC}		V
I_{IL}	Logical 0 Input Current (Ports 1,2,3)	V_{IN} = 0.45V		-50	µA
I_{TL}	Logical 1 to 0 Transition Current (Ports 1,2,3)	V_{IN} = 2V, VCC = 5V ± 10%		-650	µA
I_{LI}	Input Leakage Current (Port 0, $\overline{EA}$)	0.45 < V_{IN} < V_{CC}		±10	µA
R_{RST}	Reset Pulldown Resistor		50	300	KΩ
C_{IO}	Pin Capacitance	Test Freq. = 1 MHz, T_A = 25°C		10	pF
I_{CC}	Power Supply Current	Active Mode, 12 MHz		20	mA
		Idle Mode, 12 MHz		5	mA
	Power Down Mode[2]	V_{CC} = 6V		100	µA
		V_{CC} = 3V		40	µA

Notes: 1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
Maximum I_{OL} per port pin: 10 mA
Maximum I_{OL} per 8-bit port: Port 0: 26 mA
Ports 1, 2, 3: 15 mA
Maximum total I_{OL} for all output pins: 71 mA
If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

2. Minimum V_{CC} for Power Down is 2V.

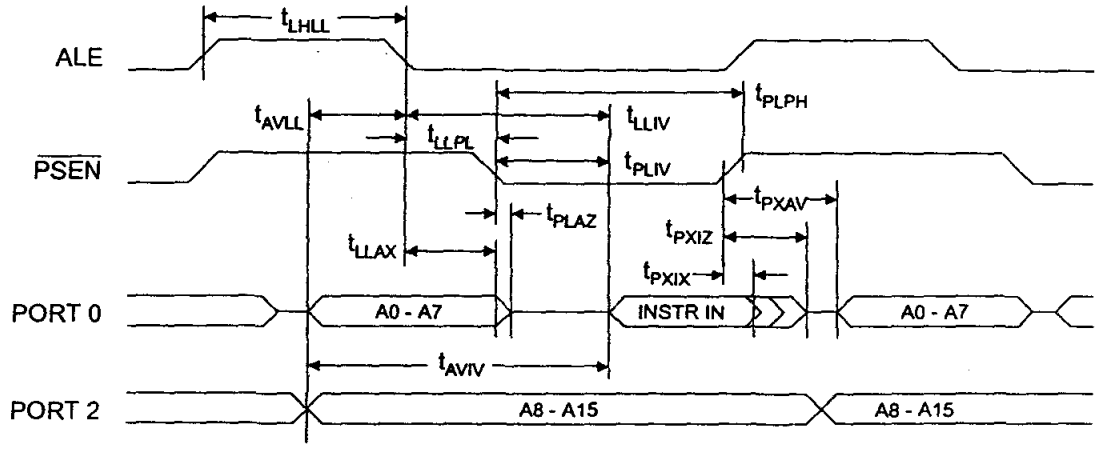
AC Characteristics

Under Operating Conditions; Load Capacitance for Port 0, ALE/$\overline{PROG}$, and $\overline{PSEN}$ = 100 pF; Load Capacitance for all other outputs = 80 pF)

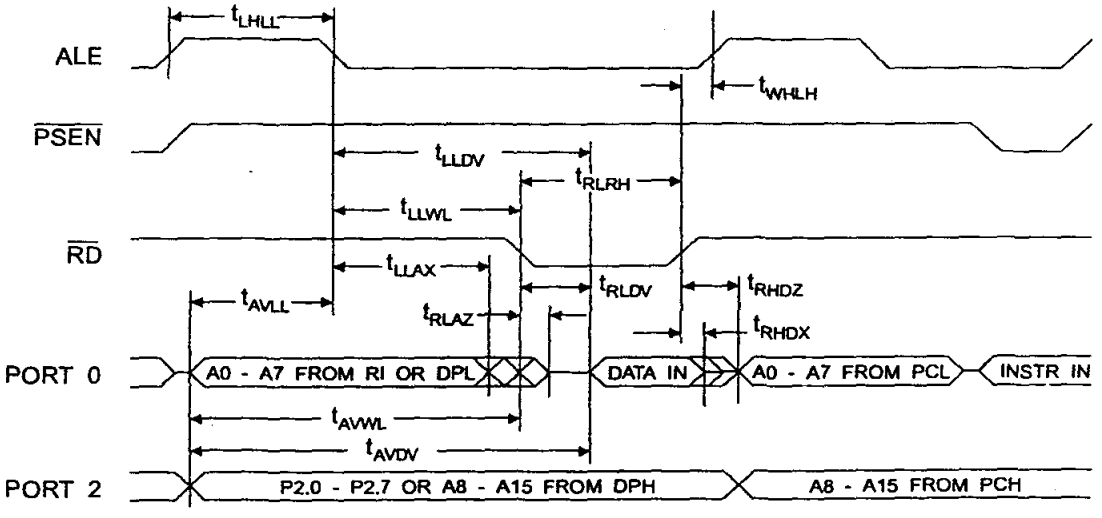
External Program and Data Memory Characteristics

Symbol	Parameter	12 MHz Oscillator		16 to 24 MHz Oscillator		Units
		Min	Max	Min	Max	
$1/t_{CLCL}$	Oscillator Frequency			0	24	MHz
t_{LHLL}	ALE Pulse Width	127		$2t_{CLCL}$-40		ns
t_{AVLL}	Address Valid to ALE Low	43		t_{CLCL}-13		ns
t_{LLAX}	Address Hold After ALE Low	48		t_{CLCL}-20		ns
t_{LLIV}	ALE Low to Valid Instruction In		233		$4t_{CLCL}$-65	ns
t_{LLPL}	ALE Low to $\overline{PSEN}$ Low	43		t_{CLCL}-13		ns
t_{PLPH}	$\overline{PSEN}$ Pulse Width	205		$3t_{CLCL}$-20		ns
t_{PLIV}	$\overline{PSEN}$ Low to Valid Instruction In		145		$3t_{CLCL}$-45	ns
t_{PXIX}	Input Instruction Hold After $\overline{PSEN}$	0		0		ns
t_{PXIZ}	Input Instruction Float After $\overline{PSEN}$		59		t_{CLCL}-10	ns
t_{PXAV}	$\overline{PSEN}$ to Address Valid	75		t_{CLCL}-8		ns
t_{AVIV}	Address to Valid Instruction In		312		$5t_{CLCL}$-55	ns
t_{PLAZ}	$\overline{PSEN}$ Low to Address Float		10		10	ns
t_{RLRH}	$\overline{RD}$ Pulse Width	400		$6t_{CLCL}$-100		ns
t_{WLWH}	$\overline{WR}$ Pulse Width	400		$6t_{CLCL}$-100		ns
t_{RLDV}	$\overline{RD}$ Low to Valid Data In		252		$5t_{CLCL}$-90	ns
t_{RHDX}	Data Hold After $\overline{RD}$	0		0		ns
t_{RHDZ}	Data Float After $\overline{RD}$		97		$2t_{CLCL}$-28	ns
t_{LLDV}	ALE Low to Valid Data In		517		$8t_{CLCL}$-150	ns
t_{AVDV}	Address to Valid Data In		585		$9t_{CLCL}$-165	ns
t_{LLWL}	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	200	300	$3t_{CLCL}$-50	$3t_{CLCL}$+50	ns
t_{AVWL}	Address to $\overline{RD}$ or $\overline{WR}$ Low	203		$4t_{CLCL}$-75		ns
t_{QVWX}	Data Valid to $\overline{WR}$ Transition	23		t_{CLCL}-20		ns
t_{QVWH}	Data Valid to $\overline{WR}$ High	433		$7t_{CLCL}$-120		ns
t_{WHQX}	Data Hold After $\overline{WR}$	33		t_{CLCL}-20		ns
t_{RLAZ}	$\overline{RD}$ Low to Address Float		0		0	ns
t_{WHLH}	$\overline{RD}$ or $\overline{WR}$ High to ALE High	43	123	t_{CLCL}-20	t_{CLCL}+25	ns

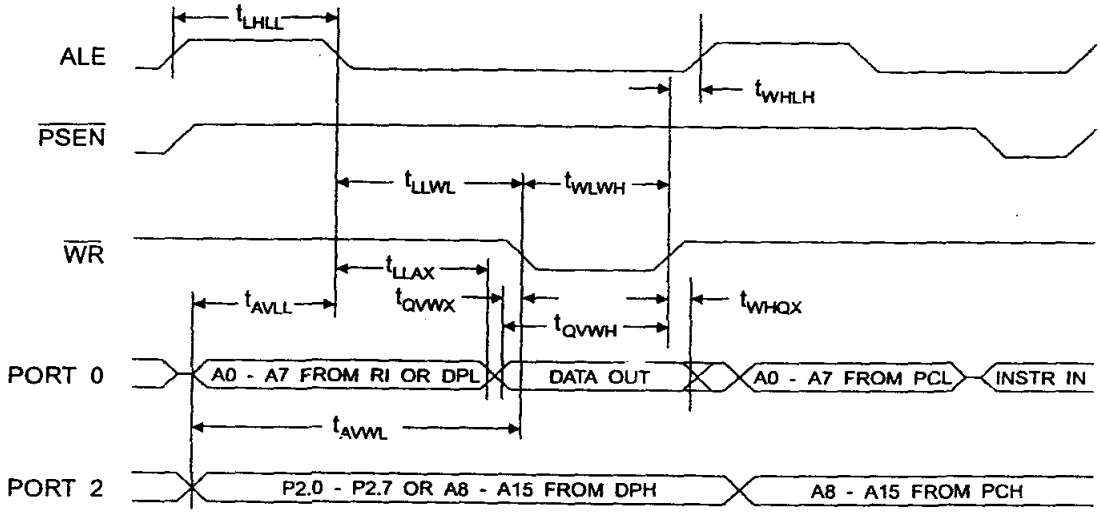
External Program Memory Read Cycle



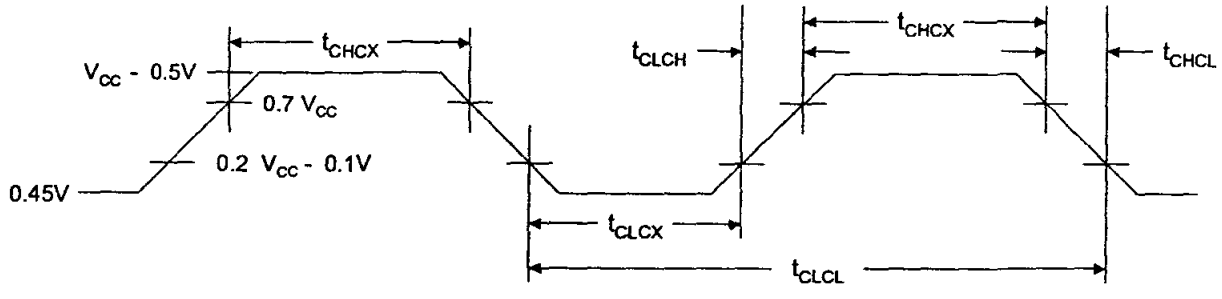
External Data Memory Read Cycle



External Data Memory Write Cycle



External Clock Drive Waveforms



External Clock Drive

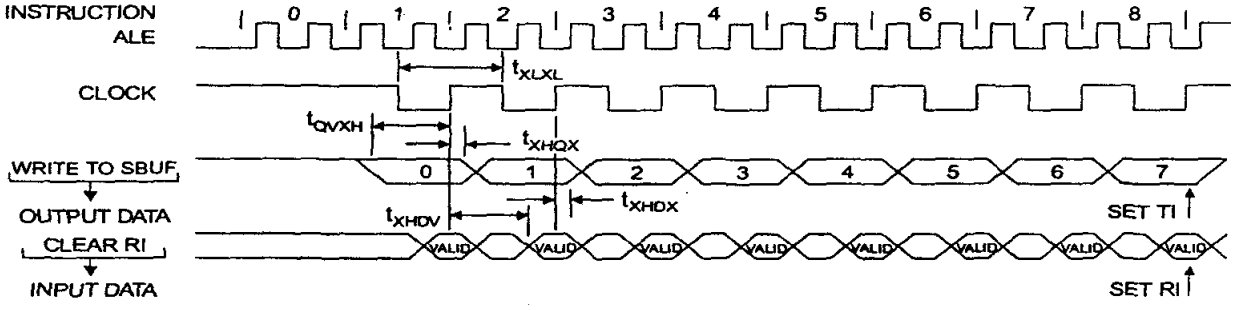
Symbol	Parameter	Min	Max	Units
$1/t_{CLCL}$	Oscillator Frequency	0	24	MHz
t_{CLCL}	Clock Period	41.6		ns
t_{CHCX}	High Time	15		ns
t_{CLCX}	Low Time	15		ns
t_{CLCH}	Rise Time		20	ns
t_{CHCL}	Fall Time		20	ns

Serial Port Timing: Shift Register Mode Test Conditions

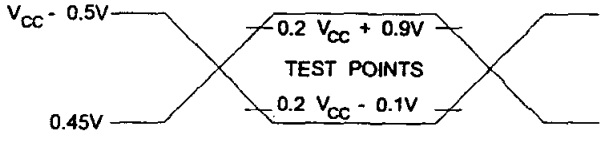
(V_{CC} = 5.0 V ± 20%; Load Capacitance = 80 pF)

Symbol	Parameter	12 MHz Osc		Variable Oscillator		Units
		Min	Max	Min	Max	
t_{XLXL}	Serial Port Clock Cycle Time	1.0		$12t_{CLCL}$		µs
t_{QVXH}	Output Data Setup to Clock Rising Edge	700		$10t_{CLCL}$-133		ns
t_{XHQX}	Output Data Hold After Clock Rising Edge	50		$2t_{CLCL}$-117		ns
t_{XHDX}	Input Data Hold After Clock Rising Edge	0		0		ns
t_{XHDV}	Clock Rising Edge to Input Data Valid		700		$10t_{CLCL}$-133	ns

Shift Register Mode Timing Waveforms

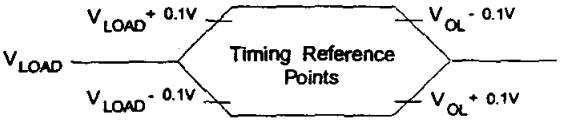


AC Testing Input/Output Waveforms[1]



Note: 1. AC Inputs during testing are driven at V_{CC} - 0.5V for a logic 1 and 0.45V for a logic 0. Timing measurements are made at V_{IH} min. for a logic 1 and V_{IL} max. for a logic 0.

Float Waveforms[1]



Note: 1. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when 100 mV change from the loaded V_{OH}/V_{OL} level occurs.

Ordering Information

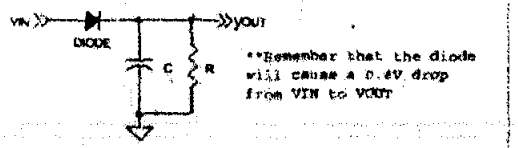
Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
12	5V ± 20%	AT89C51-12AC	44A	Commercial
		AT89C51-12JC	44J	(0°C to 70°C)
		AT89C51-12PC	40P6	
		AT89C51-12QC	44Q	
		AT89C51-12AI	44A	Industrial
		AT89C51-12JI	44J	(-40°C to 85°C)
		AT89C51-12PI	40P6	
		AT89C51-12QI	44Q	
		AT89C51-12AA	44A	Automotive
		AT89C51-12JA	44J	(-40°C to 105°C)
		AT89C51-12PA	40P6	
		AT89C51-12QA	44Q	
16	5V ± 20%	AT89C51-16AC	44A	Commercial
		AT89C51-16JC	44J	(0°C to 70°C)
		AT89C51-16PC	40P6	
		AT89C51-16QC	44Q	
		AT89C51-16AI	44A	Industrial
		AT89C51-16JI	44J	(-40°C to 85°C)
		AT89C51-16PI	40P6	
		AT89C51-16QI	44Q	
		AT89C51-16AA	44A	Automotive
		AT89C51-16JA	44J	(-40°C to 105°C)
		AT89C51-16PA	40P6	
		AT89C51-16QA	44Q	
20	5V ± 20%	AT89C51-20AC	44A	Commercial
		AT89C51-20JC	44J	(0°C to 70°C)
		AT89C51-20PC	40P6	
		AT89C51-20QC	44Q	
		AT89C51-20AI	44A	Industrial
		AT89C51-20JI	44J	(-40°C to 85°C)
		AT89C51-20PI	40P6	
		AT89C51-20QI	44Q	

Ordering Information

Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
24	5V ± 20%	AT89C51-24AC	44A	Commercial
		AT89C51-24JC	44J	(0°C to 70°C)
		AT89C51-24PC	44P6	
		AT89C51-24QC	44Q	
		AT89C51-24AI	44A	Industrial
		AT89C51-24JI	44J	(-40°C to 85°C)
		AT89C51-24PI	44P6	
		AT89C51-24QI	44Q	

Package Type	
44A	44 Lead, Thin Plastic Gull Wing Quad Flatpack (TQFP)
44J	44 Lead, Plastic J-Leaded Chip Carrier (PLCC)
40P6	40 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
44Q	44 Lead, Plastic Gull Wing Quad Flatpack (PQFP)

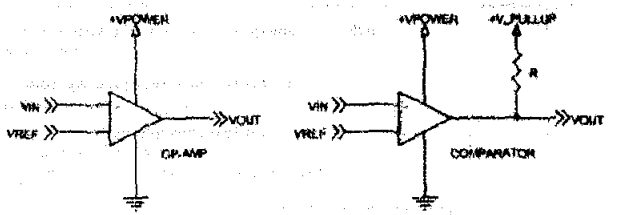
PEAK HOLD CIRCUIT



Peak Hold Circuit:
- Temporarily holds the peak voltage of the input signal.

Peak Hold Operation:
- When input signal peaks, current passes through diode to charge capacitor.
- When input drops below peak, the capacitor holds the peak value because the diode prevents reverse current flow.
- The "bleeder" resistor slowly discharges the holding capacitor so that the circuit can follow a decreasing peak voltage.

BASIC COMPARATOR CIRCUIT

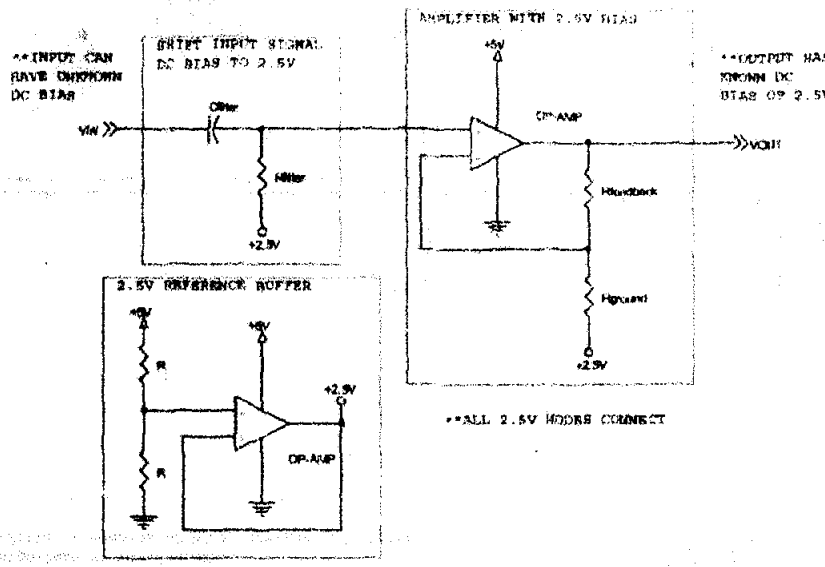


Op-Amp Comparator Operation:
- if VIN > VREF, VOUT=+VPOWER
- if VIN < VREF, VOUT=0

Comparator Operation:
- if VIN > VREF, VOUT=~+V_PULLUP
- if VIN < VREF, VOUT=0

Remember:
1. VIN and VREF must be between GND and +VPOWER
2. The + and - input terminals do not conduct any current.

BIASED AMPLIFIER CIRCUIT EXAMPLE



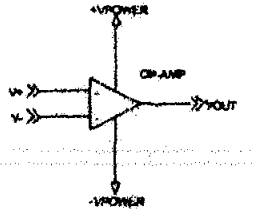
Comments:
This circuit is designed to discard the unwanted DC bias of a signal and amplify only the AC part. This is useful for processing audio, communications, and other kinds of AC signals. Ordinarily, both positive and negative supply voltages are required to properly amplify the positive and negative parts of an AC signal without "clipping" it at the output.

Because many systems don't have a negative power supply voltage available, this circuit is designed to cope with being powered only from +5V. To do this, we must DC bias the input signal to 2.5V using a high-pass filter. The filter removes the original DC (zero frequency) part of the input signal and replaces it with our own 2.5V. We then configure our amplifier to amplify only deviations from this 2.5V bias. Since we need a solid 2.5V reference to make the circuit work, we use a simple voltage divider to create 2.5V and then a buffer amplifier to make the reference "strong" in terms of current output.

You should think of the 2.5V reference as a simulated ground voltage. When using this simulated ground, +5V appears to be +2.5V and the real ground (0V) appears to be -2.5V. Thus we have created the positive and negative voltages that we needed to amplify a complete AC signal.

Title	Analog Circuit Design Reference	
Size: B	Document Number: <Doc>	Rev: A
Date: Sunday, May 10, 2015	Sheet 1 of 1	

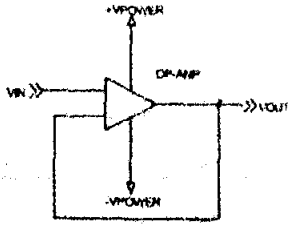
OP-AMP BASICS



Op-Amp General Operation Limits:
1. V+ and V- should stay between +VPOWER and -VPOWER
2. VOUT will not output voltages above +VPOWER or below -VPOWER

Op-Amp General Operation Rules:
1. These rules apply when operational limits are obeyed.
2. The + and - input terminals do not conduct any current.
3. VOUT = (V+ - V-)*A Note: A is typically between 10^3 to 10^8

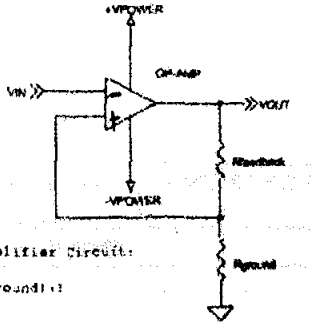
OP-AMP BUFFER CIRCUIT



Op-Amp Buffer Circuit:
1. VOUT = VIN

Uses:
- Use anywhere you need to know the voltage of a node in a circuit but cannot draw any current from that node.
- One typical use is at the output of a filter.
- Duplicate a voltage/signal while improving the current-output capacity

OP-AMP NON-INVERTING AMPLIFIER CIRCUIT

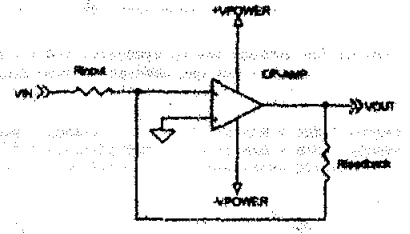


Op-Amp Non-Inverting Amplifier Circuit:
1. VOUT = GAIN*VIN
2. GAIN = (Rfeedback/Rground)+1

Uses:
- Amplify a signal without inverting it

Features:
- Minimal current drawn at input

OP-AMP INVERTING AMPLIFIER CIRCUIT

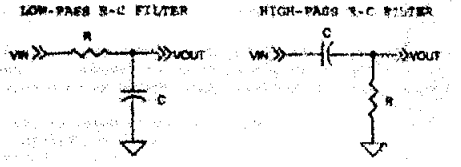


Op-Amp Inverting Amplifier Circuit:
1. VOUT = GAIN*VIN
2. GAIN = -(Rfeedback/Rinput)

Uses:
- Amplify a signal and invert it

Features:
- Low noise but current is drawn at input

R-C FILTERS



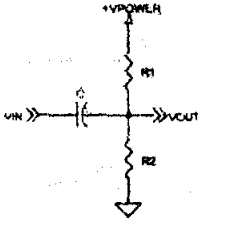
FOR BOTH HIGH AND LOW-PASS FILTERS

Fcutoff = 1/(2*pi*RC) (Hz)	Sinusoid Attenuation:
wcutoff = 1/RC [radians/sec]	-3dB at cutoff frequency
Tau = RC = 63% rise time	-6dB/octave
	-20db/decade

Low-Pass Filter Features:
-Filters, removes high-frequency noise. Averages the input.

High-Pass Filter Features:
-Filters, removes DC bias (constant DC offset).

DC-BIAS SHIFTER and HIGH-PASS R-C FILTER



VOUT DC BIAS = (R2/(R1+R2))*(-VPOWER)

Filter Fcutoff = 1/(2*pi*(R1||R2)*C)

- This circuit changes the DC bias of the input to a value controlled by the voltage divider formed by R1 and R2.
- By necessity, this circuit is also a high-pass filter

Title: Analog Circuit Design Reference		
Size: B	Document Number: <Doc>	Rev: A
Date: Saturday, May 10, 2003	Sheet 1 of 1	

LM2904,LM358/LM358A

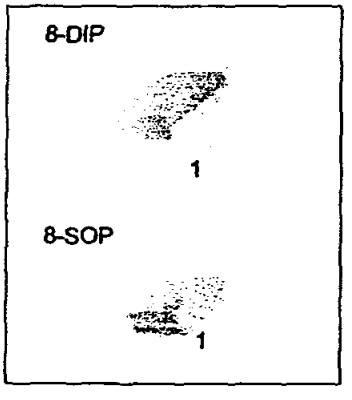
Dual Operational Amplifier

Features

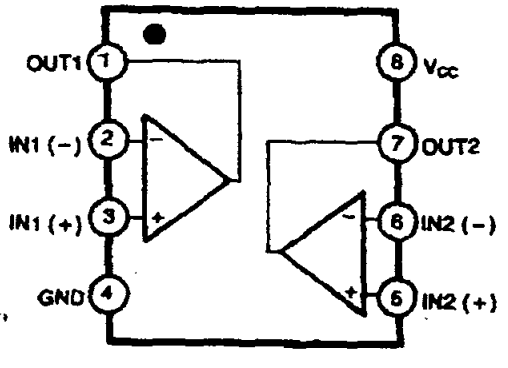
- Internally frequency compensated for unity gain
- Large DC voltage gain: 100dB
- Wide power supply range:
  LM358/LM358A: 3V~32V (or ±1.5V~16V)
  LM2904 : 3V~26V (or ±1.5V~13V)
- Input common-mode voltage range Includes ground
- Large output voltage swing: 0V DC to Vcc - 1.5V DC
- Power drain suitable for battery operation.

Description

The LM2904,LM358/LM358A consist of four independent, high gain, internally frequency compensated operational amplifiers which were designed specifically to operate from a single power supply over a wide range of voltage. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power Supply voltage. Application areas include transducer amplifier, DC gain blocks and all the conventional OP amp circuits which now can be easily implemented in single power Supply systems.

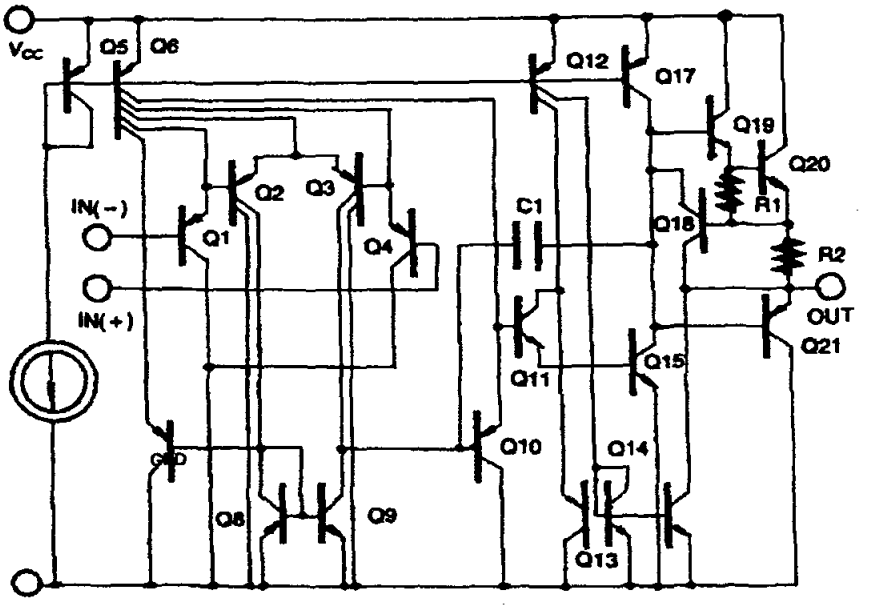


Internal Block Diagram



Schematic Diagram

(One section only)



Absolute Maximum Ratings

Parameter	Symbol	LM358/LM358A	LM2904	Unit
Supply Voltage	V_{CC}	±16 or 32	±13 or 26	V
Differential Input Voltage	$V_{I(DIFF)}$	32	26	V
Input Voltage	V_I	-0.3 to +32	-0.3 to +26	V
Output Short Circuit to GND $V_{CC} \leq V$, T_A = 25 °C(One Amp)	-	Continuous	Continuous	-
Operating Temperature Range	T_{OPR}	0 ~ + 70	-40 ~ + 85	°C
Storage Temperature Range	T_{STG}	-65 ~ + 150	-65 ~ + 150	°C

Electrical Characteristics

(V_{CC} = 5.0V, V_{EE} = GND, T = 25 °C, unless otherwise specified)

Parameter	Symbol	Conditions	LM358			LM2904			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage	V_{IO}	V_{CM} = 0V to V_{CC} -1.5V $V_{O(P)}$ = 1.4V, R_S = 0Ω	-	2.9	7.0	-	2.9	7.0	mV
Input Offset Current	I_{IO}	-	-	5	50	-	5	50	nA
Input Bias Current	I_{BIAS}	-	-	45	250	-	45	250	nA
Input Voltage Range	$V_{I(R)}$	V_{CC} = 30V (LM2904, V_{CC} = 26V)	0	-	Vcc-1.5	0	-	Vcc-1.5	V
Supply Current	I_{CC}	R_L = ∞, V_{CC} = 30V (LM2902, V_{CC} = 26V)	-	0.8	2.0	-	0.8	2.0	mA
		R_L = ∞,over full temperature range	-	0.5	1.2	-	0.5	1.2	mA
Large Signal Voltage Gain	GV	V_{CC} = 15V, R_L≥2KΩ $V_{O(P)}$ = 1V to 11V	25	100	-	25	100	-	V/mV
Output Voltage Swing	$V_{O(H)}$	V_{CC} = 30V, R_L = 2KΩ	26	-	-	22	-	-	V
		V_{CC} = 26V for 2904, R_L = 10KΩ	27	28	-	23	24	-	V
	$V_{O(L)}$	V_{CC} = 5V, R_L≥10KΩ	-	5	20		5	100	mV
Common-Mode Rejection Ratio	CMRR	-	65	80	-	50	80	-	dB
Power Supply Rejection Ratio	PSRR	-	65	100	-	50	100	-	dB
Channel Separation	CS	f = 1KHz to 20KHz	-	120	-	-	120	-	dB
Short Circuit to GND	ISC	-	-	40	60	-	40	60	mA
Output Current	I_{SOURCE}	$V_{I(+)}$ = 1V, $V_{I(-)}$ = 0V V_{CC} = 15V, $V_{O(P)}$ = 2V	10	30	-	10	30	-	mA
	I_{SINK}	$V_{I(+)}$ = 0V, $V_{I(-)}$ = 1V V_{CC} = 15V, $V_{O(P)}$ = 2V	10	15	-	10	15	-	mA
		$V_{I(+)}$ = 0V, $V_{I(-)}$ = 1V V_{CC} = 15V, $V_{O(P)}$ = 200mA	12	100	-	-	-	-	μA
Differential Input Voltage	$V_{I(DIFF)}$	-	-	-	Vcc	-	-	Vcc	V

Electrical Characteristics

(V_{CC}=5.0V, V_{EE}=GND, unless otherwise specified)
The following specification apply over the range of 0 °C ≤ T_A ≤ + 70 °C for the LM358 ; and the -40 °C ≤ T_A ≤ +85°Cfor the LM2904

Parameter	Symbol	Conditions	LM358			LM2904			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage	V_{IO}	V_{CM} = 0V to V_{CC} = 1.5V $V_{O(P)}$ = 1.4V, R_S = 0Ω	-	-	9.0	-	-	10.0	mV
Input Offset Voltage Drift	$\Delta V_{IO}/\Delta T$	R_S = 0Ω	-	7.0	-	-	7.0	-	μV/°C
Input Offset Current	I_{IO}	-	-	-	150	-	45	200	nA
Input Offset Current Drift	$\Delta I_{IO}/\Delta T$	-	-	10	-	-	10	-	pA/°C
Input Bias Current	I_{BIAS}	-	-	40	500	-	40	500	nA
Input Voltage Range	$V_{I(R)}$	V_{CC} = 30V (LM2904 , V_{CC} = 26V)	0	-	Vcc=2.0	0	-	Vcc=2.0	V
Large Signal Voltage Gain	G_V	V_{CC} = 15V, R_L≥2.0KΩ $V_{O(P)}$ = 1V to 11V	15	-	-	15	-	-	V/mV
Output Voltage Swing	$V_{O(H)}$	V_{CC} = 30V, R_L = 2KΩ	26	-	-	26	-	-	V
		V_{CC} = 26V for 2904, R_L = 10KΩ	27	28	-	27	28	-	V
	$V_{O(L)}$	V_{CC} = 5V, R_L≥10KΩ	-	5	20	-	5	20	mV
Output Current	I_{SOURCE}	$V_{I(+)}$ = 1V, $V_{I(-)}$ = 0V V_{CC} = 15V, $V_{O(P)}$ = 2V	10	30	-	10	30	-	mA
	I_{SINK}	$V_{I(+)}$ = 0V, $V_{I(-)}$ = 1V V_{CC} = 15V, $V_{O(P)}$ = 2V	5	9	-	5	9	-	mA
Differential Input Voltage	$V_{I(DIFF)}$	-	-	-	V_{CC}	-	-	V_{CC}	V

Electrical Characteristics

(V_{CC} = 5.0V. V_{EE}=GND. T_A=25 °C, unless otherwise specified)

Parameter	Symbol	Conditions		LM358A			Unit
				Min.	Typ.	Max.	
Input Offset Voltage	V_{IO}	V_{CM} = 0V to V_{CC} = 1.5V $V_{O(P)}$ = 1.4V, R_S = 0Ω		-	2.0	3.0	mV
Input Offset Current	I_{IO}	-		-	5	30	nA
Input Bias Current	I_{BIAS}	-		-	45	100	nA
Input Voltage Range	$V_{I(R)}$	V_{CC} = 30V		0	-	V_{CC}=1.5	V
Supply Current	I_{CC}	R_L = ∞,V_{CC} = 30V		-	0.8	2.0	mA
		RL = ∞,over full temperature range		-	0.5	1.2	mA
Large Signal Voltage Gain	G_V	V_{CC} = 15V, R_L≥2KΩ V_O = 1V to 11V		25	100	-	V/mV
Output Voltage Swing	V_{OH}	V_{CC} = 30V	R_L = 2KΩ	26		-	V
		V_{CC} = 26V for 2904	R_L = 10KΩ	27	28	-	V
	$V_{O(L)}$	V_{CC} = 5V, R_L≥10KΩ		-	5	20	mV
Common-Mode Rejection Ratio	CMRR	-		65	85	-	dB
Power Supply Rejection Ratio	PSRR	-		65	100	-	dB
Channel Separation	CS	f = 1KHz to 20KHz		-	120	-	dB
Short Circuit to GND	I_{SC}	-		-	40	60	mA
Output Current	I_{SOURCE}	$V_{I(+)}$ = 1V, $V_{I(-)}$ = 0V V_{CC} = 15V, $V_{O(P)}$ = 2V		20	30	-	mA
	I_{SINK}	$V_{I(+)}$ = 1V, $V_{I(-)}$ = 0V V_{CC} = 15V, $V_{O(P)}$ = 2V		10	15	-	mA
		V_{in+} = 0V, V_{in-} = 1V $V_{O(P)}$ = 200mV		12	100	-	µA
Differential Input Voltage	$V_{I(DIFF)}$	-		-	-	V_{CC}	V

Electrical Characteristics

(V_{CC} = 5.0V, V_{EE} = GND. unless otherwise specified)
The following specification apply over the range of 0 °C ≤ T_A ≤ +70 °C for the LM358A

Parameter	Symbol	Conditions	LM358A			Unit
			Min.	Typ.	Max.	
Input Offset Voltage	V_{IO}	V_{CM} = 0V to V_{CC} = 1.5V $V_{O(P)}$ = 1.4V, R_S = 0Ω	-	-	5.0	mV
Input Offset Voltage Drift	$\Delta V_{IO}/\Delta T$	-	-	7.0	20	μV/°C
Input Offset Current	I_{IO}	-	-	-	75	nA
Input Offset Current Drift	$\Delta I_{IO}/\Delta T$	-	-	10	300	pA/°C
Input Bias Current	I_{BIAS}	-	-	40	200	nA
Input Common-Mode Voltage Range	$V_{I(R)}$	V_{CC} = 30V	0	-	V_{CC}=2.0	V
Output Voltage Swing	$V_{O(H)}$	V_{CC} = 30V, R_L = 2KΩ	26	-	-	V
		V_{CC} = 30V, R_L = 10KΩ	27	28	-	V
	$V_{O(L)}$	V_{CC} = 5V, R_L≥10KΩ	-	5	20	mV
Large Signal Voltage Gain	G_V	V_{CC} = 15V, R_L≥2.0KΩ $V_{O(P)}$ = 1V to 11V	15	-	-	V/mV
Output Current	I_{SOURCE}	$V_{I(+)}$ = 1V, $V_{I(-)}$ = 0V V_{CC} = 15V, $V_{O(P)}$ = 2V	10	30	-	mA
	I_{SINK}	$V_{I(+)}$ = 1V, $V_{I(-)}$ = 0V V_{CC} = 15V, $V_{O(P)}$ = 2V	5	9	-	mA
Differential Input Voltage	$V_{I(DIFF)}$	-	-	-	V_{CC}	V

National Semiconductor

October 1989

CD4051BM/CD4051BC Single 8-Channel Analog Multiplexer/Demultiplexer
CD4052BM/CD4052BC Dual 4-Channel Analog Multiplexer/Demultiplexer
CD4053BM/CD4053BC Triple 2-Channel Analog Multiplexer/Demultiplexer

General Description

These analog multiplexers/demultiplexers are digitally controlled analog switches having low "ON" impedance and very low "OFF" leakage currents. Control of analog signals up to $15V_{p-p}$ can be achieved by digital signal amplitudes of 3–15V. For example, if $V_{DD}=5V$, $V_{SS}=0V$ and $V_{EE}=-5V$, analog signals from −5V to +5V can be controlled by digital inputs of 0–5V. The multiplexer circuits dissipate extremely low quiescent power over the full $V_{DD}-V_{SS}$ and $V_{DD}-V_{EE}$ supply voltage ranges, independent of the logic state of the control signals. When a logical "1" is present at the inhibit input terminal all channels are "OFF".

CD4051BM/CD4051BC is a single 8-channel multiplexer having three binary control inputs, A, B, and C, and an inhibit input. The three binary signals select 1 of 8 channels to be turned "ON" and connect the input to the output.

CD4052BM/CD4052BC is a differential 4-channel multiplexer having two binary control inputs, A and B, and an inhibit input. The two binary input signals select 1 or 4 pairs of channels to be turned on and connect the differential analog inputs to the differential outputs.

CD4053BM/CD4053BC is a triple 2-channel multiplexer having three separate digital control inputs, A, B, and C, and an inhibit input. Each control input selects one of a pair of channels which are connected in a single-pole double-throw configuration.

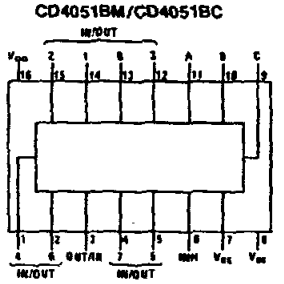
Features

- Wide range of digital and analog signal levels: digital 3–15V, analog to $15V_{p-p}$
- Low "ON" resistance: 80Ω (typ.) over entire $15V_{p-p}$ signal-input range for $V_{DD}-V_{EE}=15V$
- High "OFF" resistance: channel leakage of ±10 pA (typ.) at $V_{DD}-V_{EE}=10V$
- Logic level conversion for digital addressing signals of 3–15V ($V_{DD}-V_{SS}=3-15V$) to switch analog signals to 15 V_{p-p} ($V_{DD}-V_{EE}=15V$)
- Matched switch characteristics: $\Delta R_{ON}=5\Omega$ (typ.) for $V_{DD}-V_{EE}=15V$
- Very low quiescent power dissipation under all digital-control input and supply conditions: 1 μW (typ.) at $V_{DD}-V_{SS}=V_{DD}-V_{EE}=10V$
- Binary address decoding on chip

Connection Diagrams

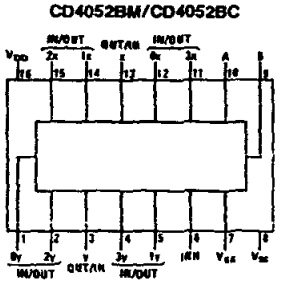
Dual-In-Line Packages

CD4051BM/CD4051BC



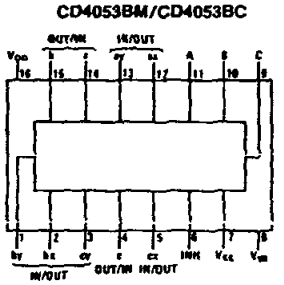
TOP VIEW

CD4052BM/CD4052BC



TOP VIEW

CD4053BM/CD4053BC



TOP VIEW

TL/F/5662–1

Order Number CD4051B, CD4052B, or CD4053B

RRD-B30M105/Printed in U. S. A.

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

DC Supply Voltage (V_{DD})	$-0.5\ V_{DC}$ to $+18\ V_{DC}$
Input Voltage (V_{IN})	$-0.5\ V_{DC}$ to $V_{DD}+0.5\ V_{DC}$
Storage Temperature Range (T_S)	$-65°C$ to $+150°C$
Power Dissipation (P_D)	
Dual-In-Line	700 mW
Small Outline	500 mW
Lead Temp. (T_L) (soldering, 10 sec.)	260°C

Recommended Operating Conditions

DC Supply Voltage (V_{DD})	$+5\ V_{DC}$ to $+15\ V_{DC}$
Input Voltage (V_{IN})	0V to $V_{DD}\ V_{DC}$
Operating Temperature Range (T_A)	
4051BM/4052BM/4053BM	$-55°C$ to $+125°C$
4051BC/4052BC/4053BC	$-40°C$ to $+85°C$

DC Electrical Characteristics (Note 2)

Symbol	Parameter	Conditions		−55°C		+25°			+125°C		Units
				Min	Max	Min	Typ	Max	Min	Max	
I_{DD}	Quiescent Device Current	$V_{DD}=5V$			5			5		150	μA
		$V_{DD}=10V$			10			10		300	μA
		$V_{DD}=15V$			20			20		600	μA
Signal Inputs (V_{IS}) and Outputs (V_{OS})											
R_{ON}	"ON" Resistance (Peak for $V_{EE}\le V_{IS}\le V_{DD}$)	$R_L=10\ k\Omega$ (any channel selected)	$V_{DD}=2.5V$, $V_{EE}=-2.5V$ or $V_{DD}=5V$, $V_{EE}=0V$		800		270	1050		1300	Ω
			$V_{DD}=5V$ $V_{EE}=-5V$ or $V_{DD}=10V$, $V_{EE}=0V$		310		120	400		550	Ω
			$V_{DD}=7.5V$, $V_{EE}=-7.5V$ or $V_{DD}=15V$, $V_{EE}=0V$		200		80	240		320	Ω
ΔR_{ON}	Δ"ON" Resistance Between Any Two Channels	$R_L=10\ k\Omega$ (any channel selected)	$V_{DD}=2.5V$, $V_{EE}=-2.5V$ or $V_{DD}=5V$, $V_{EE}=0V$				10				Ω
			$V_{DD}=5V$, $V_{EE}=-5V$ or $V_{DD}=10V$, $V_{EE}=0V$				10				Ω
			$V_{DD}=7.5V$, $V_{EE}=-7.5V$ or $V_{DD}=15V$, $V_{EE}=0V$				5				Ω
	"OFF" Channel Leakage Current, any channel "OFF"	$V_{DD}=7.5V$, $V_{EE}=-7.5V$ $O/I=\pm7.5V$, $I/O=0V$			±50		±0.01	±50		±500	nA
	"OFF" Channel Leakage Current, all channels "OFF" (Common OUT/IN)	Inhibit = 7.5V	CD4051		±200		±0.08	±200		±2000	nA
		$V_{DD}=7.5V$, $V_{EE}=-7.5V$, $O/I=0V$,	CD4052		±200		±0.04	±200		±2000	nA
		$I/O=\pm7.5V$	CD4053		±200		±0.02	±200		±2000	nA
Control Inputs A, B, C and Inhibit											
V_{IL}	Low Level Input Voltage	$V_{EE}=V_{SS}$ $R_L=1\ k\Omega$ to V_{SS} $I_{IS}<2\ \mu A$ on all OFF channels $V_{IS}=V_{DD}$ thru $1\ k\Omega$									
		$V_{DD}=5V$			1.5			1.5		1.5	V
		$V_{DD}=10V$			3.0			3.0		3.0	V
		$V_{DD}=15V$			4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	$V_{DD}=5$		3.5		3.5			3.5		V
		$V_{DD}=10$		7		7			7		V
		$V_{DD}=15$		11		11			11		V

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All voltages measured with respect to V_{SS} unless otherwise specified.

DC Electrical Characteristics (Note 2) (Continued)

Symbol	Parameter	Conditions		−40°C		+25°C			+85°C		Units
				Min	Max	Min	Typ	Max	Min	Max	
I_{IN}	Input Current	$V_{DD}=15V$, $V_{EE}=0V$ $V_{IN}=0V$			−0.1		-10^{-5}	−0.1		−1.0	μA
		$V_{DD}=15V$, $V_{EE}=0V$ $V_{IN}=15V$			0.1		10^{-5}	0.1		1.0	μA
I_{DD}	Quiescent Device Current	$V_{DD}=5V$			20			20		150	μA
		$V_{DD}=10V$			40			40		300	μA
		$V_{DD}=15V$			80			80		600	μA
Signal Inputs (V_{IS}) and Outputs (V_{OS})											
R_{ON}	"ON" Resistance (Peak for $V_{EE} \le V_{IS} \le V_{DD}$)	$R_L=10\ k\Omega$ (any channel selected)	$V_{DD}=2.5V$, $V_{EE}=-2.5V$ or $V_{DD}=5V$, $V_{EE}=0V$		850		270	1050		1200	Ω
			$V_{DD}=5V$, $V_{EE}=-5V$ or $V_{DD}=10V$, $V_{EE}=0V$		330		120	400		520	Ω
			$V_{DD}=7.5V$, $V_{EE}=-7.5V$ or $V_{DD}=15V$, $V_{EE}=0V$		210		80	240		300	Ω
ΔR_{ON}	Δ"ON" Resistance Between Any Two Channels	$R_L=10\ k\Omega$ (any channel selected)	$V_{DD}=2.5V$, $V_{EE}=-2.5V$ or $V_{DD}=5V$, $V_{EE}=0V$				10				Ω
			$V_{DD}=5V$ $V_{EE}=-5V$ or $V_{DD}=10V$, $V_{EE}=0V$				10				Ω
			$V_{DD}=7.5V$, $V_{EE}=-7.5V$ or $V_{DD}=15V$, $V_{EE}=0V$				5				Ω
	"OFF" Channel Leakage Current, any channel "OFF"	$V_{DD}=7.5V$, $V_{EE}=-7.5V$ $O/I=\pm7.5V$, $I/O=0V$			±50		±0.01	±50		±500	nA
	"OFF" Channel Leakage Current, all channels "OFF" (Common OUT/IN)	Inhibit = 7.5V CD4051 $V_{DD}=7.5V$, $V_{EE}=-7.5V$, CD4052 $O/I=0V$ $I/O=\pm7.5V$ CD4053			±200 ±200 ±200		±0.08 ±0.04 ±0.02	±200 ±200 ±200		±2000 ±2000 ±2000	nA nA nA
Control Inputs A, B, C and Inhibit											
V_{IL}	Low Level Input Voltage	$V_{EE}=V_{SS}$ $R_L=1\ k\Omega$ to V_{SS} $I_{IS}<2\ \mu A$ on all OFF Channels $V_{IS}=V_{DD}$ thru 1 kΩ									
		$V_{DD}=5V$			1.5			1.5		1.5	V
		$V_{DD}=10V$			3.0			3.0		3.0	V
		$V_{DD}=15V$			4.0			4.0		4.0	V
V_{IH}	High Level Input Voltage	$V_{DD}=5$		3.5		3.5			3.5		V
		$V_{DD}=10$		7		7			7		V
		$V_{DD}=15$		11		11			11		V
I_{IN}	Input Current	$V_{DD}=15V$, $V_{EE}=0V$ $V_{IN}=0V$			−0.1		-10^{-5}	−0.1		−1.0	μA
		$V_{DD}=15V$, $V_{EE}=0V$ $V_{IN}=15V$			0.1		10^{-5}	0.1		1.0	μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All voltages measured with respect to V_{SS} unless otherwise specified.

AC Electrical Characteristics* $T_A = 25°C$, $t_r = t_f = 20$ ns, unless otherwise specified.

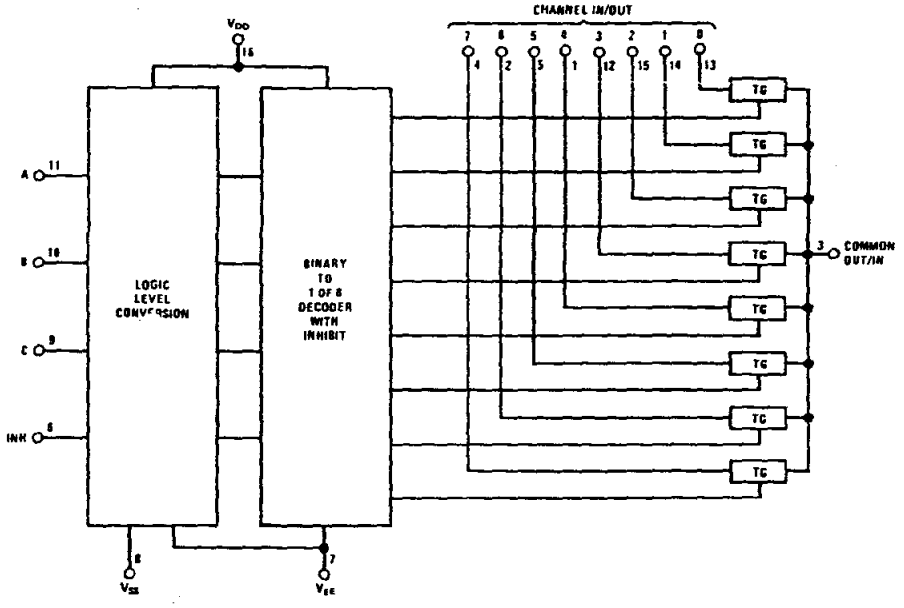
Symbol	Parameter	Conditions	V_{DD}	Min	Typ	Max	Units
t_{PZH}, t_{PZL}	Propagation Delay Time from Inhibit to Signal Output (channel turning on)	$V_{EE} = V_{SS} = 0V$ $R_L = 1\ k\Omega$ $C_L = 50$ pF	5V 10V 15V		600 225 160	1200 450 320	ns ns ns
t_{PHZ}, t_{PLZ}	Propagation Delay Time from Inhibit to Signal Output (channel turning off)	$V_{EE} = V_{SS} = 0V$ $R_L = 1\ k\Omega$ $C_L = 50$ pF	5V 10V 15V		210 100 75	420 200 150	ns ns ns
C_{IN}	Input Capacitance *Control input* Signal Input (IN/OUT)				 5 10	 7.5 15	 pF pF
C_{OUT}	Output Capacitance (common OUT/IN)						
	CD4051 CD4052 CD4053	$V_{EE} = V_{SS} = 0V$	10V 10V 10V		30 15 8		pF pF pF
C_{IOS}	Feedthrough Capacitance				0.2		pF
C_{PD}	Power Dissipation Capacitance						
	CD4051 CD4052 CD4053				110 140 70		pF pF pF
Signal Inputs (V_{IS}) and Outputs (V_{OS})							
	Sine Wave Response (Distortion)	$R_L = 10\ k\Omega$ $f_{IS} = 1$ kHz $V_{IS} = 5\ V_{p-p}$ $V_{EE} = V_{SI} = 0V$	10V		0.04		%
	Frequency Response, Channel "ON" (Sine Wave Input)	$R_L = 1\ k\Omega$, $V_{EE} = 0V$, $V_{IS} = 5V_{p-p}$, $20 \log_{10} V_{OS}/V_{IS} = -3$ dB	10V		40		MHz
	Feedthrough, Channel "OFF"	$R_L = 1\ k\Omega$, $V_{EE} = V_{SS} = 0V$, $V_{IS} = 5V_{p-p}$, $20 \log_{10} V_{OS}/V_{IS} = -40$ dB	10V		10		MHz
	Crosstalk Between Any Two Channels (frequency at 40 dB)	$R_L = 1\ k\Omega$, $V_{EE} = V_{SS} = 0V$, $V_{IS}(A) = 5V_{p-p}$ $20 \log_{10} V_{OS}(B)/V_{IS}(A) = -40$ dB (Note 3)	10V		3		MHz
t_{PHL} t_{PLH}	Propagation Delay Signal Input to Signal Output	$V_{EE} = V_{SS} = 0V$ $C_L = 50$ pF	5V 10V 15V		25 15 10	55 35 25	ns ns ns
Control Inputs, A, B, C and Inhibit							
	Control Input to Signal Crosstalk	$V_{EE} = V_{SS} = 0V$, $R_L = 10\ k\Omega$ at both ends of channel. Input Square Wave Amplitude = 10V	10V		65		mV (peak)
t_{PHL}, t_{PLH}	Propagation Delay Time from Address to Signal Output (channels "ON" or "OFF")	$V_{EE} = V_{SS} = 0V$ $C_L = 50$ pF	5V 10V 15V		500 180 120	1000 360 240	ns ns ns

*AC Parameters are guaranteed by DC correlated testing.

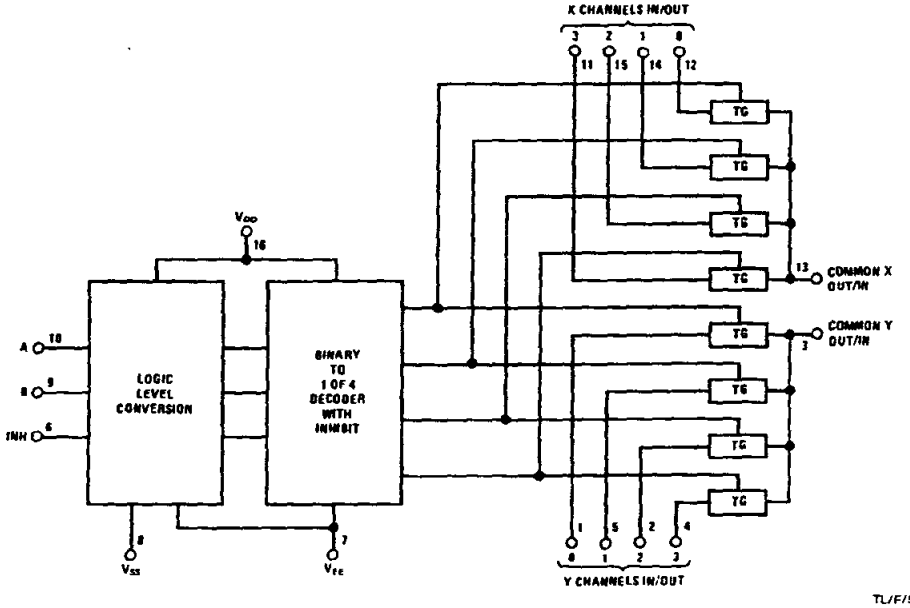
Note 3: A, B are two arbitrary channels with A turned "ON" and B "OFF".

Block Diagrams

CD4051BM/CD4051BC



CD4052BM/CD4052BC



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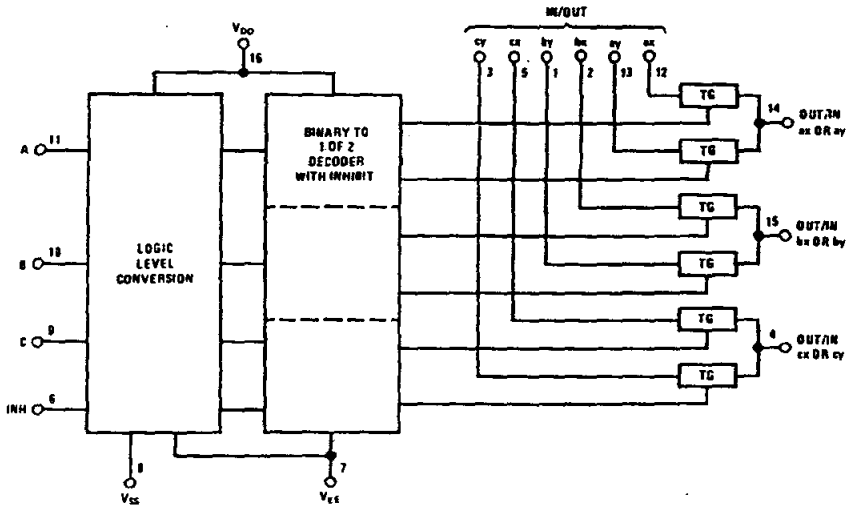
Block Diagrams (Continued)

CD4053BM/CD4053BC



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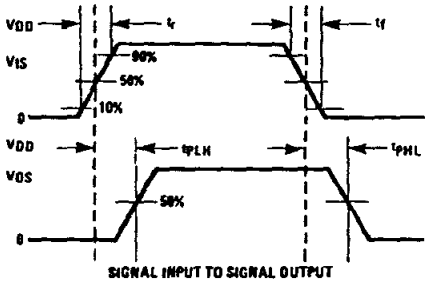
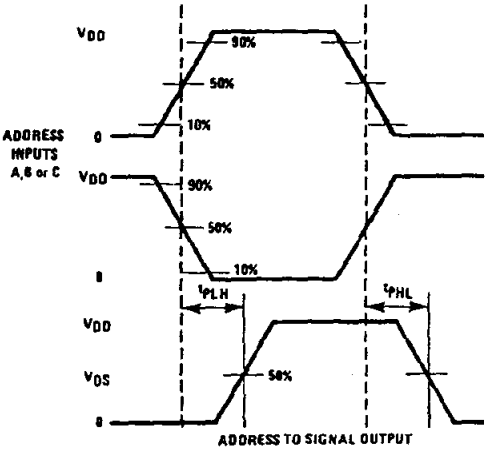
Truth Table

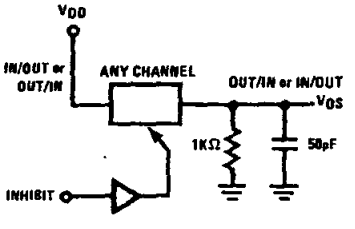
INPUT STATES				"ON" CHANNELS		
INHIBIT	C	B	A	CD4051B	CD4052B	CD4053B
0	0	0	0	0	0X, 0Y	cx, bx, ax
0	0	0	1	1	1X, 1Y	cx, bx, ay
0	0	1	0	2	2X, 2Y	cx, by, ax
0	0	1	1	3	3X, 3Y	cx, by, ay
0	1	0	0	4		cy, bx, ax
0	1	0	1	5		cy, bx, ay
0	1	1	0	6		cy, by, ax
0	1	1	1	7		cy, by, ay
1	*	*	*	NONE	NONE	NONE

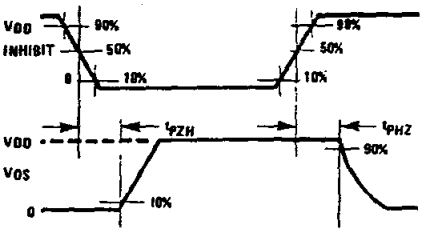
*Don't Care condition.

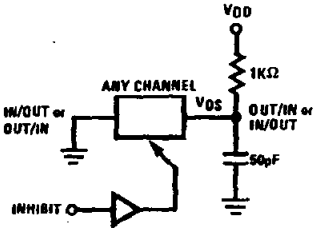
Switching Time Waveforms

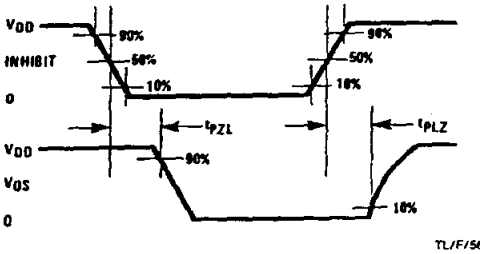












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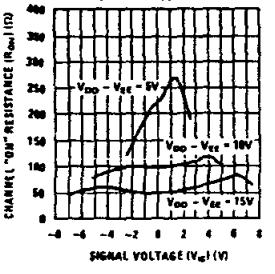
Special Considerations

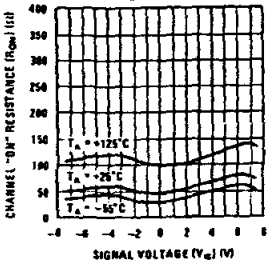
In certain applications the external load-resistor current may include both V_{DD} and signal-line components. To avoid drawing V_{DD} current when switch current flows into IN/OUT pin, the voltage drop across the bidirectional switch must not exceed 0.6V at $T_A \leq 25°C$, or 0.4V at $T_A > 25°C$ (calculated from R_{ON} values shown). No V_{DD} current will flow through R_L if the switch current flows into OUT/IN pin.

Typical Performance Characteristics

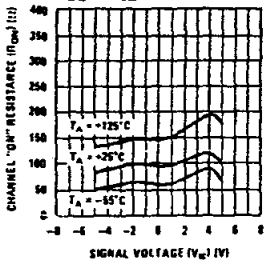
"ON" Resistance vs Signal Voltage for $T_A = 25°C$



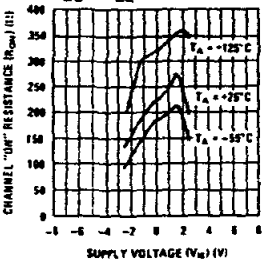
"ON" Resistance as a Function of Temperature for $V_{DD} - V_{EE} = 15V$



"ON" Resistance as a Function of Temperature for $V_{DD} - V_{EE} = 10V$



"ON" Resistance as a Function of Temperature for $V_{DD} - V_{EE} = 5V$



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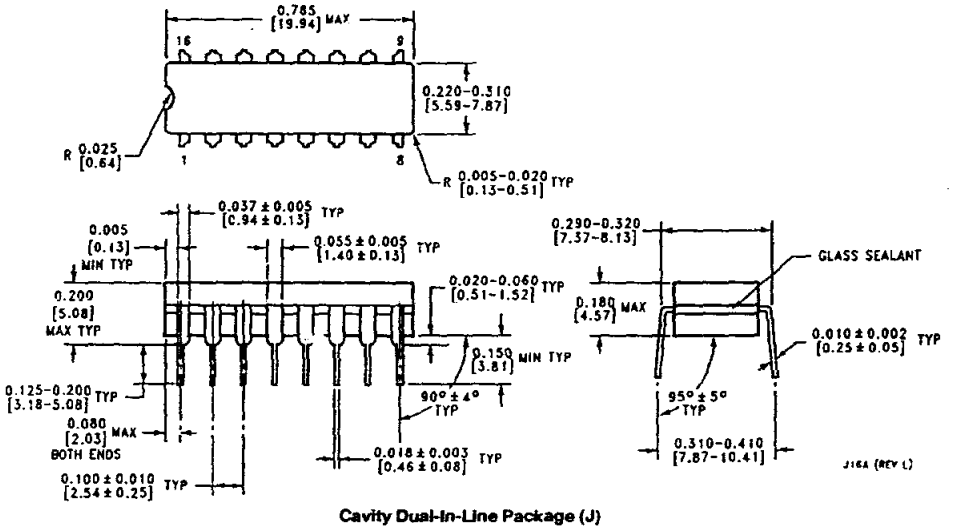
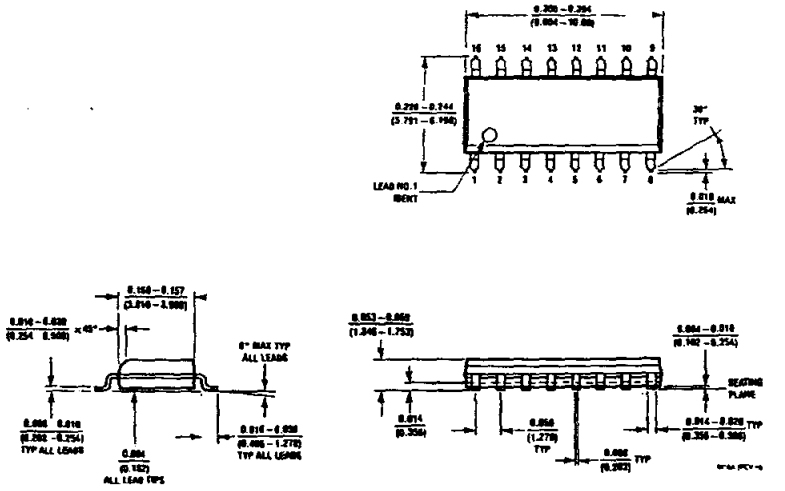
Physical Dimensions inches (millimeters)

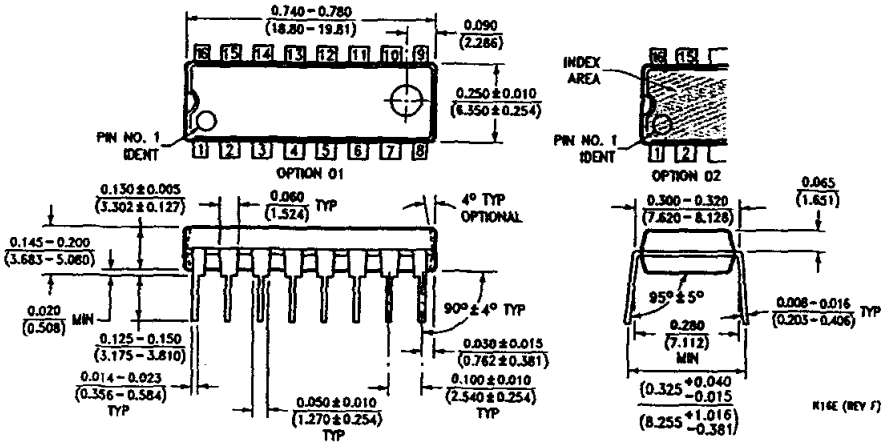


Cavity Dual-In-Line Package (J)
Order Number CD4051BMJ, CD4051BCJ, CD4052BMJ, CD4052BCJ, CD4053BMJ or CD4053BCJ
NS Package Number J16A



Small Outline Package (M)
Order Number CD4051BCM, CD4052BCM or CD4053BCM
NS Package Number M16A

Physical Dimensions inches (millimeters) (Continued)



Molded Dual-In-Line Package (N)
Order CD4051BM, CD4051BC,
CD4052BM, CD4052BC, CD4053BM, CD4053BC
NS Package Number N16E

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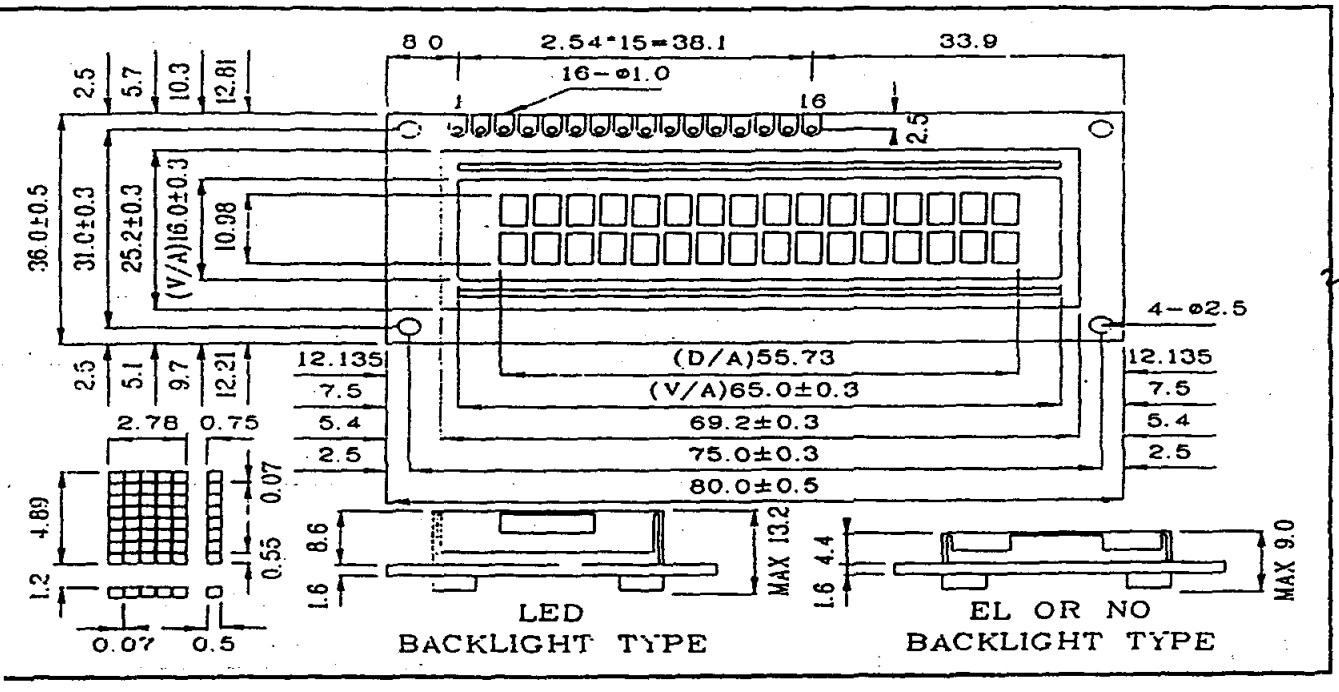
DOT MATRIX
LIQUID CRYSTAL DISPLAY
MODULE

USER MANUAL

1. Mechanical Specification

ITEM	STANDARD VALUE						UNIT
NUMBER OF CHARACTERS	16 CHARACTERS X 2 LINES						--
CHARACTER FORMAT	5 X 8 DOTS						--
MODULE DIMENSION	80.0 (W) X 36.0 (H) X 13.2 (T)						mm
VIEWING DISPLAY AREA	65.0 (W) X 16.0 (H)						mm
ACTIVE DISPLAY AREA	55.73 (W) X 10.98 (H)						mm
CHARACTER SIZE	2.78 (W) X 4.89 (H)						mm
CHARACTER PITCH	3.53 (W) X 6.09 (H)						mm
DOT SIZE	0.50 (W) X 0.55 (H)						mm
DOT PITCH	0.57 (W) X 0.62 (H)						mm
APPROX. WEIGHT	30						g
LCD TYPE	STN , Gray , 1/16 DUTY , 6 O'clock						
BACKLIGHT TYPE	LED		USE INVERTER				
BACKLIGHT INPUT	DC +5V	V	100	mA			Hz
INVERTER INPUT		V		mA			Hz
BACKLIGHT Half-Life TIME	100,000						HR.

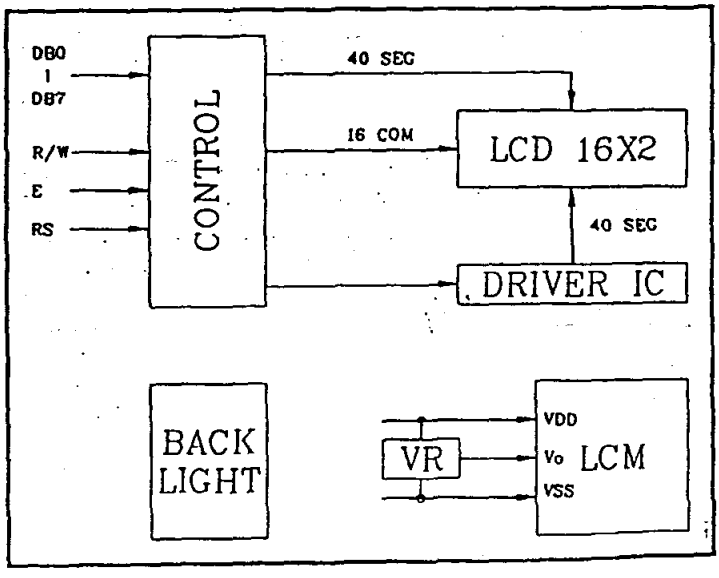
2. Mechanical Diagram



3. Interface Pin Connections

NO	SYMBOL	LEVEL	FUNCTION
1	VSS	--	GND (0V)
2	VDD	H/L	DC +5V
3	VO	H/L	Contrast Adjust
4	RS	H/L	Register select
5	R/W	H/L	Read/Write
6	E	H,H→L	Enable signal
7	DB0	H/L	Data Bit 0
8	DB1	H/L	Data Bit 1
9	DB2	H/L	Data Bit 2
10	DB3	H/L	Data Bit 3
11	DB4	H/L	Data Bit 4
12	DB5	H/L	Data Bit 5
13	DB6	H/L	Data Bit 6
14	DB7	H/L	Data Bit 7
15	A(+)	DC +5V	LED Backlight +
16	K(-)	0V	LED Backlight -

4. Black Diagram



5. Absolute Maximum Ratings

ITEM	SYMBOL	MIN.	TYPE	MAX.	UNIT
OPERATING TEMPERATURE	TOP	0/-20	--	+50/+70	℃
STORAGE TEMPERATURE	TST	-10/-30	--	+60/+80	℃
INPUT VOLAGE	VI	VSS	--	VDD	V
SUPPLY VOLTAGE FOR LOGIC	VDD-VSS	--	5.0	6.5	V
SUPPLY VOLTAGE FOR LCD	VDD-VO	--	--	6.5	V
STATIC ELECTRICITY	Be sure that you are grounded when handing LCM.				

6. Electrical Characteristics

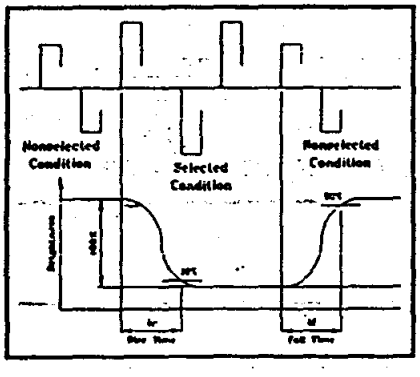
ITEM	SYN	CONDITION	MIN.	TYPE	MAX.	UNIT
SUPPLY VOLTAGE FOR LOGIC	VDD-VSS	--	4.5	5.0	5.5	V
SUPPLY VOLTAGE FOR LCD	VDD-VO	Ta= 0/-20 ℃	--	4.8/5.0	--	V
		Ta= 25℃	--	4.4	--	V
		Ta= +50/+70 ℃	--	4.1/3.9	--	V
INPUT HIGH VOLTAGE	VIH	--	2.2	--	VDD	V
INPUT LOW VOLTAGE	VIL	--	0	--	0.6	V
OUTPUT HIGH VOLTAGE	VOH	--	2.4	--	--	V
OUTPUT LOW VOLTAGE	VOL	--	--	--	0.4	V
SUPPLY CURRENT	IDD	VDD=+5V	--	3.0	4.5	mA

7. Optical Characteristics

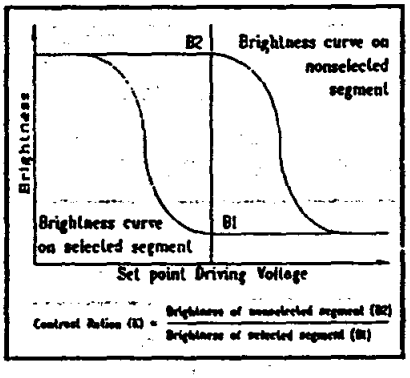
ITEM	SYM	CONDITION	MIN.	TYPE	MAX.	UNIT
VIEW ANGLE (V)	θ	CR≧2	-10	--	40	deg.
VIEW ANGLE (H)	φ	CR≧2	-30	--	30	deg.
CONTRAST RATIO	CR	--	--	5	--	--
RESPONSE TIME	TON	--	--	180	230	mS
RESPONSE TIME	TOFF	--	--	100	150	mS

8. Optical Definitions

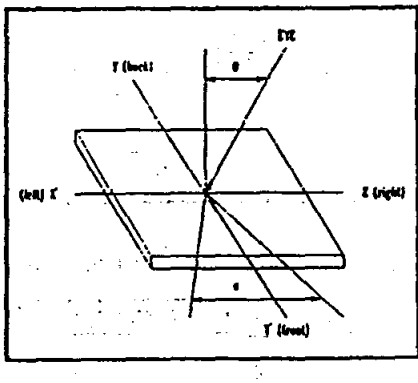
Response Time



Contrast Ration



View Angle

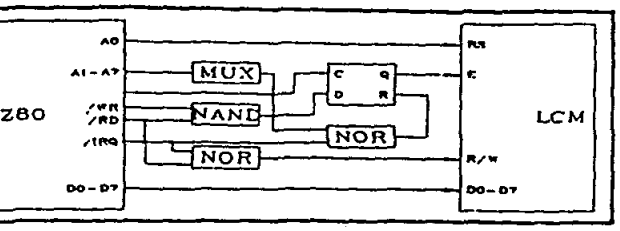


9. Display Address

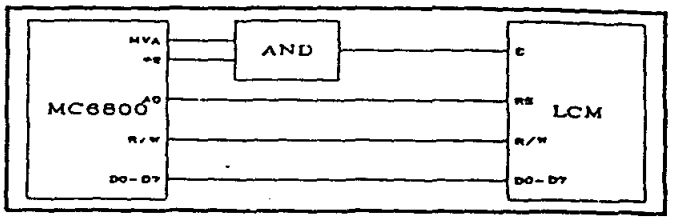
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
Line 1	80	81	82	83	84	85	86	87	88	89	8A	8B	8C	8D	8E	8F				
Line 2	C0	C1	C2	C3	C4	C5	C6	C7	C8	C9	CA	CB	CC	CD	CE	CF				
Line 3																				
Line 4																				

	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40
Line 1																				
Line 2																				
Line 3																				
Line 4																				

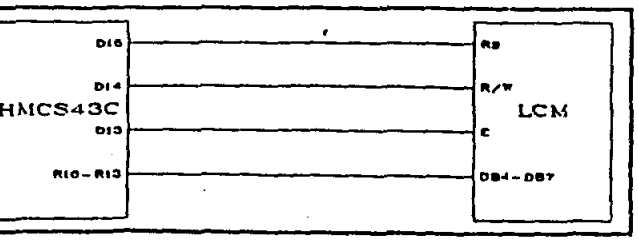
10.1 Interface to Z-80 CPU



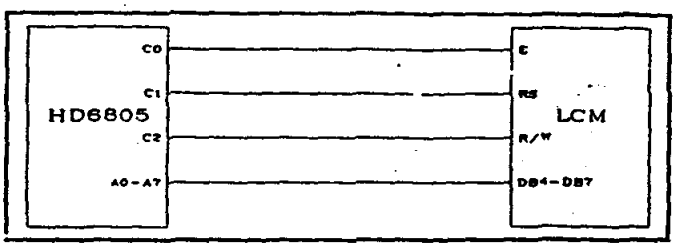
10.2 Interface to MC6800 CPU



10.3 Interface to 4-bit CPU (HMCS43C)



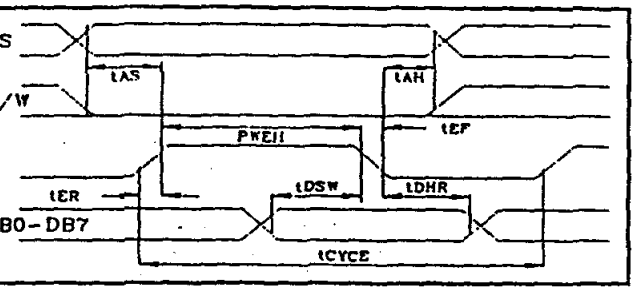
10.4 Interface to HD6805 MP



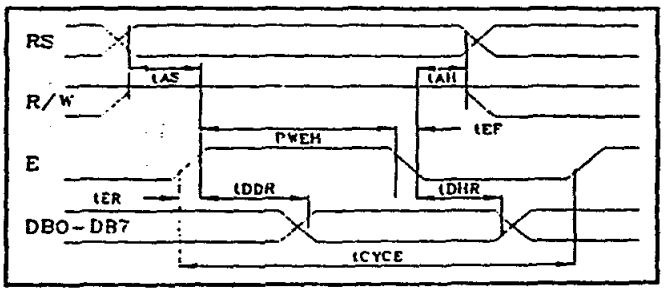
. Timing Control

11.1 Write and Read Operation

Write Operation

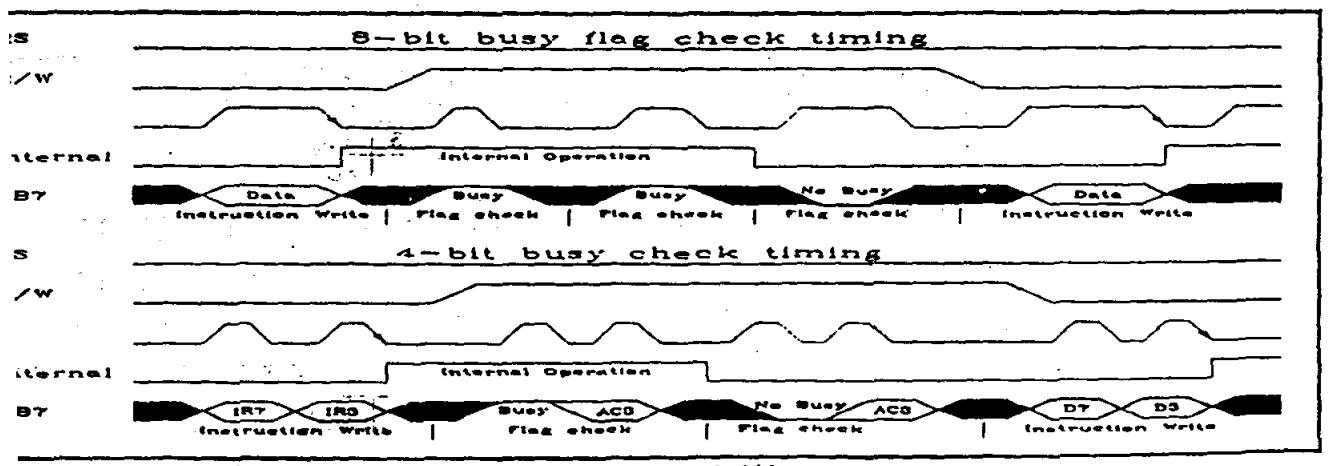


Read Operation



Item	Symbol	Limit (Min.)	Limit (Max.)	Unit
Enable Cycle Time	tCYCE	1000	--	ns
Enable Pules Width (High level)	PWEH	450	--	ns
Enable Rise/Fall Time	tER,tEF	--	25	ns
Address Set-Up Time (RS,R/W,E)	tAS	100	--	ns
Address Hole Time	tAH	10	--	ns
Data Set-Up Time	tDSW	100	--	ns
Data Delay Time	tDDR	--	190	ns
Data Hold Time	tDHR	20	--	ns

11.2 Busy flag check timing

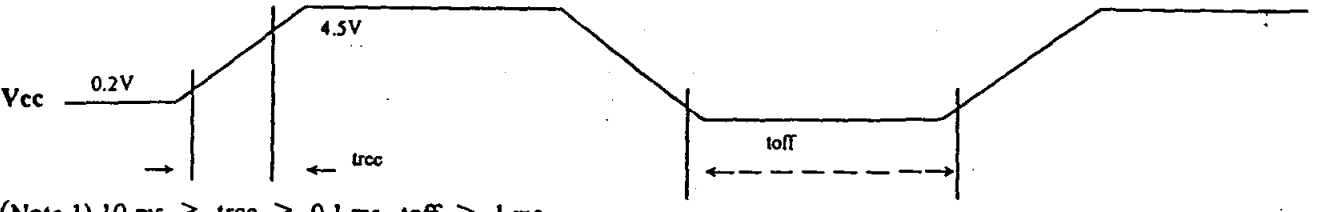


: IR7, IR3 : Instruction 7th bit , 3rd bit ; AC3 : Address Counter 3rd bit.

12. Initialization of LCM

The LCM automatically initializes (reset) when power is turned on using the internal reset circuit. If the power supply conditions for correctly operating of the internal reset circuit are not met, initialization by instruction is required. Use the procedure is next page for initialization.

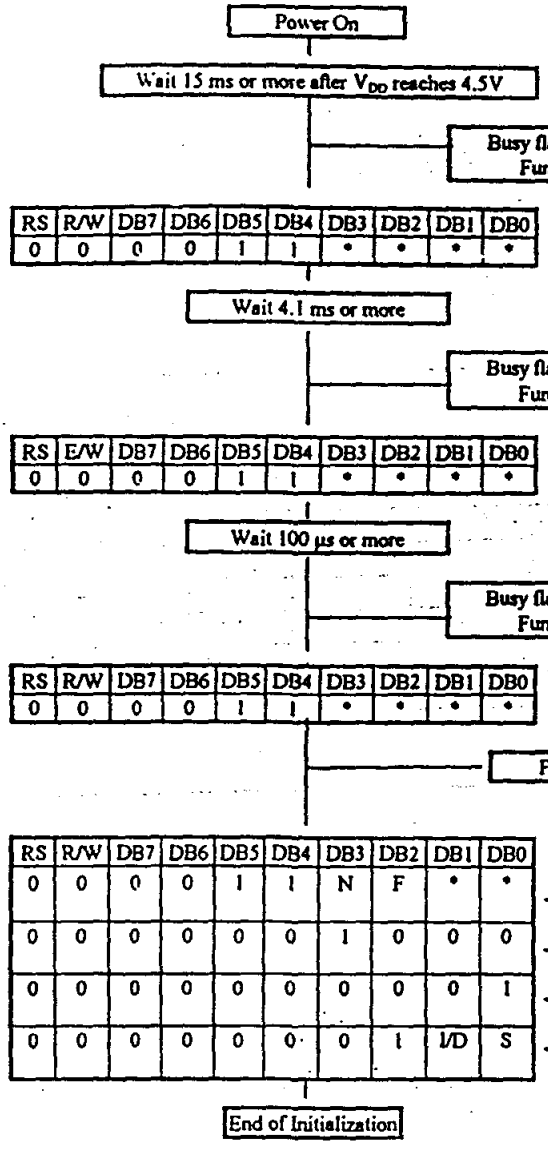
Internal Power Supply reset



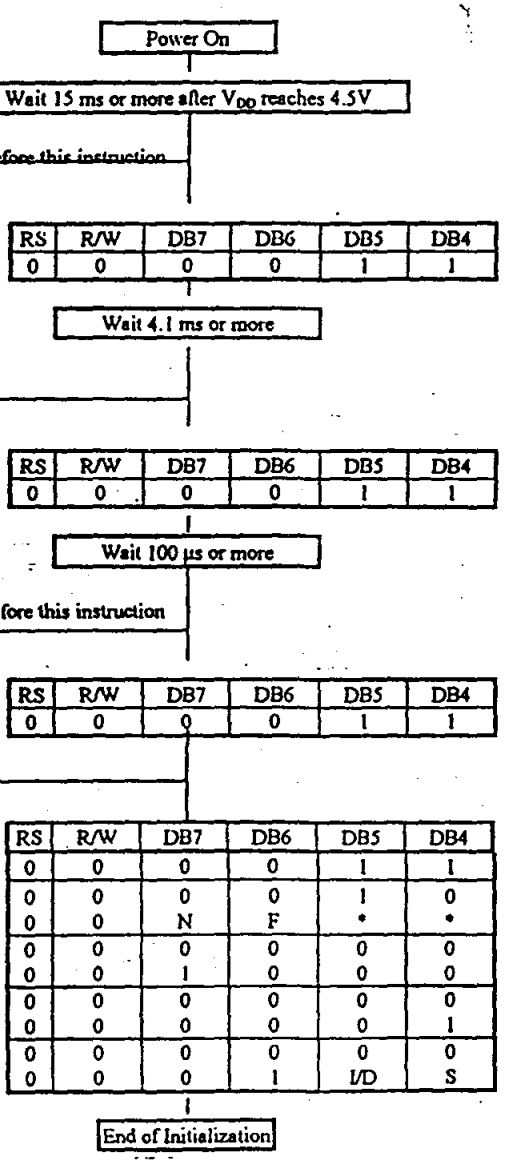
(Note 1) 10 ms ≥ trcc ≥ 0.1 ms, toff ≥ 1 ms.
(Note 2) toff stipulates the time of power OFF for momentary power supply dip or when power supply cycles ON and OFF.

Item	Symbol	Test condition	Limit (Min.)	Limit (Max.)	Unit
Power supply rise time	trcc	--	0.1	10	ms
Power supply off time	toff	--	1	--	ms

1) 8 Bit Interface



2) 4 Bit Interface



- Busy flag is checked after instructions are completed. If busy flay isn't checked, the waiting time between instructions should be longer than execution time of these instructions.

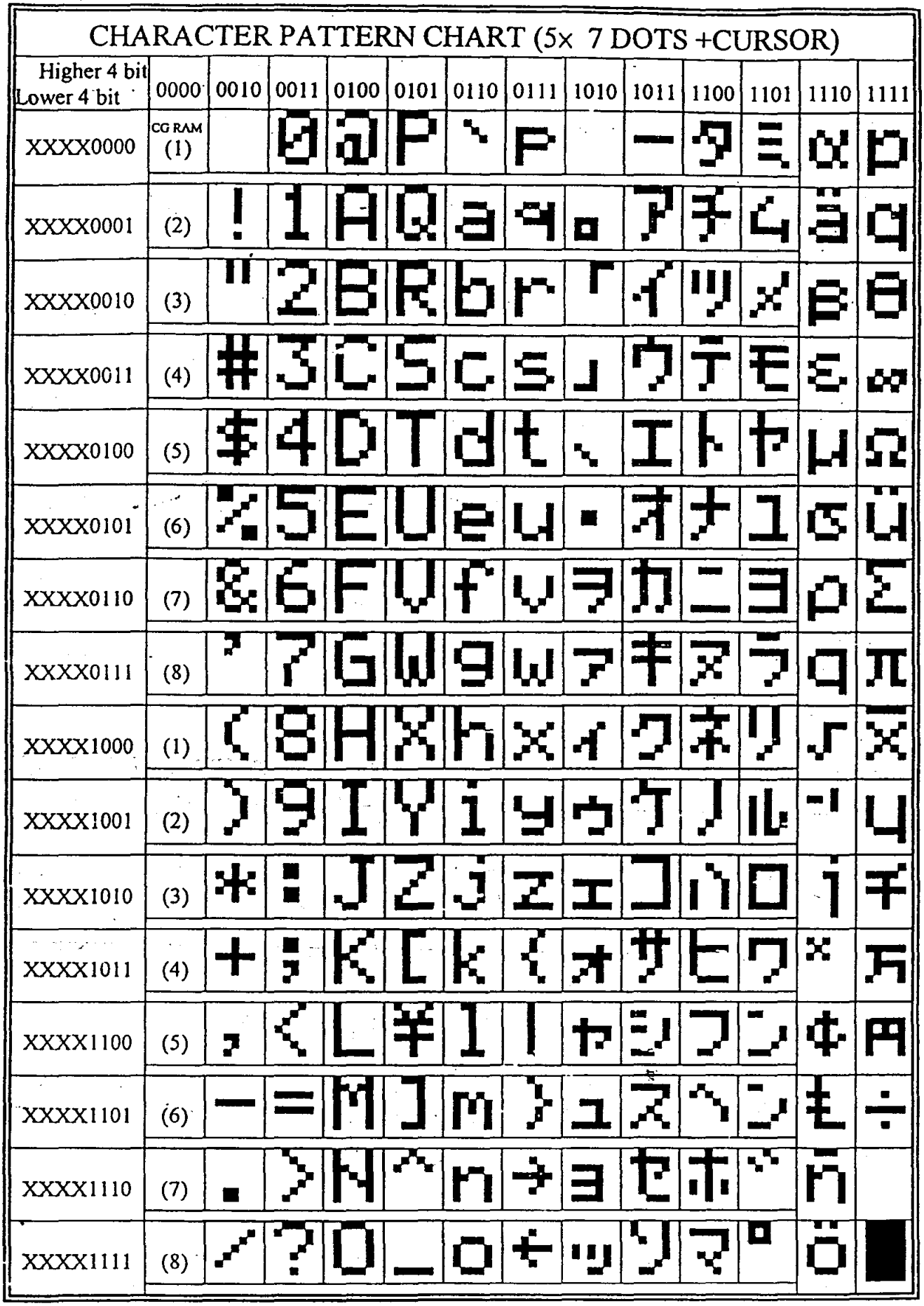
3. Instruction Set

FUNCTION	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	DESCRIPTION	EXECU. TIME* (MAX.)
Clear Display	0	0	0	0	0	0	0	0	0	1	Clears entire display and returns the cursor to home position (address 0).	1.64ms
Return Home	0	0	0	0	0	0	0	0	1	x	Return the cursor to the home position. Also returns the display being shifted to the original position. DD RAM contents remain unchanged.	1.64ms
Entry mode set	0	0	0	0	0	0	0	1	I/D	S	Set cursor move direct and specifies display shift.These operations are performed during data rite/read. For normal operation, set S to zero. I/D=1 : increment ; 0 :decrement ;S=1 : accompanies display shift when data is written, for normal operation, set to zero.	40 μs
Display ON/OFF control	0	0	0	0	0	0	1	D	C	B	Set ON/OFF all display(D),cursor ON/OFF(C), and blink of cursor position character(B). D=1: ON display; 0:OFF display. C=1: ON cursor;0: OFF cursor. B=1: ON blink cursor; 0: OFF blink cursor.	40 μs
Cursor or Display shift	0	0	0	0	0	1	S/C	R/L	x	x	Move the cursor and shift the display without changing DD RAM contents. S/C=1: Display shift; 0:Cursor move. R/L=1: shift to right; 0: shift to left.	40 μs
Function Set	0	0	0	0	1	DL	N	F	x	x	Set the interface data length (DL). Number of display lines (N) and character font (F). DL=1: 8 bits; 0:4 bits. N=1: 2 lines; 0: 1 lines. F=1: 5x10 dots; 0: 5x7 dots.	40 μs
Set CG RAM address	0	0	0	1	ACG						Set CG RAM address. CG RAM data is sent and received after this setting.	40 μs
Set DD RAM address	0	0	1	ADD							Set DD RAM address. DD RAM data is sent and received after this setting	40 μs
Read busy flag & address	0	1	BF	AC							Reads Busy Flag (BF) indicating internal operation is being performed and reads address counter contents. BF=1: internally operating. 0: can accept instruction	1 μs
Write Data to CG/DDRAM	1	0	WRITE DATA								Write data into DD RAM or CG RAM.	40 μs
Read Data for CG/DDRAM	1	1	READ DATA								Read data from DD RAM or CG RAM	40 μs

4. User Font Patterns (CG RAM Character)

Character Code (DD RAM data)		CG RAM Address		Character Pattern (CG RAM data)	
Hi 76543210 Lo		543 210		Hi 765 4 3 2 1 0 Lo	
0000x000		000	000	xxx 1 1 1 1 0	
			001	xxx 1 0 0 0 1	
			010	xxx 1 0 0 0 1	
			011	xxx 1 1 1 1 0	
			100	xxx 1 0 1 0 0	
			101	xxx 1 0 0 1 0	
			110	xxx 1 0 0 0 1	
			111	xxx 0 0 0 0 0	
0000x001		001	000	xxx 1 0 0 0 1	
			001	xxx 0 1 0 1 0	
			010	xxx 1 1 1 1 1	
			011	xxx 0 0 1 0 0	
			100	xxx 1 1 1 1 1	
			101	xxx 0 0 1 1 0	
			110	xxx 0 0 1 0 0	
			111	xxx 0 0 0 0 0	
----------		----------		----------	
0000x111		111	000		
			001		
			010		
			011		
			100		
			101		
			110		
			111		

18. Character Generator ROM Map

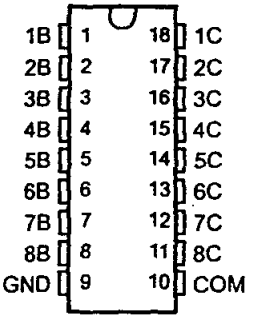


ULN2803A
DARLINGTON TRANSISTOR ARRAY

SLRS049 – FEBRUARY 1997

- **500 mA Rated Collector Current (Single Output)**
- **High-Voltage Outputs . . . 50 V**
- **Output Clamp Diodes**
- **Inputs Compatible With Various Types of Logic**
- **Relay Driver Applications**
- **Compatible with ULN2800A Series**

N PACKAGE
(TOP VIEW)



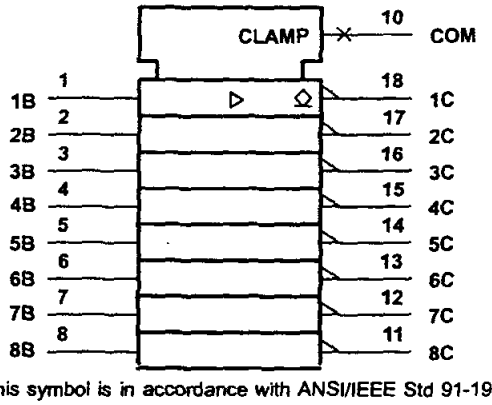
description

The ULN2803A is a monolithic high-voltage, high-current Darlington transistor array. The device consists of eight npn Darlington pairs that feature high-voltage outputs with common-cathode clamp diodes for switching inductive loads. The collector-current rating of each Darlington pair is 500 mA. The Darlington pairs may be paralleled for higher current capability.

Applications include relay drivers, hammer drivers, lamp drivers, display drivers (LED and gas discharge), line drivers, and logic buffers. The ULN2803A has a 2.7-kΩ series base resistor for each Darlington pair for operation directly with TTL or 5-V CMOS devices.

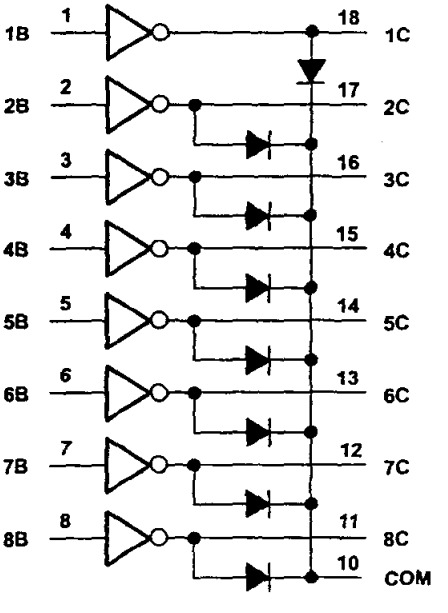
The ULN2803A is offered in a standard 18-pin dual in-line (N) package. The device is characterized for operation over the temperature range of –20°C to 85°C.

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



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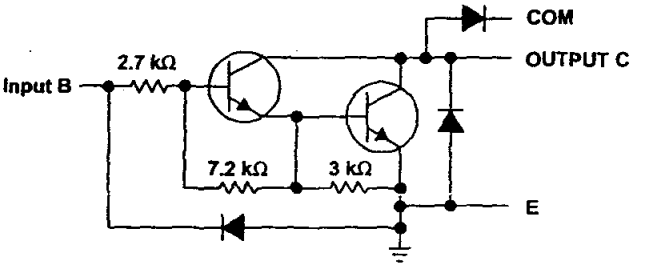
schematic (each Darlington pair)



absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)†

Collector-emitter voltage	50 V
Input voltage (see Note 1)	30 V
Continuous collector current	500 mA
Output clamp diode current	500 mA
Total substrate-terminal current	–2.5 A
Continuous dissipation at (or below) 25°C free-air temperature	1150 mW
Operating free-air temperature range, T_A	–20°C to 85°C
Storage temperature range, T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds:	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages values, unless otherwise noted, are with respect to the emitter/substrate terminal GND.

electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_{CEX}	Collector cutoff current	V_{CE} = 50 V, I_I = 0, See Figure 1				50	µA
$I_{I(off)}$	Off-state input current	V_{CE} = 50 V, I_C = 500 µA, T_A = 70°C, See Figure 2		50	65		µA
$I_{I(on)}$	Input current	V_I = 3.85 V, See Figure 3			0.93	1.35	mA
$V_{I(on)}$	On-state input voltage	V_{CE} = 2 V, See Figure 4	I_C = 200 mA			2.4	V
			I_C = 250 mA			2.7	
			I_C = 300 mA			3	
$V_{CE(sat)}$	Collector emitter saturation voltage	I_I = 250 µA, See Figure 5	I_C = 100 mA,		0.9	1.1	V
		I_I = 350 µA, See Figure 5	I_C = 200 mA,		1	1.3	
		I_I = 500 µA, See Figure 5	I_C = 350 mA,		1.3	1.6	
I_R	Clamp diode reverse current	V_R = 50 V, See Figure 6				50	µA
V_F	Clamp diode forward voltage	I_F = 350 mA, See Figure 7			1.7	2	V
C_i	Input capacitance	V_I = 0 V, f = 1 MHz			15	25	pF

switching characteristics at 25°C free-air temperature

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	V_S = 50 V, C_L = 15 pF,	R_L = 163 Ω, See Figure 8		130		ns
t_{PHL}	Propagation delay time, high-to-low level output				20		
V_{OH}	High-level output voltage after switching	V_S = 50 V, See Figure 9	I_O = 300 mA,	V_S–20			mV

PARAMETER MEASUREMENT INFORMATION

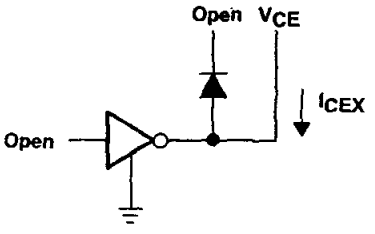


Figure 1. I_{CEX} Test Circuit

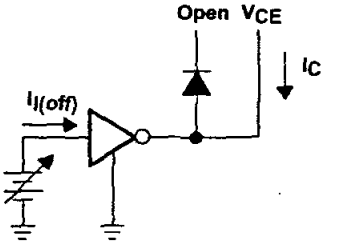


Figure 2. $I_{I(off)}$ Test Circuit

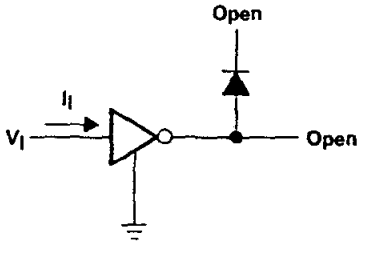


Figure 3. $I_{I(on)}$ Test Circuit

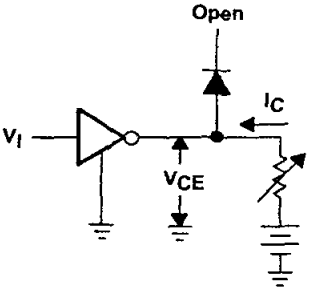


Figure 4. $V_{I(on)}$ Test Circuit

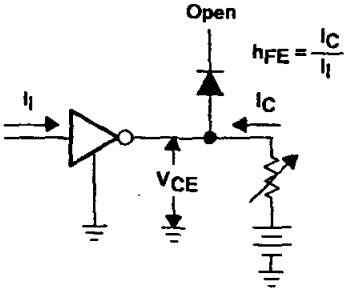


Figure 5. h_{FE}, $V_{CE(sat)}$ Test Circuit

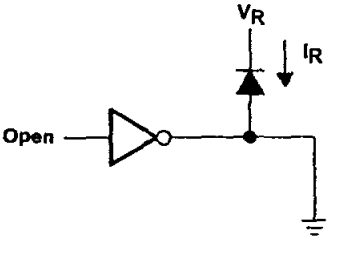


Figure 6. I_R Test Circuit

PARAMETER MEASUREMENT INFORMATION

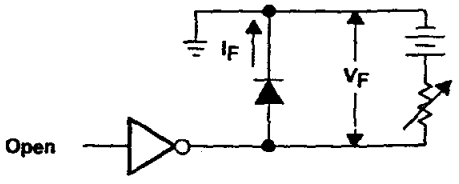
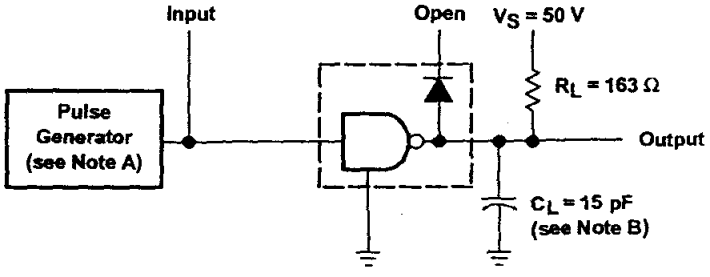
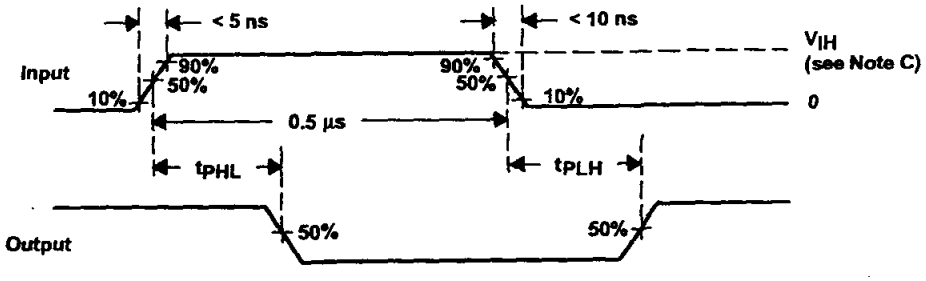


Figure 7. V_F Test Circuit



Test Circuit

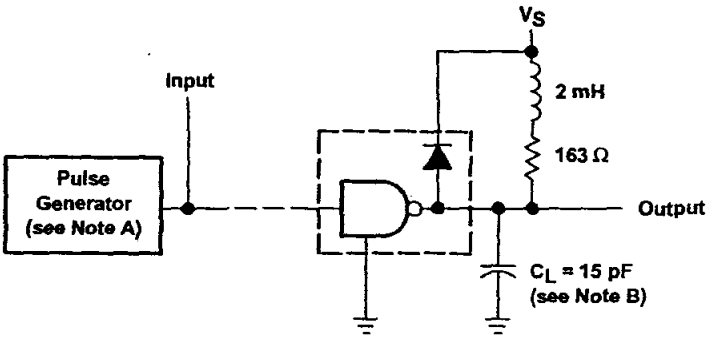


Voltage Waveforms

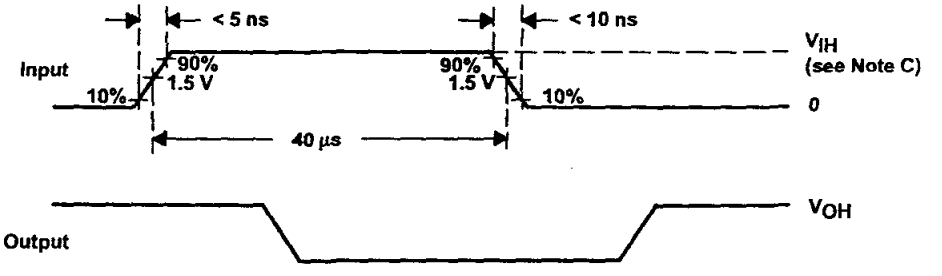
NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.
C. V_{IH} = 3 V

Figure 8. Propagation Delay Times

PARAMETER MEASUREMENT INFORMATION



Test Circuit



Voltage Waveforms

NOTES: A. The pulse generator has the following characteristics: PRR = 12.5 KHz, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.
C. V_{IH} = 3 V

Figure 9. Latch-Up Test

BIODATA

BIODATA

Nama	: Welly Agus Sanjaya
NRP	: 5103099020
Tempat, Tgl. Lahir	: Surabaya, 18-08-1980
Agama	: Katolik
Alamat Rumah	: Jl. Kapas Gading Madya 3/7 Surabaya

Riwayat Pendidikan :

- Tahun 1993 Lulus SD Angela, Surabaya.
- Tahun 1996 Lulus SMP Katolik Angelus Custos, Surabaya.
- Tahun 1999 Lulus SMA Frateran , Surabaya.