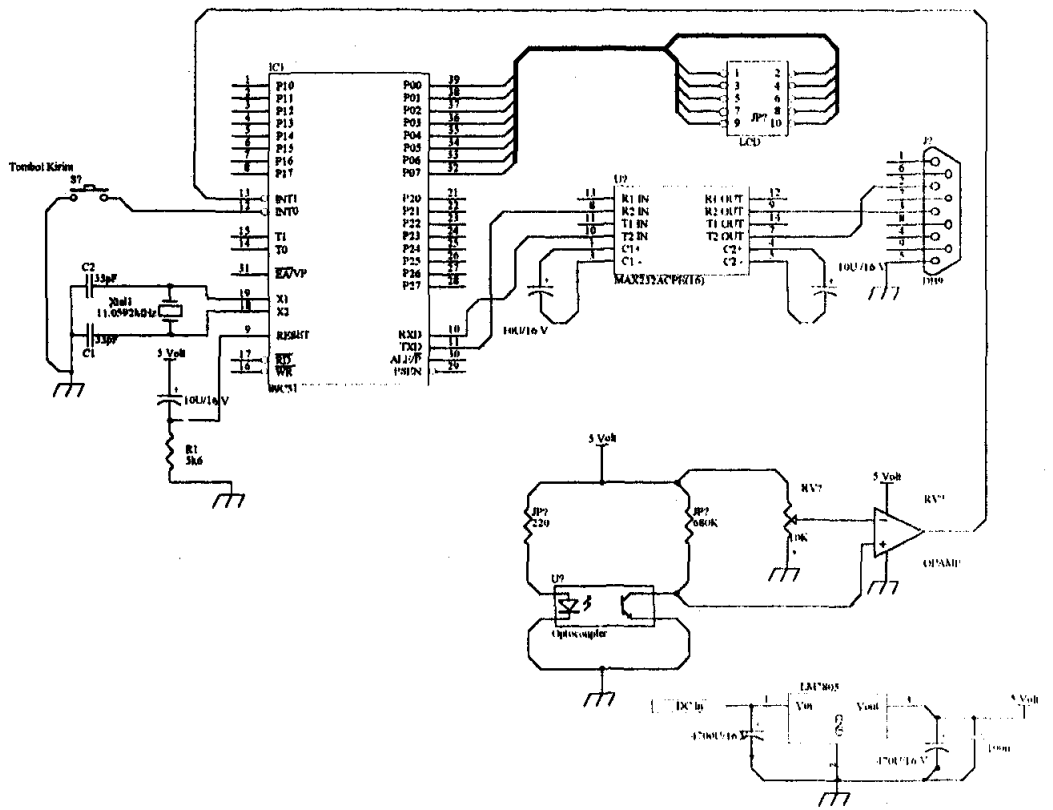
LAMPIRAN



Title		
Size: B	Number:	Revision:
Date: 23-Jan-2002	Sheet of	
File:	Drawn by:	

```
uses dos,crt,GRAPH;
const TX  = $3F8;
      RX  = $3F8;
      LCR = $3FB;
      MSB = $3F9;
      LSB = $3F8;
      IER = $3F9;
      LSR = $3FD;
      MCR = $3FC;
      IIR = $3FA;
      AO0 = $20;
      AO1 = $21;
      Gray50 : FillPatternType = ($AA, $55, $AA,
      $55, $AA, $55, $AA, $55);

var  r:registers;
     rev:pointer;
     TOM:CHAR;
     data_ok,read_ok:boolean;
     n,serial,pointer:byte;
     gd,gm:integer;
     data:array[0..10]of byte;
     temp_meteran,meteran:longint;
     s:string[12];
     pentol:string[9];

PROCEDURE INITSER;
          BEGIN
          PORT[LCR]:=128;
          PORT[MSB]:=0;
          PORT[LSB]:=12;
          PORT[LCR]:=7;
          PORT[IER]:=1;
          PORT[AO1]:=32;
          PORT[LSR]:=0;
          PORT[MCR]:=$F;
          END;

FUNCTION DATA_IN:BOOLEAN;
         BEGIN
          IF PORT[IIR]=4 THEN DATA_IN:=TRUE ELSE DATA_IN:=FALSE;
          END;
FUNCTION TX_KOSONG:BOOLEAN;
         BEGIN
         IF PORT[LSR]=96 THEN TX_KOSONG:= TRUE ELSE TX_KOSONG:=FA
LSE;
         END;

function IntToStr(I:longint):string;
var
```

```
 S: string[11];
begin
Str(I,S);
IntToStr :=S;
end;

PROCEDURE SEND(DATA:BYTE);
          BEGIN
          IF TX_KOSONG THEN PORT[TX]:=DATA;
          delay(10);
          END;

PROCEDURE RECEIVER;INTERRUPT;
          BEGIN
          IF DATA_IN THEN
             BEGIN
             if not(read_Ok) then
                begin
                serial:=PORT[RX];
                data[pointer]:=serial;
                inc(pointer);
                if pointer=7 then
                   begin
                   meteran:=data[3]+256*data[4]+65536*data[5]+167
77216*data[6];
                   meteran:=meteran div 36;
                   read_ok:=true;
                   end;
                end;
             END;
          PORT[AOO]:=$20;
          END;

BEGIN
Gd := Detect;
InitGraph(Gd, Gm, ' ');
if GraphReSult <> grOk then Halt(1);
clrscr;
getintvec($c,rev);
setintvec($c,@receiver);
initser;
repeat
if read_ok then
   begin
   cleardevice;
   setbkcolor(black);
   SetTextStyle(1,0,7);
   setcolor(white);
   outtextxy(120,90,'Pemakaian :');
   SetFillPattern(Gray50,blue);
```

```
   bar(20,170,600,300);
   s:='0000,0000M';
   temp_meteran:=meteran;
   for n:=9 downto 1 do
       begin
       if n<>5 then
          begin
          pentol:=inttostr(temp_meteran mod 10);
          s[n]:=pentol[1];
          temp_meteran:=temp_meteran div 10;
          end;
       end;
   SetTextStyle(1,0,7);
   setcolor(yellow);
   outtextxy(90,170,s);
   SetTextStyle(1,0,5);
   setcolor(yellow);
   outtextxy(530,160,'3');
   pointer:=0;
   read_ok:=false;
   end;
if keypressed then tom:=readkey;
until tom=#27;
setintvec($c,rev);
closegraph;
end.
```

```
COUNT           EQU     08H
TEMP1           EQU     09H
TEMP2           EQU     0AH
TEMP3           EQU     0BH
TEMP4           EQU     0CH
IN1             EQU     0DH
IN2             EQU     0EH
IN3             EQU     0FH
IN4             EQU     10H
VAR6            EQU     11H             ;VARIABEL 64 BIT
VAR7            EQU     12H
VAR8            EQU     13H
VAR9            EQU     14H
VAR10           EQU     15H
VAR11           EQU     16H
VAR12           EQU     17H             ;MSB 64 BIT
VAR1            EQU     18H             ;LSB 32 BIT
VAR2            EQU     19H
VAR3            EQU     1AH
VAR4            EQU     1BH             ;MSB 32 BIT
FREE            EQU     1CH
SELECT          EQU     1DH
VAR5            DATA    21H             ;LSB 64 BIT
VOLUME          EQU     30H             ;4 BYTES
DETIK           EQU     34H
MENIT           EQU     35H
JAM             EQU     36H
DAY             EQU     37H
VOLUME_DISP     EQU     38H             ; 4 BYTES
prescaler       EQU     3ch             ; 4 bytes
lcd_buff_ln1    EQU     40H             ;16 BYTES
lcd_buff_ln2    EQU     50H             ;16 BYTES
PRESS           BIT     0
UPDATE          BIT     1
BLANK           BIT     2
CLOCK           BIT     3
STAT_BLINK      BIT     4

                ORG     00H
                AJMP    MULAI

                ORG     0BH
                AJMP    TMR0

                ORG     13H
                AJMP    INT1

                ORG     30H
;-------------------------------
;               TIMER0
```

```
;--------------------------------
tmr0            djnz    prescaler,esc_tmr0
                mov     prescaler,#30
                djnz    prescaler+1,esc_tmr0
                mov     prescaler+1,#20
                djnz    prescaler+2,esc_tmr0
                mov     prescaler+2,#3
                cpl     stat_blink
                jb      stat_blink,esc_tmr0
                setb    clock
esc_tmr0        reti

;--------------------------------
;          PULSA OPTO
;--------------------------------
INT1            PUSH    A
                INC     VOLUME
                MOV     A,VOLUME
                JNZ     RUTIN_UPDATE
                INC     VOLUME+1
                MOV     A,VOLUME+1
                JNZ     RUTIN_UPDATE
                INC     VOLUME+2
                MOV     A,VOLUME+2
                JNZ     RUTIN_UPDATE
                INC     VOLUME+3
RUTIN_UPDATE    JB      UPDATE,ESC_INT1
                MOV     VOLUME_DISP,VOLUME
                MOV     VOLUME_DISP+1,VOLUME+1
                MOV     VOLUME_DISP+2,VOLUME+2
                MOV     VOLUME_DISP+3,VOLUME+3
                SETB    UPDATE
ESC_INT1        POP     A
                RETI

;-------------------
;    DELAY 4 mS
;-------------------
delay4m         mov     r7,#50
del4m           mov     r6,#250
                djnz    r6,$
                djnz    r7,del4m
                ret

;-------------------
;   delay data lcd
;-------------------
del_lcd         mov     a,#200
                djnz    a,$
                ret
```

```
;--------------------
;    enable pulse
;--------------------
enable          anl     a,#0fh
                anl     p0,#0f0h
                orl     p0,a
                clr     p0.5
                setb    p0.5
                clr     p0.5
                mov     a,#10
                djnz    a,$
                ret

;--------------------
;    CONTROL LCD
;--------------------
lcdcontrol      mov     free,a
                swap    a
                acall   enable
                mov     a,free
                acall   enable
                acall   del_lcd
                ret

;---------------------
;  inisialisasi lcd
;---------------------
initlcd4bit     clr     p0.4
                mov     r5,#10
wait_lcd        mov     a,#3
                acall   enable
                acall   delay4m
                djnz    r5,wait_lcd

WAITFUNCT       mov     a,#2
                acall   enable
                acall   delay4m

                mov     a,#2fh          ;FUNCTIONSET
                acall   lcdcontrol
                mov     a,#0ch          ;DISPLAY ON
                acall   lcdcontrol
                mov     a,#01h          ;DISPLAY CLEAR
                acall   lcdcontrol
                mov     a,#06h          ;ENTRY
                acall   lcdcontrol
                ret

;------------------------------
```

```
;           DISPLAY LCD
;--------------------------------
lcd             setb    p0.4
                mov     free,a
                swap    a
                acall   enable
                acall   del_lcd
                mov     a,free
                acall   enable
                clr     p0.4
                ret

;-----------------------------------
;              PEMBAGIAN
;-----------------------------------
BAGI            MOV     A,R0
                PUSH    A
                MOV     A,R1
                PUSH    A
                MOV     A,R2
                PUSH    A
                MOV     IN1,VAR1
                MOV     IN2,VAR2
                MOV     IN3,VAR3
                MOV     IN4,VAR4
                MOV     VAR1,#0
                MOV     VAR2,#0
                MOV     VAR3,#0
                MOV     VAR4,#0
                MOV     COUNT,#64

BAGI1           CLR     C
                MOV     A,VAR5          ;GESER LSB 64 BIT
                RLC     A
                MOV     VAR5,A
                MOV     R0,#11H         ;ALAMAT VAR6
                MOV     R2,#11
SHIFT           MOV     A,@R0           ;GESER KIRI
                RLC     A
                MOV     @R0,A
                INC     R0
                DJNZ    R2,SHIFT
                MOV     TEMP1,VAR1
                MOV     TEMP2,VAR2
                MOV     TEMP3,VAR3
                MOV     TEMP4,VAR4
                CLR     C               ;PENGURANGAN
                MOV     R0,#18H
                MOV     R1,#0DH
                MOV     R2,#4
```

```
KURANG          MOV     A,@R0
                SUBB    A,@R1
                MOV     @R0,A
                INC     R0
                INC     R1
                DJNZ    R2,KURANG
                JC      CLEAR_VARBIT0           ;CEK APAKAH RESULT
 NEGATIVE
                SETB    VAR5.0
                AJMP    CEKCOUNTER

CLEAR_VARBIT0   MOV     VAR1,TEMP1
                MOV     VAR2,TEMP2
                MOV     VAR3,TEMP3
                MOV     VAR4,TEMP4
CEKCOUNTER      DJNZ    COUNT,BAGI1
                POP     A
                MOV     R2,A
                POP     A
                MOV     R1,A
                POP     A
                MOV     R0,A
                RET

;--------------------------------
;            PERKALIAN
;--------------------------------
KALI            MOV     IN1,VAR1
                MOV     IN2,VAR2
                MOV     IN3,VAR3
                MOV     IN4,VAR4
                MOV     VAR9,#0
                MOV     VAR10,#0
                MOV     VAR11,#0
                MOV     VAR12,#0
                MOV     VAR1,#0
                MOV     VAR2,#0
                MOV     VAR3,#0
                MOV     VAR4,#0
                MOV     COUNT,#32

KALI1           CLR     C
                JNB     VAR5.0,PASS2            ;APAKAH Q0 = 0 ?
                MOV     R0,#18H
                MOV     R1,#0DH
                MOV     R2,#4
TAMBAH          MOV     A,@R0
                ADDC    A,@R1
                MOV     @R0,A
                INC     R0
```

```
                INC     R1
                DJNZ    R2,TAMBAH
PASS2           MOV     R0,#1BH                 ;ALAMAT VAR6
                MOV     R2,#4
SHIFTR1         MOV     A,@R0                   ;GESER KANAN
                RRC     A
                MOV     @R0,A
                DEC     R0
                DJNZ    R2,SHIFTR1
                MOV     R0,#13H
                MOV     R2,#3
SHIFTR2         MOV     A,@R0
                RRC     A
                MOV     @R0,A
                DEC     R0
                DJNZ    R2,SHIFTR2
                MOV     A,VAR5                  ;GESER LSB 64 BIT
                RRC     A
                MOV     VAR5,A
                DJNZ    COUNT,KALI1             ;APAKAH COUNTER =
0 ?
                MOV     VAR12,VAR4
                MOV     VAR11,VAR3
                MOV     VAR10,VAR2
                MOV     VAR9,VAR1
                RET

;-------------------------
;PROTOCOL DISPLAY 16 CHAR
;-------------------------
protocol_lcd    mov     r0,a
                mov     free,#16
next_protocol   mov     a,#0
                movc    a,@a+dptr
                inc     dptr
                push    dph
                push    dpl
                push    free
                mov     @r0,a
                inc     r0
                pop     free
                pop     dpl
                pop     dph
                djnz    free,next_protocol
                ret

;--------------------------
;   MAPING MEMORY TO LCD
;--------------------------
map_buff        mov     a,#80h
```

```
                acall   lcdcontrol
                mov     r0,#lcd_buff_ln1
                mov     r7,#16
disp_l1         mov     a,@r0
                acall   lcd
                inc     r0
                djnz    r7,disp_l1

                mov     a,#0c0h
                acall   lcdcontrol
                mov     r0,#lcd_buff_ln2
                mov     r7,#16
disp_l2         mov     a,@r0
                acall   lcd
                inc     r0
                djnz    r7,disp_l2
                ret

;-----------------------
;     delay 1 secon
;-----------------------
delay           mov     a,#7
delay2          mov     r7,#250
delay1          mov     r6,#250
                djnz    r6,$
                djnz    r7,delay1
                djnz    a,delay2
                ret

;-----------------------
;       IDENTITY
;-----------------------
IDENTITY        MOV     DPTR,#NAMA
                MOV     A,#LCD_BUFF_LN1
                ACALL   PROTOCOL_LCD
                MOV     DPTR,#NRP
                MOV     A,#LCD_BUFF_LN2
                ACALL   PROTOCOL_LCD
                ACALL   MAP_BUFF
                ACALL   DELAY
                RET
NAMA            DB      ' GO KIANG DJOEN '
NRP             DB      '   51030960XX   '

;-----------------------
;       BACKGROUND
;-----------------------
BACKGROUND      MOV     DPTR,#BACKGROUND2
                MOV     A,#LCD_BUFF_LN2
                ACALL   PROTOCOL_LCD
```

```
                RET
BACKGROUND2     DB      'TOTAL:      ,     '

;-------------------------
;    ALU ACTIV 4 BYTES
;-------------------------
ACTIV_4BYTE     MOV     VAR9,#0
                MOV     VAR10,#0
                MOV     VAR11,#0
                MOV     VAR12,#0
                RET

;---------------------------
;    DISP BCD METER AIR
;---------------------------
DISP_BCD        MOV     VAR1,#10
                MOV     VAR2,#0
                MOV     VAR3,#0
                MOV     VAR4,#0
                ACALL   BAGI
                MOV     A,VAR1
                ORL     A,#30H
                MOV     @R0,A
                DEC     R0
                DJNZ    R7,DISP_BCD
                RET

;---------------------
;  routine baris 1
;---------------------
baris1          mov     a,detik
                mov     b,#60
                div     ab
                mov     detik,b         ;detik
                add     a,menit         ;menit
                mov     b,#60
                div     ab
                mov     menit,b
                add     a,jam           ;jam
                mov     b,#24
                div     ab
                mov     jam,b
                add     a,day           ;hari
                mov     b,#7
                div     ab
                mov     day,b

                mov     r0,#jam                 ;load jam to buffe
r lcd
                mov     r1,#lcd_buff_ln1+8
```

```
                mov     r7,#3
bcd_adjust      mov     a,@r0
                mov     b,#10
                div     ab
                orl     a,#30h
                orl     b,#30h
                mov     @r1,a
                inc     r1
                mov     @r1,b
                inc     r1
                inc     r1
                dec     r0
                djnz    r7,bcd_adjust
                mov     lcd_buff_ln1+8+2,#3ah
                mov     lcd_buff_ln1+8+5,#3ah

                mov     dptr,#hari              ;load day to buffe
r lcd
                mov     a,day
                mov     b,#6
                mul     ab
                add     a,dpl
                mov     dpl,a
                mov     a,#0
                addc    a,dph
                mov     dph,a
                mov     r0,#lcd_buff_ln1
                mov     r7,#6
get_char_hari   mov     a,#0
                movc    a,@a+dptr
                mov     @r0,a
                inc     dptr
                inc     r0
                djnz    r7,get_char_hari
                inc     detik
                ret

hari            db      'Senin   '
                db      'Selasa  '
                db      'Rabu    '
                db      'Kamis   '
                db      'Jumat   '
                db      'Sabtu   '
                db      'Minggu  '

;---------------------
;     MAIN PROGRAM
;---------------------
MULAI           MOV     SP,#60H
                ACALL   INITLCD4BIT
```

```
                ACALL   IDENTITY
                CLR     PRESS
                MOV     R0,#VOLUME
                MOV     R7,#11
RESET_VALUE     MOV     @R0,#0
                INC     R0
                DJNZ    R7,RESET_VALUE

                MOV     R0,#VOLUME_disp
                MOV     R7,#4
RESET_Volume    MOV     @R0,#0
                INC     R0
                DJNZ    R7,RESET_volume
                mov     prescaler+2,#3
                MOV     DETIK,#0
                MOV     MENIT,#48
                MOV     JAM,#10
                mov     select,#0
                MOV     TMOD,#22H
                MOV     SCON,#50H
                MOV     PCON,#80H
                MOV     TL1,#0FAH
                MOV     TH1,#0FAH
                SETB    TR1
                MOV     TL0,#64
                MOV     TH0,#64
                SETB    TR0
                SETB    IT1
                MOV     IE,#86H          ;ACTIF INT1 & TMR0
                SETB    UPDATE

DISP_METER_AIR  JNB     UPDATE,RUTIN_JAM
                acall   background
                MOV     VAR5,VOLUME_DISP
                MOV     VAR6,VOLUME_DISP+1
                MOV     VAR7,VOLUME_DISP+2
                MOV     VAR8,VOLUME_DISP+3
                ACALL   ACTIV_4BYTE
                MOV     VAR1,#36
                MOV     VAR2,#0
                MOV     VAR3,#0
                MOV     VAR4,#0
                ACALL   BAGI
                MOV     R0,#LCD_BUFF_LN2+15
                MOV     R7,#4
                ACALL   DISP_BCD
                MOV     R0,#LCD_BUFF_LN2+10
                MOV     R7,#5
                ACALL   DISP_BCD
                JB      P1.0,esc_disp_volume
```

```
                mov     r0,#volume_disp
                mov     r7,#4
next_tx         mov     a,@r0
                mov     sbuf,a
                jnb     ti,$
                clr     ti
                inc     r0
                djnz    r7,next_tx
esc_disp_volume clr     update

RUTIN_JAM       jb      p0.6,cek_keyset
                jb      press,rutinCLOCK
                setb    press
                inc     select
                mov     a,select
                cjne    a,#5,rutinCLOCK
                mov     select,#0
                sjmp    rutinCLOCK

cek_keyset      jb      p0.7,no_keypress
                jb      press,rutinCLOCK
                setb    press
                mov     a,select
                jz      rutinCLOCK
                cjne    a,#1,set_mnt_jam_day    ;if set detik then
 detik=reset
                mov     detik,#0
                sjmp    rutinCLOCK
set_mnt_jam_day add     a,#detik-1
                mov     r0,a
                inc     @r0
                sjmp    rutinCLOCK

no_keypress     clr     press

rutinCLOCK      jnb     clock,blink
                acall   baris1
                clr     clock
                ajmp    display

blink           jnb     stat_blink,no_display
                mov     a,select
                cjne    a,#1,blink_mnt
                mov     lcd_buff_ln1+14,#20h
                mov     lcd_buff_ln1+15,#20h
blink_mnt       cjne    a,#2,blink_detik
                mov     lcd_buff_ln1+11,#20h
                mov     lcd_buff_ln1+12,#20h
blink_detik     cjne    a,#3,blink_day
                mov     lcd_buff_ln1+8,#20h
```

```
                mov     lcd_buff_ln1+9,#20h
blink_day       cjne    a,#4,display
                mov     lcd_buff_ln1+0,#20h
                mov     lcd_buff_ln1+1,#20h
                mov     lcd_buff_ln1+2,#20h
                mov     lcd_buff_ln1+3,#20h
                mov     lcd_buff_ln1+4,#20h
                mov     lcd_buff_ln1+5,#20h
display         acall   map_buff
no_display      ajmp    DISP_METER_AIR
```

eatures

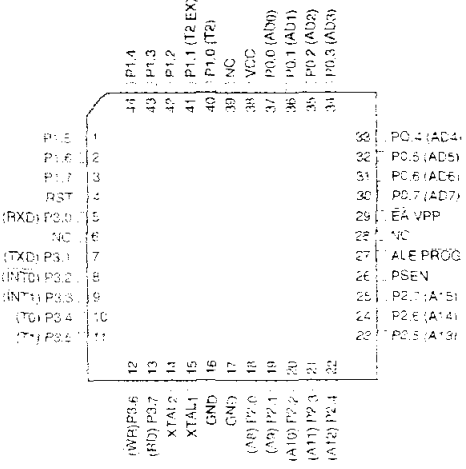
- Compatible with MCS-51™ Products
- 4K Bytes of In-System Reprogrammable Flash Memory
  - Endurance: 1,000 Write/Erase Cycles
- Fully Static Operation: 0 Hz to 24 MHz
- *Three-level Program Memory Lock*
- 128 x 8-bit Internal RAM
- 32 Programmable I/O Lines
- Two 16-bit Timer/Counters
- Six Interrupt Sources
- *Programmable Serial Channel*
- Low-power Idle and Power-down Modes

escription

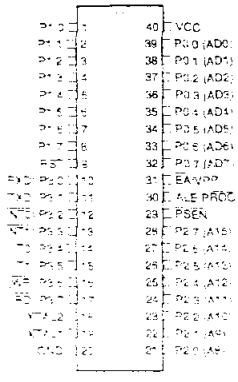
he AT89C51 is a low-power, high-performance CMOS 8-bit microcomputer with 4K ytes of Flash programmable and erasable read only memory (PEROM). The device manufactured using Atmel's high-density nonvolatile memory technology and is *ompatible with the industry-standard MCS-51 instruction set and pinout. The on-chip* lash allows the program memory to be reprogrammed in-system or by a conven- onal nonvolatile memory programmer. By combining a versatile 8-bit CPU with Flash n a monolithic chip, the Atmel AT89C51 is a powerful microcomputer which provides highly-flexible and cost-effective solution to many embedded control applications.

in Configurations

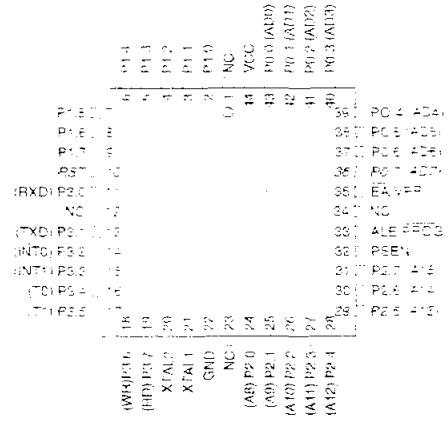
PQFP/TQFP



PDIP



PLCC

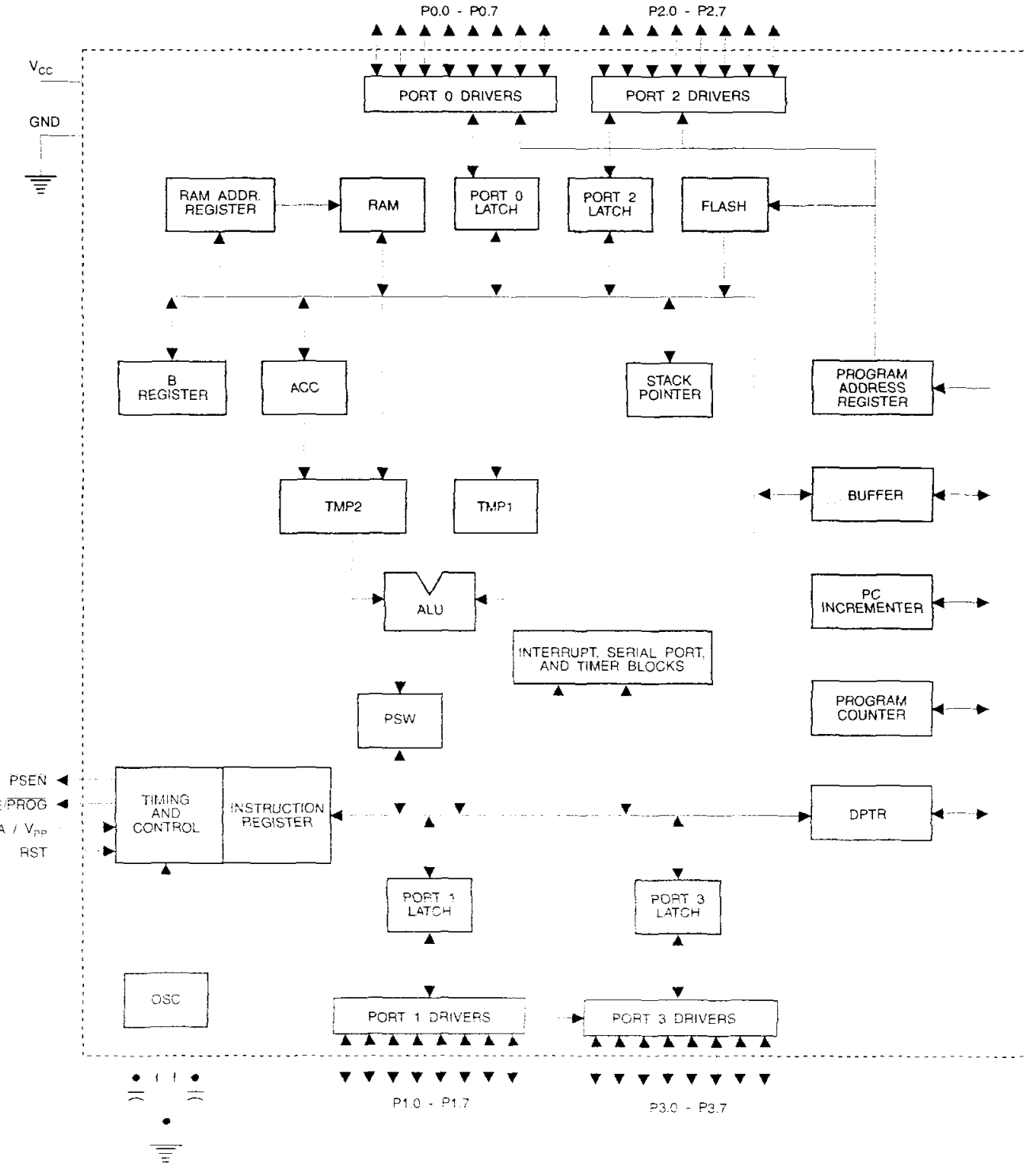


8-bit Microcontroller with 4K Bytes Flash

AT89C51

Rev. 0265G–02/00

ock Diagram


P0.0 - P0.7
P2.0 - P2.7
V_{CC}
GND
PORT 0 DRIVERS
PORT 2 DRIVERS
RAM ADDR. REGISTER
RAM
PORT 0 LATCH
PORT 2 LATCH
FLASH
B REGISTER
ACC
STACK POINTER
PROGRAM ADDRESS REGISTER
TMP2
TMP1
BUFFER
ALU
PC INCREMENTER
INTERRUPT, SERIAL PORT, AND TIMER BLOCKS
PSW
PROGRAM COUNTER
PSEN
PROG
/ V_{PP}
RST
TIMING AND CONTROL
INSTRUCTION REGISTER
DPTR
PORT 1 LATCH
PORT 3 LATCH
OSC
PORT 1 DRIVERS
PORT 3 DRIVERS
P1.0 - P1.7
P3.0 - P3.7

T89C51 provides the following standard features: 4K of Flash, 128 bytes of RAM, 32 I/O lines, two 16-bit counters, a five vector two-level interrupt architecture, duplex serial port, on-chip oscillator and clock cir- In addition, the AT89C51 is designed with static logic eration down to zero frequency and supports two are selectable power saving modes. The Idle Mode the CPU while allowing the RAM, timer/counters, port and interrupt system to continue functioning. The r-down Mode saves the RAM contents but freezes cillator disabling all other chip functions until the next are reset.

Description

y voltage.

d.

is an 8-bit open-drain bi-directional I/O port. As an t port, each pin can sink eight TTL inputs. When 1s ritten to port 0 pins, the pins can be used as high- ance inputs.

may also be configured to be the multiplexed low- address/data bus during accesses to external pro- and data memory. In this mode P0 has internal s.

also receives the code bytes during Flash program- , and outputs the code bytes during program ation. *External pullups are required during program* ation.

is an 8-bit bi-directional I/O port with internal pullups. ort 1 output buffers can sink/source four TTL inputs. 1s are written to Port 1 pins they are pulled high by ernal pullups and can be used as inputs. As inputs. pins that are externally being pulled low will source t (I_{IL}) because of the internal pullups.

also receives the low-order address bytes during programming and verification.

is an 8-bit bi-directional I/O port with internal pullups. ort 2 output buffers can sink/source four TTL inputs. 1s are written to Port 2 pins they are pulled high by ernal pullups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL}) because of the internal pullups.

Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application, it uses strong internal pullups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

Port 3

Port 3 is an 8-bit bi-directional I/O port with internal pullups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}) because of the pullups.

Port 3 also serves the functions of various special features of the AT89C51 as listed below:

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

Port 3 also receives some control signals for Flash programming and verification.

RST

Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device.

ALE/$\overline{PROG}$

Address Latch Enable output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input ($\overline{PROG}$) during Flash programming.

In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that one ALE

is skipped during each access to external Data
ory.

ired, ALE operation can be disabled by setting bit 0 of
ocation 8EH. With the bit set, ALE is active only dur-
MOVX or MOVC instruction. Otherwise, the pin is
ly pulled high. Setting the ALE-disable bit has no
if the microcontroller is in external execution mode.

am Store Enable is the read strobe to external pro-
memory.

the AT89C51 is executing code from external pro-
memory, $\overline{PSEN}$ is activated twice each machine
except that two $\overline{PSEN}$ activations are skipped during
access to external data memory.

PP

nal Access Enable. $\overline{EA}$ must be strapped to GND in
to enable the device to fetch code from external pro-
memory locations starting at 0000H up to FFFFH.
however, that if lock bit 1 is programmed, $\overline{EA}$ will be
ally latched on reset.

hould be strapped to V_{CC} for internal program
tions.

in also receives the 12-volt programming enable volt-
V_{PP}) during Flash programming, for parts that require
lt V_{PP}.

1

to the inverting oscillator amplifier and input to the
al clock operating circuit.

2

lt from the inverting oscillator amplifier.

illator Characteristics

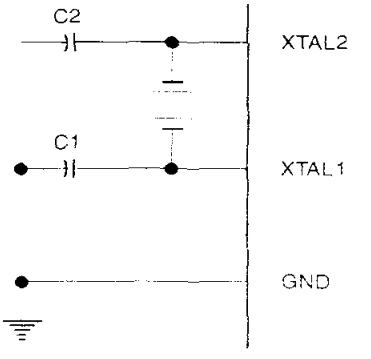
1 and XTAL2 are the input and output, respectively,
nverting amplifier which can be configured for use as
-chip oscillator, as shown in Figure 1. Either a quartz
il or ceramic resonator may be used. To drive the
from an external clock source, XTAL2 should be left
unconnected while XTAL1 is driven as shown in Figure 2. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

Idle Mode

In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special functions registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

It should be noted that when idle is terminated by a hard ware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.

Figure 1. Oscillator Connections

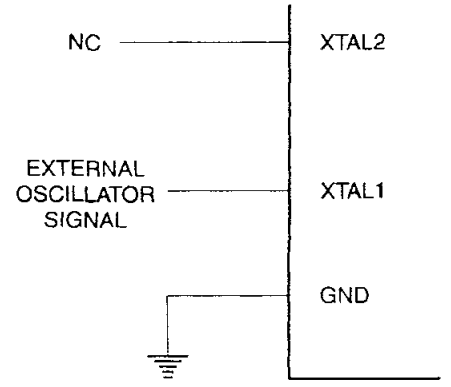


Note: C1, C2 = 30 pF ± 10 pF for Crystals
= 40 pF ± 10 pF for Ceramic Resonators

us of External Pins During Idle and Power-down Modes

	Program Memory	ALE	$\overline{PSEN}$	PORT0	PORT1	PORT2	PORT3
	Internal	1	1	Data	Data	Data	Data
	External	1	1	Float	Data	Address	Data
r-down	Internal	0	0	Data	Data	Data	Data
r-down	*External*	*0*	*0*	*Float*	*Data*	*Data*	*Data*

e 2. External Clock Drive Configuration



ver-down Mode

power-down mode, the oscillator is stopped, and the ction that invokes power-down is the last instruction ited. The on-chip RAM and Special Function Registers retain their values until the power-down mode is terminated. The only exit from power-down is a hardware reset. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

Program Memory Lock Bits

On the chip are three lock bits which can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in the table below.

When lock bit 1 is programmed, the logic level at the $\overline{EA}$ pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value, and holds that value until reset is activated. It is necessary that the latched value of $\overline{EA}$ be in agreement with the current logic level at that pin in order for the device to function properly.

k Bit Protection Modes

	Program Lock Bits			
	LB1	LB2	LB3	Protection Type
1	U	U	U	No program lock features
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, $\overline{EA}$ is sampled and latched on reset, and further programming of the Flash is disabled
3	P	P	U	Same as mode 2, also verify is disabled
4	P	P	P	Same as mode 3, also external execution is disabled

gramming the Flash

T89C51 is normally shipped with the on-chip Flash ry array in the erased state (that is, contents = FFH) eady to be programmed. The programming interface ts either a high-voltage (12-volt) or a low-voltage program enable signal. The low-voltage program- mode provides a convenient way to program the C51 inside the user's system, while the high-voltage amming mode is compatible with conventional third- Flash or EPROM programmers.

T89C51 is shipped with either the high-voltage or oltage programming mode enabled. The respective de marking and device signature codes are listed in lowing table.

	V_{PP} = 12V	V_{PP} = 5V
Side Mark	AT89C51 xxxx yyww	AT89C51 xxxx-5 yyww
ature	(030H) = 1EH (031H) = 51H (032H) =F FH	(030H) = 1EH (031H) = 51H (032H) = 05H

T89C51 code memory array is programmed byte-by- n either programming mode. *To program any non- byte in the on-chip Flash Memory, the entire memory be erased using the Chip Erase Mode.*

ramming Algorithm: Before programming the C51, the address, data and control signals should be according to the Flash programming mode table and e 3 and Figure 4. To program the AT89C51, take the ng steps.

put the desired memory location on the address es.

put the appropriate data byte on the data lines.

ctivate the correct combination of control signals.

aise $\overline{EA}/V_{PP}$ to 12V for the high-voltage program- ing mode.

ulse ALE/$\overline{PROG}$ once to program a byte in the ash array or the lock bits. The byte-write cycle is lf-timed and typically takes no more than 1.5 ms. epeat steps 1 through 5, changing the address and data for the entire array or until the end of the object file is reached.

Data Polling: The AT89C51 features Data Polling to indicate the end of a write cycle. During a write cycle, an attempted read of the last byte written will result in the complement of the written datum on PO.7. Once the write cycle has been completed, true data are valid on all outputs, and the next cycle may begin. Data Polling may begin any time after a write cycle has been initiated.

Ready/Busy: The progress of byte programming can also be monitored by the RDY/$\overline{BSY}$ output signal. P3.4 is pulled low after ALE goes high during programming to indicate BUSY. P3.4 is pulled high again when programming is done to indicate READY.

Program Verify: If lock bits LB1 and LB2 have not been programmed, the programmed code data can be read back via the address and data lines for verification. The lock bits cannot be verified directly. Verification of the lock bits is achieved by observing that their features are enabled.

Chip Erase: The entire Flash array is erased electrically by using the proper combination of control signals and by holding ALE/$\overline{PROG}$ low for 10 ms. The code array is written with all "1"s. *The chip erase operation must be executed* before the code memory can be re-programmed.

Reading the Signature Bytes: The signature bytes are read by the same procedure as a normal verification of locations 030H, 031H, and 032H, except that P3.6 and P3.7 must be pulled to a logic low. The values returned are as follows.

(030H) = 1EH indicates manufactured by Atmel
(031H) = 51H indicates 89C51
(032H) = FFH indicates 12V programming
(032H) = 05H indicates 5V programming

Programming Interface

Every code byte in the Flash array can be written and the entire array can be erased by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

All major programming vendors offer worldwide support for the Atmel microcontroller series. Please contact your local programming vendor for the appropriate software revision.

sh Programming Modes

e		RST	PSEN	ALE/PROG	EA/V_{PP}	P2.6	P2.7	P3.6	P3.7
e Code Data		H	L		H/12V	L	H	H	H
d Code Data		H	L	H	H	L	L	H	H
e Lock	Bit - 1	H	L		H/12V	H	H	H	H
	Bit - 2	H	L		H/12V	H	H	L	L
	Bit - 3	H	L		H/12V	H	L	H	L
Erase		H	L	(1)	H/12V	H	L	L	L
d Signature Byte		H	L	H	H	L	L	L	L

1. Chip Erase requires a 10 ms $\overline{PROG}$ pulse.

e 3. Programming the Flash

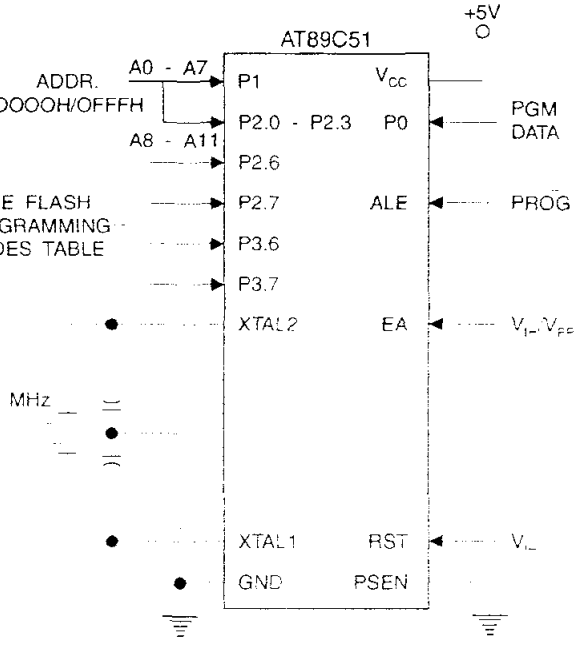
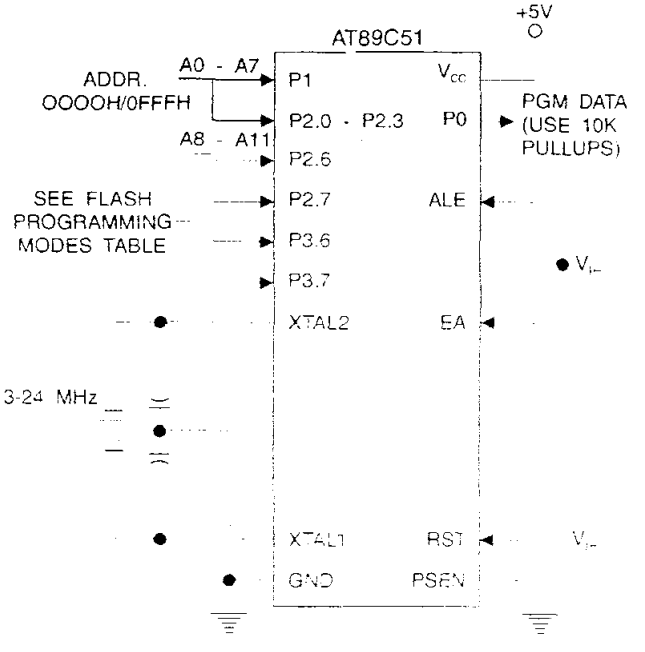
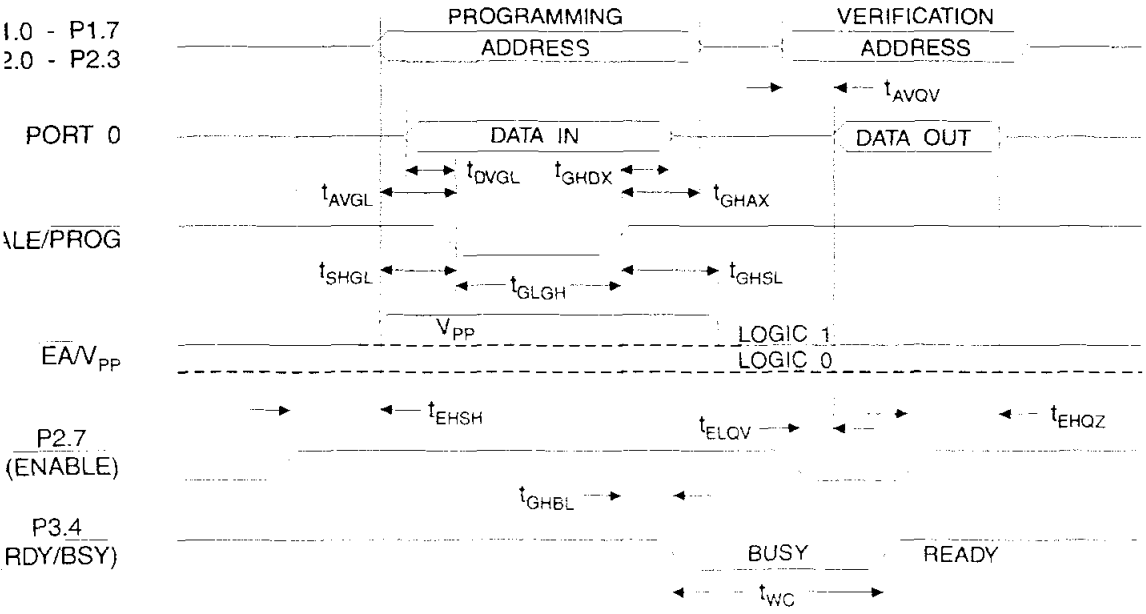


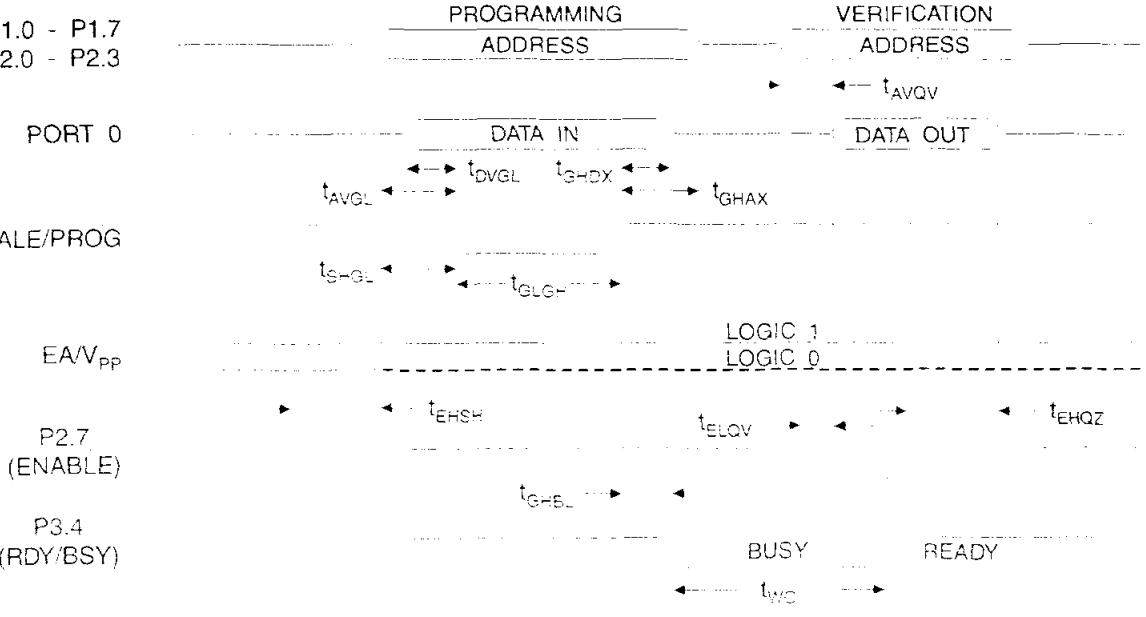
Figure 4. Verifying the Flash



h Programming and Verification Waveforms - High-voltage Mode (V_{PP} = 12V)



sh Programming and Verification Waveforms - Low-voltage Mode (V_{PP} = 5V)



h Programming and Verification Characteristics

°C to 70°C, V_{CC} = 5.0 ± 10%

ol	Parameter	Min	Max	Units
	Programming Enable Voltage	11.5	12.5	V
	Programming Enable Current		1.0	mA
L	Oscillator Frequency	3	24	MHz
	Address Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
	Address Hold After $\overline{PROG}$	$48t_{CLCL}$		
	Data Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
	Data Hold After $\overline{PROG}$	$48t_{CLCL}$		
	P2.7 ($\overline{ENABLE}$) High to V_{PP}	$48t_{CLCL}$		
	V_{PP} Setup to $\overline{PROG}$ Low	10		µs
1)	V_{PP} Hold After $\overline{PROG}$	10		µs
	$\overline{PROG}$ Width	1	110	µs
	Address to Data Valid		$48t_{CLCL}$	
	$\overline{ENABLE}$ Low to Data Valid		$48t_{CLCL}$	
	Data Float After $\overline{ENABLE}$	0	$48t_{CLCL}$	
	$\overline{PROG}$ High to $\overline{BUSY}$ Low		1.0	µs
	Byte Write Cycle Time		2.0	ms

1. Only used in 12-volt programming mode.

solute Maximum Ratings*

rating Temperature	-55°C to +125°C
age Temperature	-65°C to +150°C
age on Any Pin Respect to Ground	-1.0V to +7.0V
imum Operating Voltage	6.6V
Output Current	15.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Characteristics

-40°C to 85°C, V_{CC} = 5.0V ± 20% (unless otherwise noted)

bol	Parameter	Condition	Min	Max	Units
	Input Low-voltage	(Except $\overline{EA}$)	-0.5	0.2 V_{CC} - 0.1	V
	Input Low-voltage ($\overline{EA}$)		-0.5	0.2 V_{CC} - 0.3	V
	Input High-voltage	(Except XTAL1, RST)	0.2 V_{CC} + 0.9	V_{CC} + 0.5	V
	Input High-voltage	(XTAL1, RST)	0.7 V_{CC}	V_{CC} + 0.5	V
	Output Low-voltage[1] (Ports 1,2,3)	I_{OL} = 1.6 mA		0.45	V
	Output Low-voltage[1] (Port 0, ALE, $\overline{PSEN}$)	I_{OL} = 3.2 mA		0.45	V
	Output High-voltage (Ports 1,2,3, ALE, $\overline{PSEN}$)	I_{OH} = -60 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -25 µA	0.75 V_{CC}		V
		I_{OH} = -10 µA	0.9 V_{CC}		V
	Output High-voltage (*Port 0 in External Bus Mode*)	I_{OH} = -800 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -300 µA	0.75 V_{CC}		V
		I_{OH} = -80 µA	0.9 V_{CC}		V
	Logical 0 Input Current (Ports 1,2,3)	V_{IN} = 0.45V		-50	µA
	Logical 1 to 0 Transition Current (Ports 1,2,3)	V_{IN} = 2V, VCC = 5V ± 10%		-650	µA
	Input Leakage Current (Port 0, $\overline{EA}$)	0.45 < V_{IN} < V_{CC}		±10	µA
T	*Reset Pull-down Resistor*		50	300	KΩ
	Pin Capacitance	Test Freq. = 1 MHz, T_A = 25°C		10	pF
	Power Supply Current	Active Mode, 12 MHz		20	mA
		Idle Mode, 12 MHz		5	mA
	Power-down Mode[2]	V_{CC} = 6V		100	µA
		V_{CC} = 3V		40	µA

1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 10 mA
   Maximum I_{OL} per 8-bit port: Port 0: 26 mA
   Ports 1, 2, 3: 15 mA
   Maximum total I_{OL} for all output pins: 71 mA
   If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. *Minimum V_{CC} for Power-down is 2V.*

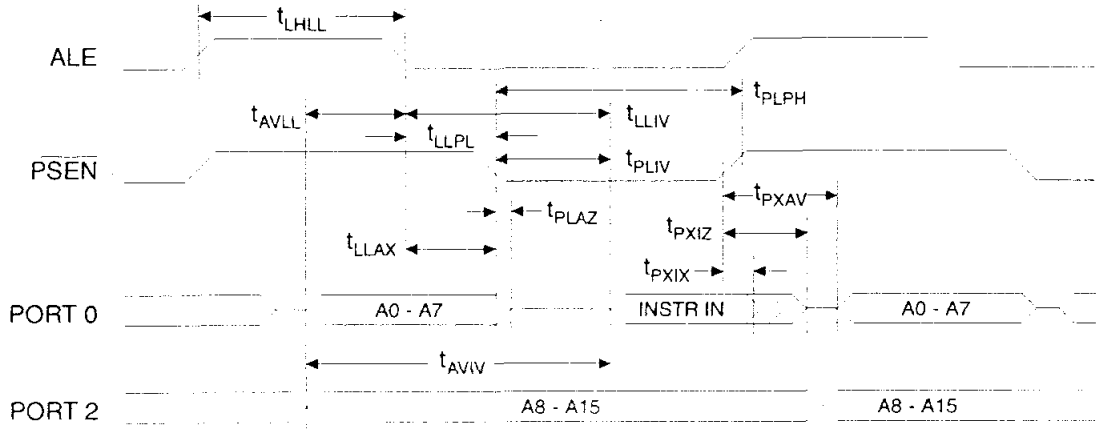
Characteristics

r operating conditions, load capacitance for Port 0, ALE/$\overline{PROG}$, and $\overline{PSEN}$ = 100 pF; load capacitance for all other ts = 80 pF.

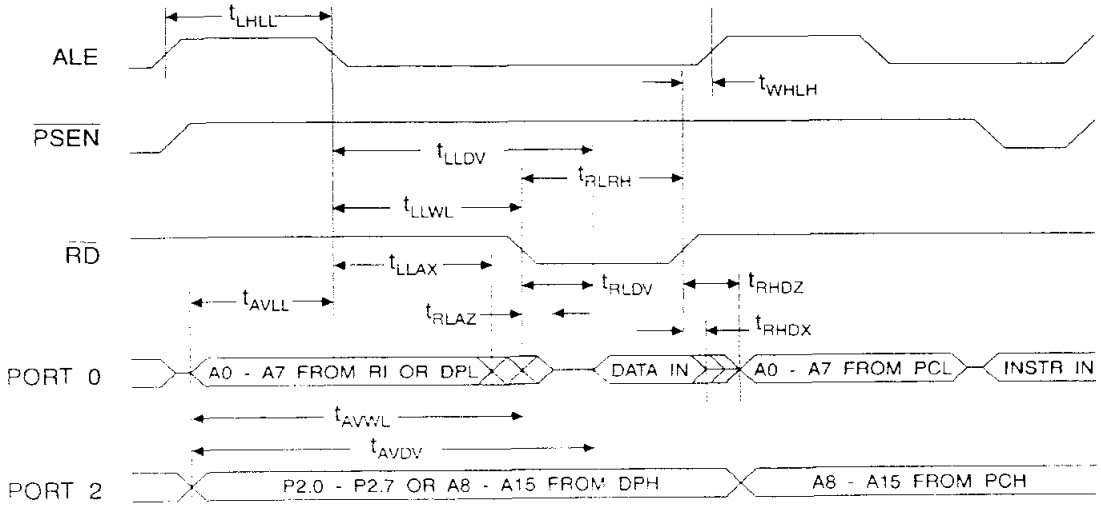
ernal Program and Data Memory Characteristics

bol	Parameter	12 MHz Oscillator		16 to 24 MHz Oscillator		Units
		Min	Max	Min	Max	
CL	Oscillator Frequency			0	24	MHz
	ALE Pulse Width	127		$2t_{CLCL}$-40		ns
	Address Valid to ALE Low	43		t_{CLCL}-13		ns
	Address Hold After ALE Low	48		t_{CLCL}-20		ns
	ALE Low to Valid Instruction In		233		$4t_{CLCL}$-65	ns
	ALE Low to $\overline{PSEN}$ Low	43		t_{CLCL}-13		ns
	$\overline{PSEN}$ Pulse Width	205		$3t_{CLCL}$-20		ns
	$\overline{PSEN}$ Low to Valid Instruction In		145		$3t_{CLCL}$-45	ns
	Input Instruction Hold After $\overline{PSEN}$	0		0		ns
	Input Instruction Float After $\overline{PSEN}$		59		t_{CLCL}-10	ns
	$\overline{PSEN}$ to Address Valid	75		t_{CLCL}-8		ns
	Address to Valid Instruction In		312		$5t_{CLCL}$-55	ns
	$\overline{PSEN}$ Low to Address Float		10		10	ns
	$\overline{RD}$ Pulse Width	400		$6t_{CLCL}$-100		ns
H	$\overline{WR}$ Pulse Width	400		$6t_{CLCL}$-100		ns
	$\overline{RD}$ Low to Valid Data In		252		$5t_{CLCL}$-90	ns
	Data Hold After $\overline{RD}$	0		0		ns
	Data Float After $\overline{RD}$		97		$2t_{CLCL}$-28	ns
	ALE Low to Valid Data In		517		$8t_{CLCL}$-150	ns
	Address to Valid Data In		585		$9t_{CLCL}$-165	ns
	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	200	300	$3t_{CLCL}$-50	$3t_{CLCL}$+50	ns
	Address to $\overline{RD}$ or $\overline{WR}$ Low	203		$4t_{CLCL}$-75		ns
	Data Valid to $\overline{WR}$ Transition	23		t_{CLCL}-20		ns
	Data Valid to $\overline{WR}$ High	433		$7t_{CLCL}$-120		ns
	Data Hold After $\overline{WR}$	33		t_{CLCL}-20		ns
	$\overline{RD}$ Low to Address Float		0		0	ns
	$\overline{RD}$ or $\overline{WR}$ High to ALE High	43	123	t_{CLCL}-20	t_{CLCL}+25	ns

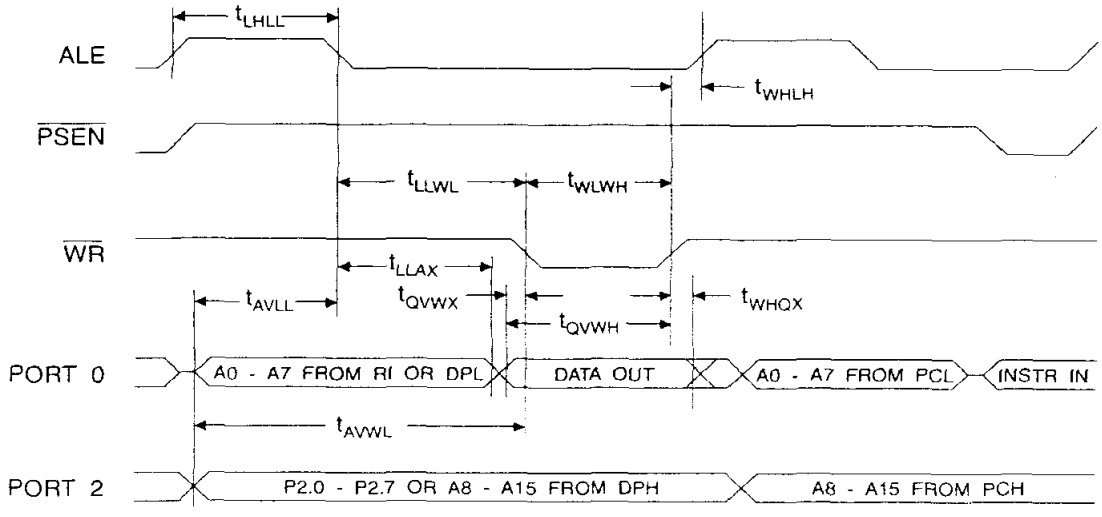
ternal Program Memory Read Cycle



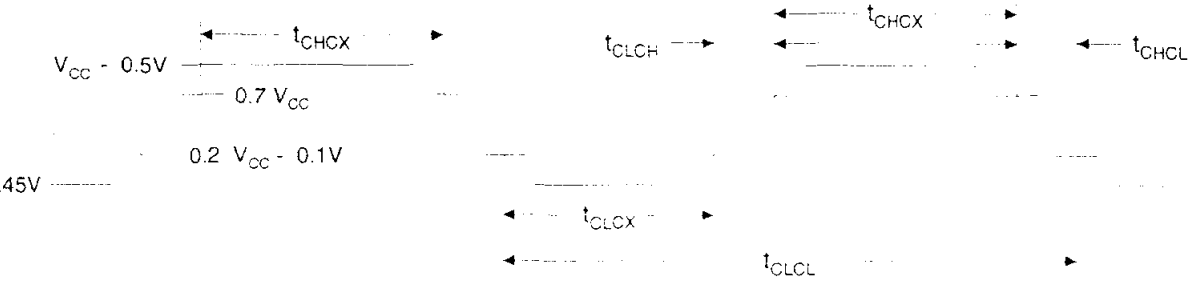
ternal Data Memory Read Cycle



ernal Data Memory Write Cycle



ernal Clock Drive Waveforms



ernal Clock Drive

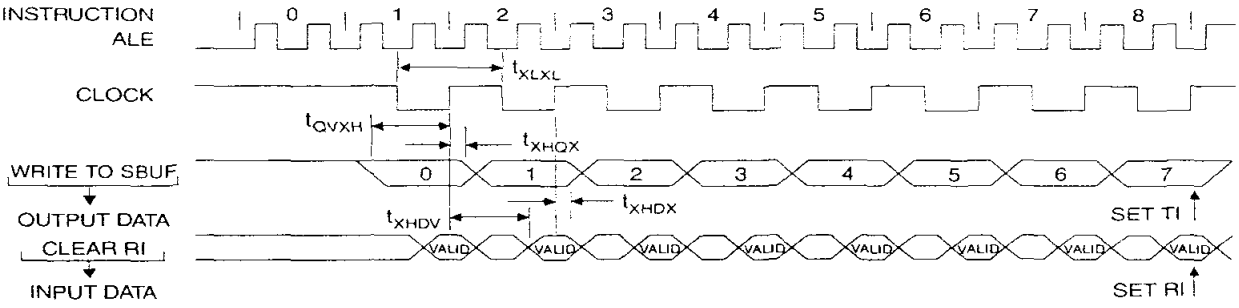
bol	Parameter	Min	Max	Units
CL	Oscillator Frequency	0	24	MHz
	Clock Period	41.6		ns
	High Time	15		ns
	Low Time	15		ns
	Rise Time		20	ns
	Fall Time		20	ns

rial Port Timing: Shift Register Mode Test Conditions

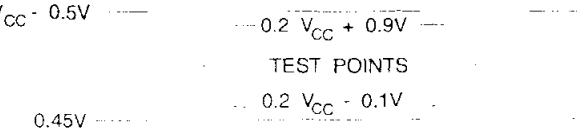
= 5.0 V ± 20%; Load Capacitance = 80 pF)

mbol	Parameter	12 MHz Osc		Variable Oscillator		Units
		Min	Max	Min	Max	
KL	Serial Port Clock Cycle Time	1.0		$12t_{CLCL}$		µs
XH	Output Data Setup to Clock Rising Edge	700		$10t_{CLCL}$-133		ns
QX	Output Data Hold After Clock Rising Edge	50		$2t_{CLCL}$-117		ns
DX	Input Data Hold After Clock Rising Edge	0		0		ns
DV	Clock Rising Edge to Input Data Valid		700		$10t_{CLCL}$-133	ns

ift Register Mode Timing Waveforms

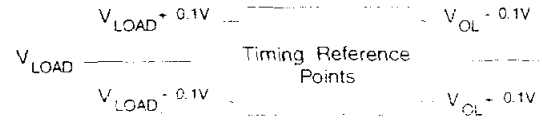


C Testing Input/Output Waveforms[1]



e: 1. AC Inputs during testing are driven at V_{CC} - 0.5V for a logic 1 and 0.45V for a logic 0. Timing measurements are made at V_{IH} min. for a logic 1 and V_{IL} max. for a logic 0.

Float Waveforms[1]



Note: 1. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when 100 mV change from the loaded V_{OH}/V_{OL} level occurs.

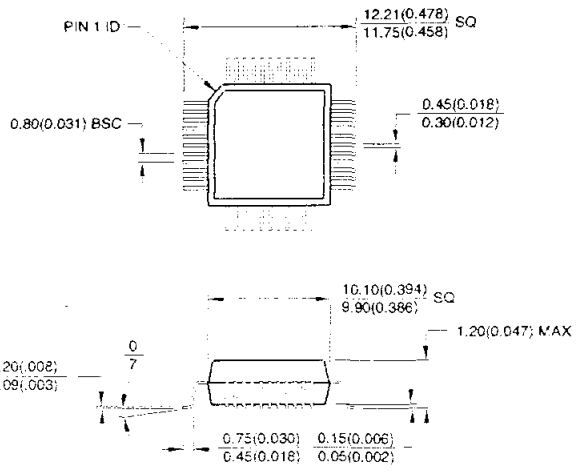
lering Information

peed MHz)	Power Supply	Ordering Code	Package	Operation Range
12	5V ± 20%	AT89C51-12AC	44A	Commercial
		AT89C51-12JC	44J	(0°C to 70°C)
		AT89C51-12PC	40P6	
		AT89C51-12QC	44Q	
		AT89C51-12AI	44A	Industrial
		AT89C51-12JI	44J	(-40°C to 85°C)
		AT89C51-12PI	40P6	
		AT89C51-12QI	44Q	
16	5V ± 20%	AT89C51-16AC	44A	Commercial
		AT89C51-16JC	44J	(0°C to 70°C)
		AT89C51-16PC	40P6	
		AT89C51-16QC	44Q	
		AT89C51-16AI	44A	Industrial
		AT89C51-16JI	44J	(-40°C to 85°C)
		AT89C51-16PI	40P6	
		AT89C51-16QI	44Q	
20	5V ± 20%	AT89C51-20AC	44A	Commercial
		AT89C51-20JC	44J	(0°C to 70°C)
		AT89C51-20PC	40P6	
		AT89C51-20QC	44Q	
		AT89C51-20AI	44A	Industrial
		AT89C51-20JI	44J	(-40°C to 85°C)
		AT89C51-20PI	40P6	
		AT89C51-20QI	44Q	
24	5V ± 20%	AT89C51-24AC	44A	Commercial
		AT89C51-24JC	44J	(0°C to 70°C)
		AT89C51-24PC	40P6	
		AT89C51-24QC	44Q	
		AT89C51-24AI	44A	Industrial
		AT89C51-24JI	44J	(-40°C to 85°C)
		AT89C51-24PI	40P6	
		AT89C51-24QI	44Q	

	Package Type
	44-lead, Thin Plastic Gull Wing Quad Flatpack (TQFP)
	44-lead, Plastic J-leaded Chip Carrier (PLCC)
3	40-lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
	44-lead, Plastic Gull Wing Quad Flatpack (PQFP)

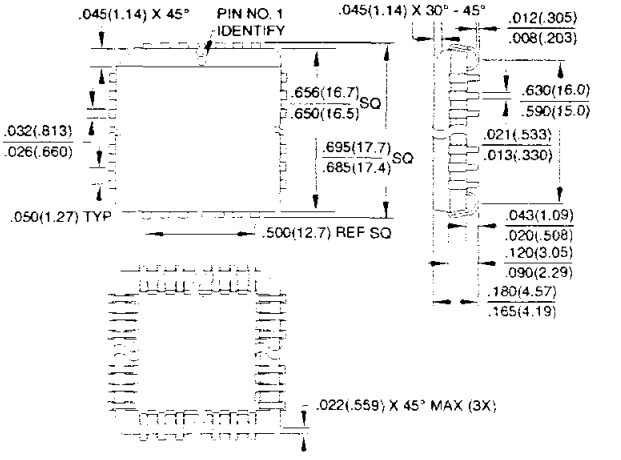
kaging Information

4A, 44-lead, Thin (1.0 mm) Plastic Gull Wing Quad latpack (TQFP)
Dimensions in Millimeters and (Inches)*
EDEC STANDARD MS-026 ACB

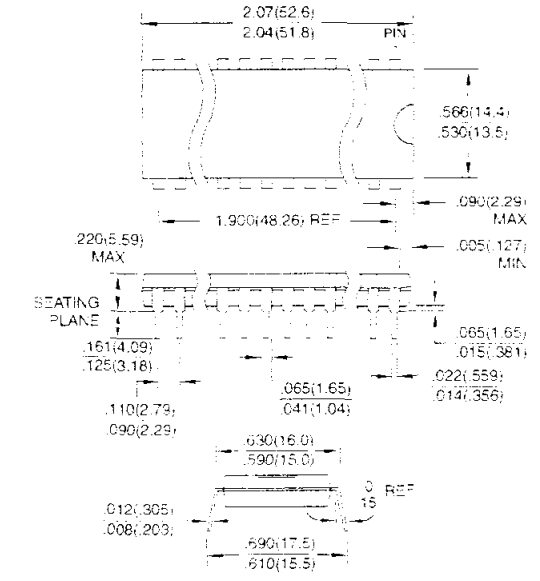


Controlling dimension: millimeters

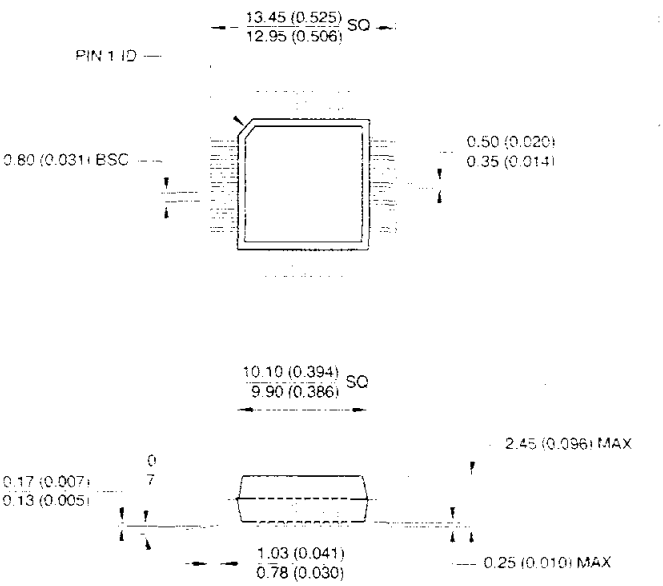
44J, 44-lead, Plastic J-leaded Chip Carrier (PLCC)
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-018 AC



0P6, 40-lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
Dimensions in Inches and (Millimeters)



44Q, 44-lead, Plastic Quad Flat Package (PQFP)
Dimensions in Millimeters and (Inches)*
JEDEC STANDARD MS-022 AB



Controlling dimension: millimeters

tmel Headquarters

rporate Headquarters
2325 Orchard Parkway
San Jose, CA 95131
TEL (408) 441-0311
FAX (408) 487-2600

rope
Atmel U.K., Ltd.
Coliseum Business Centre
Riverside Way
Camberley, Surrey GU15 3YL
England
TEL (44) 1276-686-677
FAX (44) 1276-686-697

ia
Atmel Asia, Ltd.
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimhatsui
East Kowloon
Hong Kong
TEL (852) 2721-9778
FAX (852) 2722-1369

pan
Atmel Japan K.K.
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
TEL (81) 3-3523-3551
FAX (81) 3-3523-7581

Atmel Operations

Atmel Colorado Springs
1150 E. Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
TEL (719) 576-3300
FAX (719) 540-1759

Atmel Rousset
Zone Industrielle
13106 Rousset Cedex
France
TEL (33) 4-4253-6000
FAX (33) 4-4253-6001

Fax-on-Demand
North America:
1-(800) 292-8635
International:
1-(408) 441-0732

e-mail
literature@atmel.com

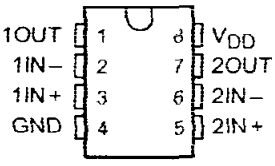
Web Site
http://www.atmel.com

BBS
1-(408) 436-4309

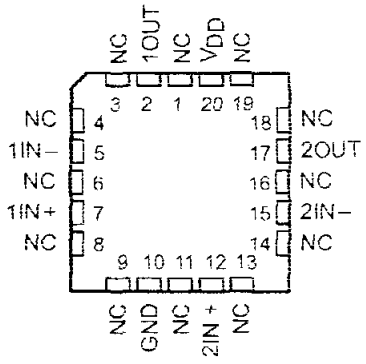
0265G–02/00/xM

- **Trimmed Offset Voltage:**
  TLC277 . . . 500 μV Max at 25°C,
  V_{DD} = 5 V
- **Input Offset Voltage Drift . . . Typically 0.1 μV/Month, Including the First 30 Days**
- **Wide Range of Supply Voltages Over Specified Temperature Range:**
  0°C to 70°C . . . 3 V to 16 V
  –40°C to 85°C . . . 4 V to 16 V
  –55°C to 125°C . . . 4 V to 16 V
- **Single-Supply Operation**
- **Common-Mode Input Voltage Range Extends Below the Negative Rail (C-Suffix, I-Suffix types)**
- **Low Noise . . . Typically 25 nV/√Hz at f = 1 kHz**
- **Output Voltage Range Includes Negative Rail**
- **High Input impedance . . . 10^{12} Ω Typ**
- **ESD-Protection Circuitry**
- **Small-Outline Package Option Also Available in Tape and Reel**
- **Designed-in Latch-Up Immunity**

D, JG, P, OR PW PACKAGE
(TOP VIEW)

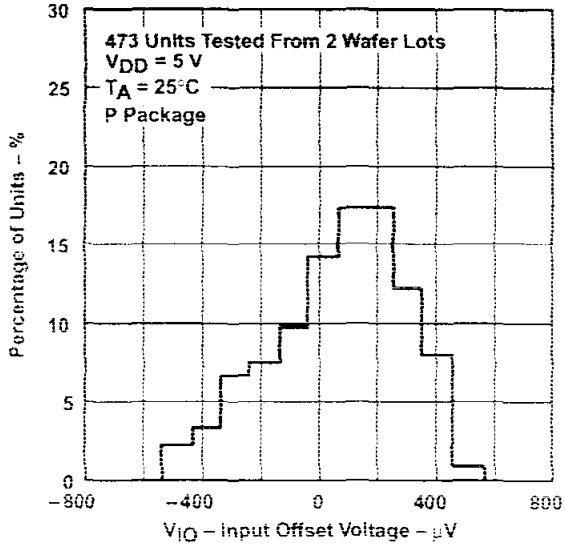


FK PACKAGE
(TOP VIEW)



NC – No internal connection

DISTRIBUTION OF TLC277
INPUT OFFSET VOLTAGE



description

The TLC272 and TLC277 precision dual operational amplifiers combine a wide range of input offset voltage grades with low offset voltage drift, high input impedance, low noise, and speeds approaching those of general-purpose BIFET devices.

These devices use Texas Instruments silicon-gate LinCMOS™ technology, which provides offset voltage stability far exceeding the stability available with conventional metal-gate processes.

The extremely high input impedance, low bias currents, and high slew rates make these cost-effective devices ideal for applications which have previously been reserved for BIFET and NFET products. Four offset voltage grades are available (C-suffix and I-suffix types), ranging from the low-cost TLC272 (10 mV) to the high-precision TLC277 (500 μV). These advantages, in combination with good common-mode rejection and supply voltage rejection, make these devices a good choice for new state-of-the-art designs as well as for upgrading existing designs.

LinCMOS is a trademark of Texas Instruments.

description (continued)

AVAILABLE OPTIONS

T_A	V_{IO}max AT 25°C	PACKAGED DEVICES					CHIP FORM (Y)
		SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)	TSSOP (PW)	
0°C to 70°C	500 µV	TLC277CD	—	—	TLC277CP	—	—
	2 mV	TLC272BCD	—	—	TLC272BCP	—	—
	5 mV	TLC272ACD	—	—	TLC272ACP	—	—
	10mV	TLC272CD	—	—	TLC272CP	TLC272CPW	TLC272Y
–40°C to 85°C	500 µV	TLC277ID	—	—	TLC277IP	—	—
	2 mV	TLC272BID	—	—	TLC272BIP	—	—
	5 mV	TLC272AID	—	—	TLC272AIP	—	—
	10 mV	TLC272ID	—	—	TLC272IP	—	—

The D package is available taped and reeled. Add R suffix to the device type (e.g., TLC277CDR).

In general, many features associated with bipolar technology are available on LinCMOS™ operational amplifiers without the power penalties of bipolar technology. General applications such as transducer interfacing, analog calculations, amplifier blocks, active filters, and signal buffering are easily designed with the TLC272 and TLC277. The devices also exhibit low voltage single-supply operation, making them ideally suited for remote and inaccessible battery-powered applications. The common-mode input voltage range includes the negative rail.

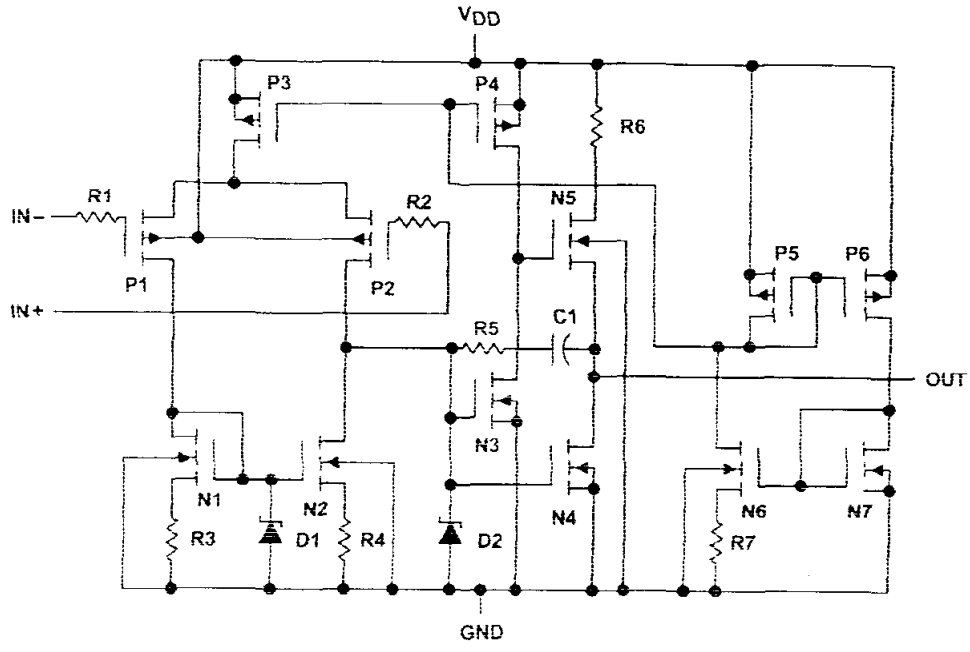
A wide range of packaging options is available, including small-outline and chip carrier versions for high-density system applications.

The device inputs and outputs are designed to withstand –100-mA surge currents without sustaining latch-up.

The TLC272 and TLC277 incorporate internal ESD-protection circuits that prevent functional failures at voltages up to 2000 V as tested under MIL-STD-883C, Method 3015.2; however, care should be exercised in handling these devices as exposure to ESD may result in the degradation of the device parametric performance.

The C-suffix devices are characterized for operation from 0°C to 70°C. The I-suffix devices are characterized for operation from –40°C to 85°C. The M-suffix devices are characterized for operation over the full military temperature range of –55°C to 125°C.

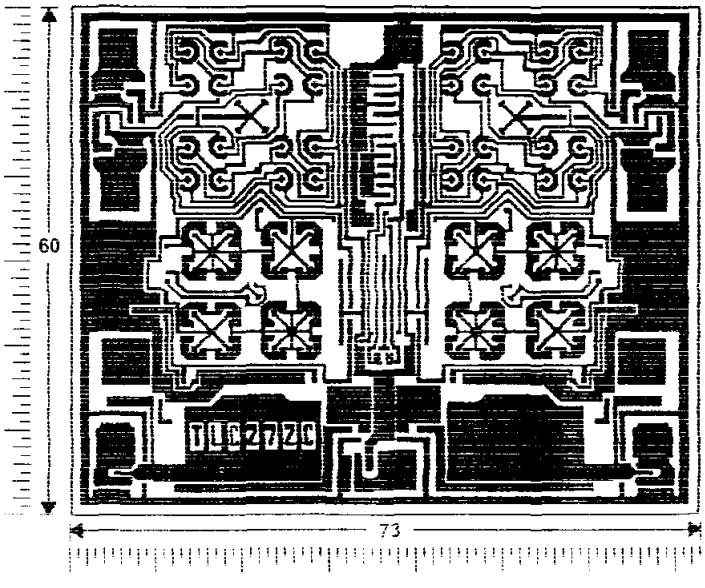
equivalent schematic (each amplifier)

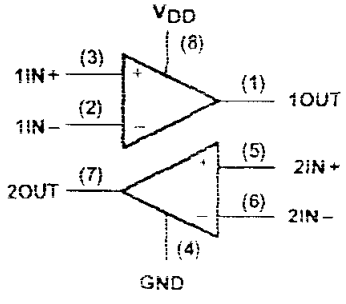


TLC272Y chip information

This chip, when properly assembled, displays characteristics similar to the TLC272C. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

PIN (4) IS INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

bsolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) ..... 18 V
Differential input voltage, V_{ID} (see Note 2) ..... $\pm V_{DD}$
Input voltage range, V_I (any input) ..... −0.3 V to V_{DD}
Input current, I_I ..... ±5 mA
output current, I_O (each output) ..... ±30 mA
Total current into V_{DD} ..... 45 mA
Total current out of GND ..... 45 mA
Duration of short-circuit current at (or below) 25°C (see Note 3) ..... unlimited
Continuous total dissipation ..... See Dissipation Rating Table
Operating free-air temperature, T_A: C suffix ..... 0°C to 70°C
I suffix ..... −40°C to 85°C
M suffix ..... −55°C to 125°C
Storage temperature range ..... −65°C to 150°C
Case temperature for 60 seconds: FK package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: D, P, or PW package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: JG package ..... 300°C

Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and unctional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not mplied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

OTES: 1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at IN+ with respect to IN−.
3. The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded (see application section).

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING	$T_A = 125°C$ POWER RATING
D	725 mW	5.8 mW/°C	464 mW	377 mW	N/A
FK	1375 mW	11 mW/°C	880 mW	715 mW	275 mW
JG	1050 mW	8.4 mW/°C	672 mW	546 mW	210 mW
P	1000 mW	8.0 mW/°C	640 mW	520 mW	N/A
PW	525 mW	4.2 mW/°C	336 mW	N/A	N/A

commended operating conditions

		C SUFFIX		I SUFFIX		M SUFFIX		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
upply voltage, V_{DD}		3	16	4	16	4	16	V
ommon-mode input voltage, V_{IC}	V_{DD} = 5 V	−0.2	3.5	−0.2	3.5	0	3.5	V
	V_{DD} = 10 V	−0.2	8.5	−0.2	8.5	0	8.5	
perating free-air temperature, T_A		0	70	−40	85	−55	125	°C

electrical characteristics at specified free-air temperature, V_{DD} = 5 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	TLC272C, TLC272AC, TLC272BC, TLC277C			UNIT
						MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC272C	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 10 kΩ	25°C		1.1	10	mV
					Full range			12	
		TLC272AC	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 10 kΩ	25°C		0.9	5	
					Full range			6.5	
		TLC272BC	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 10 kΩ	25°C		230	2000	µV
					Full range			3000	
		TLC277C	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 10 kΩ	25°C		200	500	
					Full range			1500	
α_{VIO}	Temperature coefficient of input offset voltage				25°C to 70°C		1.8		µV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 2.5 V,	V_{IC} = 2.5 V	25°C		0.1	60	pA
					70°C		7	300	
I_{IB}	Input bias current (see Note 4)				25°C		0.6	60	pA
					70°C		40	600	
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	−0.2 to 4	−0.3 to 4.2		V
					Full range	−0.2 to 3.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 10 kΩ	25°C	3.2	3.8		V
					0°C	3	3.8		
					70°C	3	3.8		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					0°C		0	50	
					70°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 0.25 V to 2 V,	R_L = 10 kΩ	25°C	5	23		V/mV
					0°C	4	27		
					70°C	4	20		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min		25°C	65	80		dB
					0°C	60	84		
					70°C	60	85		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	65	95		dB
					0°C	60	94		
					70°C	60	96		
I_{DD}	Supply current (two amplifiers)		V_O = 2.5 V, No load	V_{IC} = 5 V,	25°C		1.4	3.2	mA
					0°C		1.6	3.6	
					70°C		1.2	2.6	

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.

5. This range also applies to each input individually.

electrical characteristics at specified free-air temperature, V_{DD} = 10 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS		T_A†	TLC272C, TLC272AC, TLC272BC, TLC277C			UNIT
						MIN	TYP	MAX	
V_{IO}	Input offset voltage	TLC272C	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 10 kΩ	25°C		1.1	10	mV
					Full range			12	
		TLC272AC	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 10 kΩ	25°C		0.9	5	
					Full range			6.5	
		TLC272BC	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 10 kΩ	25°C		290	2000	μV
					Full range			3000	
		TLC277C	V_O = 1.4 V, R_S = 50 Ω,	V_{IC} = 0, R_L = 10 kΩ	25°C		250	800	
					Full range			1900	
α_{VIO}	Temperature coefficient of input offset voltage				25°C to 70°C		2		μV/°C
I_{IO}	Input offset current (see Note 4)		V_O = 5 V,	V_{IC} = 5 V	25°C		0.1	60	pA
					70°C		7	300	
I_{IB}	Input bias current (see Note 4)				25°C		0.7	60	pA
					70°C		50	600	
V_{ICR}	Common-mode input voltage range (see Note 5)				25°C	−0.2 to 9	−0.3 to 9.2		V
					Full range	−0.2 to 8.5			V
V_{OH}	High-level output voltage		V_{ID} = 100 mV,	R_L = 10 kΩ	25°C	8	8.5		V
					0°C	7.8	8.5		
					70°C	7.8	8.4		
V_{OL}	Low-level output voltage		V_{ID} = −100 mV,	I_{OL} = 0	25°C		0	50	mV
					0°C		0	50	
					70°C		0	50	
A_{VD}	Large-signal differential voltage amplification		V_O = 1 V to 6 V,	R_L = 10 kΩ	25°C	10	36		V/mV
					0°C	7.5	42		
					70°C	7.5	32		
CMRR	Common-mode rejection ratio		V_{IC} = V_{ICR}min		25°C	65	85		dB
					0°C	60	88		
					70°C	60	88		
k_{SVR}	Supply-voltage rejection ratio ($\Delta V_{DD}/\Delta V_{IO}$)		V_{DD} = 5 V to 10 V,	V_O = 1.4 V	25°C	65	95		dB
					0°C	60	94		
					70°C	60	96		
I_{DD}	Supply current (two amplifiers)		V_O = 2.5 V, No load	V_{IC} = 5 V,	25°C		1.9	4	mA
					0°C		2.3	4.4	
					70°C		1.6	3.4	

† Full range is 0°C to 70°C.

NOTES: 4. The typical values of input bias current and input offset current below 5 pA were determined mathematically.
5. This range also applies to each input individually.

BIODATA

Nama	: Go Kian Djoen
NRP	: 5103096010
Tempat / Tanggal Lahir	: Surabaya / 23 April 1978
Alamat	: Jl. Cantikan Tengah IV/14 Surabaya
Agama	: Kristen

PENDIDIKAN :

- SD KEMALA BHAYANGKARI II SURABAYA1990
- SMP YPPI I SURABAYA 1993
- SMA YPPI II SURABAYA 1996
- UNIVERSITAS KATOLIK WIDYA MANDALA SURABAYA
  ANGKATAN 1996