LAMPIRAN

320	5.3
352	5.9
384	6.4
416	6.9
449	7.5
481	8
513	8.55
545	9
577	9.6
602	10
642	10.7
673	11.2
705	11.75
729	12.15
769	12.8
787	13.1
802	13.4
834	13.9
851	14.2
882	14.7
914	15.23
978	16.3
1010	16.83
984	17
949	17.2
918	17.9
950	18
981	19
1013	19.6
982	20
1000	20.5
969	20.635
937	21
906	21.5

Tabel pengukuran kecepatan terhadap waktu pada 1200 rpm

kecepatan(rpm)	Waktu(det)
0	0
32	0.5
61	1
91	1.5
131	2.2
160	2.7
192	3.2
224	3.7
256	4.3
288	4.8
320	5.3
352	5.9
384	6.4
416	6.9
449	7.5
481	8
513	8.55
545	9
577	9.6

609	10
642	10.7
673	11.2
705	11.75
729	12.15
769	12.8
787	13.1
802	13.4
834	13.9
851	14.2
882	14.7
914	15.23
978	16.3
1010	16.83
1041	17.35
1073	17.8
1105	18.4
1137	18.95
1169	19.48
1200	20
1168	20.2
1136	20.35
1120	20.6
1151	20.9
1182	21
1214	21.6

Tabel pengukuran kecepatan terhadap waktu pada 1400 rpm

kecepatan(rpm)	Waktu(det)
0	0
32	0.5
61	1
91	1.5
131	2.2
160	2.7
192	3.2
224	3.7
256	4.3
288	4.8
320	5.3
352	5.9
384	6.4
416	6.9
449	7.5
481	8
513	8.55
545	9
577	9.6
609	10
642	10.7
673	11.2
705	11.75
729	12.15
769	12.8
787	13.1
802	13.4

834	13.9
851	14.2
882	14.7
914	15.23
978	16.3
1010	16.83
1041	17.35
1073	17.8
1105	18.4
1137	18.95
1169	19.48
1200	20
1231	20.5
1263	21.05
1295	21.6
1326	22.1
1358	22.6
1390	23.2
1422	23.7
1387	24
1356	24.6
1391	24.9
1423	25
1383	25.6

Tabel pengukuran kecepatan terhadap waktu pada 1600 rpm

kecepatan(rpm)	Waktu(det)
0	0
32	0.5
61	1
91	1.5
131	2.2
160	2.7
192	3.2
224	3.7
256	4.3
288	4.8
320	5.3
352	5.9
384	6.4
416	6.9
449	7.5
481	8
513	8.55
545	9
577	9.6
609	10
642	10.7
673	11.2
705	11.75
729	12.15
769	12.8
787	13.1
802	13.4
834	13.9
851	14.2

882	14.7
914	15.23
978	16.3
1010	16.83
1041	17.35
1073	17.8
1105	18.4
1137	18.95
1169	19.48
1200	20
1231	20.5
1263	21.05
1295	21.6
1326	22.1
1358	22.6
1390	23.2
1422	23.7
1454	24.3
1485	24.75
1517	25.28
1549	25.8
1580	26.333
1612	26.9
1572	27
1604	27.6
1573	27.39

```
0001=DISPCLR     EQU   00000001B              ;DISPLAY CLEAR
0038=FUNCSET     EQU   00111000B              ;INTERFACE DATA LENGTH :8 BITS
0006=ENTRMOD     EQU   00000110B              ;INCREMENT, NO DISPLAY SHIFT
000C=DISPON      EQU   00001100B            ;DISPLAY ON, CURSOR OFF, BLINK OFF
000E=CURSOR      EQU   00001110B            ;DISPLAY ON, CURSOR ON, BLINK OFF
000D=BLINK       EQU   00001101B            ;DISPLAY ON, CURSOR OFF, BLINK ON
A000=LCD               EQU   0A000H
A000=LCD0              EQU   LCD+0                    ; LCD CONTROL OPERATION
A001=LCD1              EQU   LCD+1                    ; LCD DATA OPERATION
E000=PORT_A  EQU 0E000H ;port-2 PPI ini diberi alamat sesuai kapasitas EPROM
E001=PORT_B            EQU   0E001H                   ;
E002=PORT_C            EQU   0E002H                   ;
E003=CONTROL_REG       EQU   0E003H                   ;
000C=SETUP             EQU   0cH
000D=BUFFER            EQU   0dH
000E=INPUT             EQU   0eH
000F=outputdac         EQU   0fh
0008=simpan            EQU   08h
000A=setuprpm          EQU   0ah
0002=SizeX             EQU   2                        ;16 bit!
0020=Operand           EQU   020h
0022=Pembagi           EQU   022h
0024=HasilBagi         EQU   024h
0026=SisaBagi          EQU   026h
0022=Pengali           EQU   Pembagi
0024=HasilKali         EQU   HasilBagi

0000                   ORG   0000H
0000 41 14     =0214   AJMP  MAIN

0060                   ORG   060H
0060             Pembagian:
0060 78 24             MOV   R0,#HasilBagi
0062 11 D3     =00D3   ACALL HapusNilai
0064 78 26             MOV   R0,#SisaBagi
0066 11 D3     =00D3   ACALL HapusNilai
0068 7B 10             MOV   R3,#SizeX*8
006A               LoopPembagian:
006A C3                CLR   C
006B 78 20             MOV   R0,#Operand
006D 11 89     =0089   ACALL GeserKiri1X
006F 78 26             MOV   R0,#SisaBagi
0071 11 89     =0089   ACALL GeserKiri1X
0073 78 26             MOV   R0,#SisaBagi
0075 79 22             MOV   R1,#Pembagi
0077 11 BE     =00BE   ACALL Perbandingan             SisaBagi-Pembagi?
0079 40 06     =0081   JC    JanganDikurangi          SisaBagi<Pembagi, skip!
007B 78 26             MOV   R0,#SisaBagi
007D 79 22             MOV   R1,#Pembagi
007F 11 C8     =00C8   ACALL Pengurangan              SisaBagi:=SisaBagi-Pembagi
0081               JanganDikurangi:
0081 B3                CPL   C
0082 78 24             MOV   R0,#HasilBagi            Simpan hasil
0084 11 89     =0089   ACALL GeserKiri1X
0086 DB E2     =006A   DJNZ  R3,LoopPembagian
0088 22                RET
0089               GeserKiri1X:
0089 7A 02             MOV   R2,#SizeX
008B               LeftShift:
008B E6                MOV   A,@R0
008C 33                RLC   A
```

```
008D F6              MOV   @R0,A
008E 08              INC   R0
008F DA FA    =008B  DJNZ  R2,LeftShift
0091 22              RET
0092               Perkalian:
0092 78 24           MOV   R0,#HasilKali
0094 11 D3    =00D3  ACALL HapusNilai
0096 7B 10           MOV   R3,#SizeX*8
0098               LoopPerkalian:
0098 C3              CLR   C
0099 78 23           MOV   R0,#Pengali+SizeX-1
009B 7A 02           MOV   R2,#SizeX
009D               GeserKanan:
009D E6              MOV   A,@R0
009E 13              RRC   A
009F F6              MOV   @R0,A
00A0 18              DEC   R0
00A1 DA FA    =009D  DJNZ  R2,GeserKanan
00A3 50 06    =00AB  JNC   JanganDitambah
00A5 78 24           MOV   R0,#HasilKali
00A7 79 20           MOV   R1,#Operand
00A9 11 B3    =00B3  ACALL Penambahan
00AB               JanganDitambah:
00AB C3              CLR   C
00AC 78 20           MOV   R0,#Operand
00AE 11 89    =0089  ACALL GeserKiri1X
00B0 DB E6    =0098  DJNZ  R3,LoopPerkalian
00B2 22              RET
00B3               Penambahan:
00B3 C3              CLR   C
00B4 7A 02           MOV   R2,#SizeX
00B6               LoopPenambahan:
00B6 E6              MOV   A,@R0
00B7 37              ADDC  A,@R1
00B8 F6              MOV   @R0,A
00B9 08              INC   R0
00BA 09              INC   R1
00BB DA F9    =00B6  DJNZ  R2,LoopPenambahan
00BD 22              RET
00BE               Perbandingan:
00BE C3              CLR   C
00BF 7A 02           MOV   R2,#SizeX
00C1               LoopPerbandingan:
00C1 E6              MOV   A,@R0
00C2 97              SUBB  A,@R1
00C3 09              INC   R1
00C4 08              INC   R0
00C5 DA FA    =00C1  DJNZ  R2,LoopPerbandingan
00C7 22              RET
00C8               Pengurangan:
00C8 C3              CLR   C
00C9 7A 02           MOV   R2,#SizeX
00CB               LoopPengurangan:
00CB E6              MOV   A,@R0
00CC 97              SUBB  A,@R1
00CD F6              MOV   @R0,A
00CE 08              INC   R0
00CF 09              INC   R1
00D0 DA F9    =00CB  DJNZ  R2,LoopPengurangan
00D2 22              RET
00D3               HapusNilai:
```

```
00D3 7A 02           MOV   R2,#SizeX
00D5               LoopHapus:
00D5 76 00           MOV   @R0,#0
00D7 08              INC   R0
00D8 DA FB     =00D5 DJNZ  R2,LoopHapus
00DA 22              RET

00DB               POSISI2.1:
00DB C0 E0           PUSH  A
00DD EF              MOV   A,R7                    ;KOLOM 1
00DE               POSISI2:
00DE 24 C0           ADD   A,#11000000B            ;POSISI DI BARIS 2
00E0 80 05     =00E7 SJMP  POSISI.SUB
00E2               POSISI1.1:
00E2 C0 E0           PUSH  A
00E4 EE              MOV   A,R6                    ;KOLOM 1
00E5               POSISI1:
00E5 24 80           ADD   A,#10000000B            ;POSISI DI BARIS 1
00E7               POSISI.SUB:
00E7 14              DEC   A              ;AWALAN POSISI KOLOM DIMULAI DARI 0
00E8 11 FD     =00FD ACALL CONTROLOUT          ;KIRIM SEBAGAI OPERASI KONTROL
00EA D0 E0           POP   A
00EC 22              RET
00ED               PRINTSTRING2:               ;CETAK STRING DI BARIS 2 KOLOM 1
00ED 11 DB     =00DB ACALL POSISI2.1                ;BARIS 2 KOLOM 1
00EF 80 02     =00F3 SJMP  PRINTSTRING              ;CETAK STRING
00F1               PRINTSTRING1:               ;CETAK STRING DI BARIS 1 KOLOM 1
00F1 11 E2     =00E2 ACALL POSISI1.1                ;BARIS 1 KOLOM 1
00F3               PRINTSTRING:                      ;CETAK STRING
00F3 80 03     =00F8 SJMP  OUTSTRING                ;AMBIL DATA DULU
00F5               PRINTSTRINGLOOP:
00F5 31 06     =0106 ACALL DATAOUT                ;KIRIM SEBAGAI OPERASI DATA
00F7 A3              INC   DPTR                    ;POSISI DATA BERIKUTNYA
00F8               OUTSTRING:
00F8 E4              CLR   A                       ;POINTER=0
00F9 93              MOVC  A,@A+DPTR   ;AMBIL DATA DI EPROM BERDASARKAN DPTR
00FA 70 F9     =00F5 JNZ   PRINTSTRINGLOOP ;APAKAH MASIH ADA DATA BERIKUTNYA
00FC 22              RET
00FD               CONTROLOUT:
00FD C0 83           PUSH  DPH                     ;SIMPAN DPH DI STACK
00FF C0 82           PUSH  DPL                     ;SIMPAN DPL DI STACK
0101 90 A0 00        MOV   DPTR,#LCD0             ;ALAMAT OPERASI CONTROL LCD
0104 80 07     =010D SJMP  LCD.OUT                 ;KIRIM KE LCD
0106               DATAOUT:
0106 C0 83           PUSH  DPH                     ;SIMPAN DPH DI STACK
0108 C0 82           PUSH  DPL                     ;SIMPAN DPL DI STACK
010A 90 A0 01        MOV   DPTR,#LCD1              ;ALAMAT OPERASI DATA LCD
010D               LCD.OUT:                        ;KIRIM KE LCD
010D F0              MOVX  @DPTR,A
010E               DELAY.LCD:
010E 74 FA           MOV   A,#250                  ;250
0110 D5 E0 FD  =0110 DJNZ  A,$
0113 D0 82           POP   DPL                   ;AMBIL KEMBALI DPL DARI STACK
0115 D0 83           POP   DPH                   ;AMBIL KEMBALI DPH DARI STACK
0117 22              RET
0118               DELAYIT:
0118 79 40           MOV   R1,#040h                ;20h
011A               DLY.LCD.LP:
011A 7A 14           MOV   R2,#20                  ;0
011C DA FE     =011C DJNZ  R2,$
011E D9 FA     =011A DJNZ  R1,DLY.LCD.LP
```

```
0120 22              RET
0121              INIT.LCD:
0121 74 01           MOV   A,#DISPCLR          ;DISPLAY CLEAR
0123 11 FD    =00FD  ACALL CONTROLOUT
0125 31 18    =0118  ACALL DELAYIT
0127 74 38           MOV   A,#FUNCSET          ;FUNCTION SET
0129 11 FD    =00FD  ACALL CONTROLOUT
012B 74 0C           MOV   A,#DISPON           ;DISPLAY ON
012D 11 FD    =00FD  ACALL CONTROLOUT
012F 74 06           MOV   A,#ENTRMOD          ;ENTRY MODE
0131 11 FD    =00FD  ACALL CONTROLOUT
0133 22              RET

0134              delay:
0134 7B 02           MOV   r3,#2
0136              delay2:
0136 7C FF           MOV   r4,#255
0138              delay1:
0138 7D FF           MOV   r5,#255
013A DD FE    =013A  DJNZ  r5,$
013C DC FA    =0138  DJNZ  r4,delay1
013E DB F6    =0136  DJNZ  r3,delay2
0140 22              RET

0141              tamp_setup:
0141 7E 0C           MOV   r6,#12
0143 11 E2    =00E2  ACALL posisi1.1
0145 74 00           MOV   a,#0
0147 24 30           ADD   a,#30h
0149 31 06    =0106  ACALL dataout

014B 85 0C 0D        MOV   buffer,setup
014E 7E 0B           MOV   r6,#11
0150              ulang1:
0150 11 E2    =00E2  ACALL posisi1.1
0152 E5 0D           MOV   a,buffer
0154 75 F0 0A        MOV   b,#10
0157 84              DIV   ab
0158 F5 0D           MOV   buffer,a
015A E5 F0           MOV   a,b
015C 24 30           ADD   a,#30h
015E 31 06    =0106  ACALL dataout
0160 1E              DEC   r6
0161 BE 08 EC =0150  CJNE  r6,#8,ulang1

0164 7E 0E           MOV   r6,#14
0166 11 E2    =00E2  ACALL posisi1.1
0168 74 52           MOV   a,#'R'
016A 31 06    =0106  ACALL dataout
016C 7E 0F           MOV   r6,#15
016E 11 E2    =00E2  ACALL posisi1.1
0170 74 50           MOV   a,#'P'
0172 31 06    =0106  ACALL dataout
0174 7E 10           MOV   r6,#16
0176 11 E2    =00E2  ACALL posisi1.1
0178 74 4D           MOV   a,#'M'
017A 31 06    =0106  ACALL dataout
017C 22              RET

017D              tampilan:
017D 85 08 24        MOV   hasilbagi,simpan
```

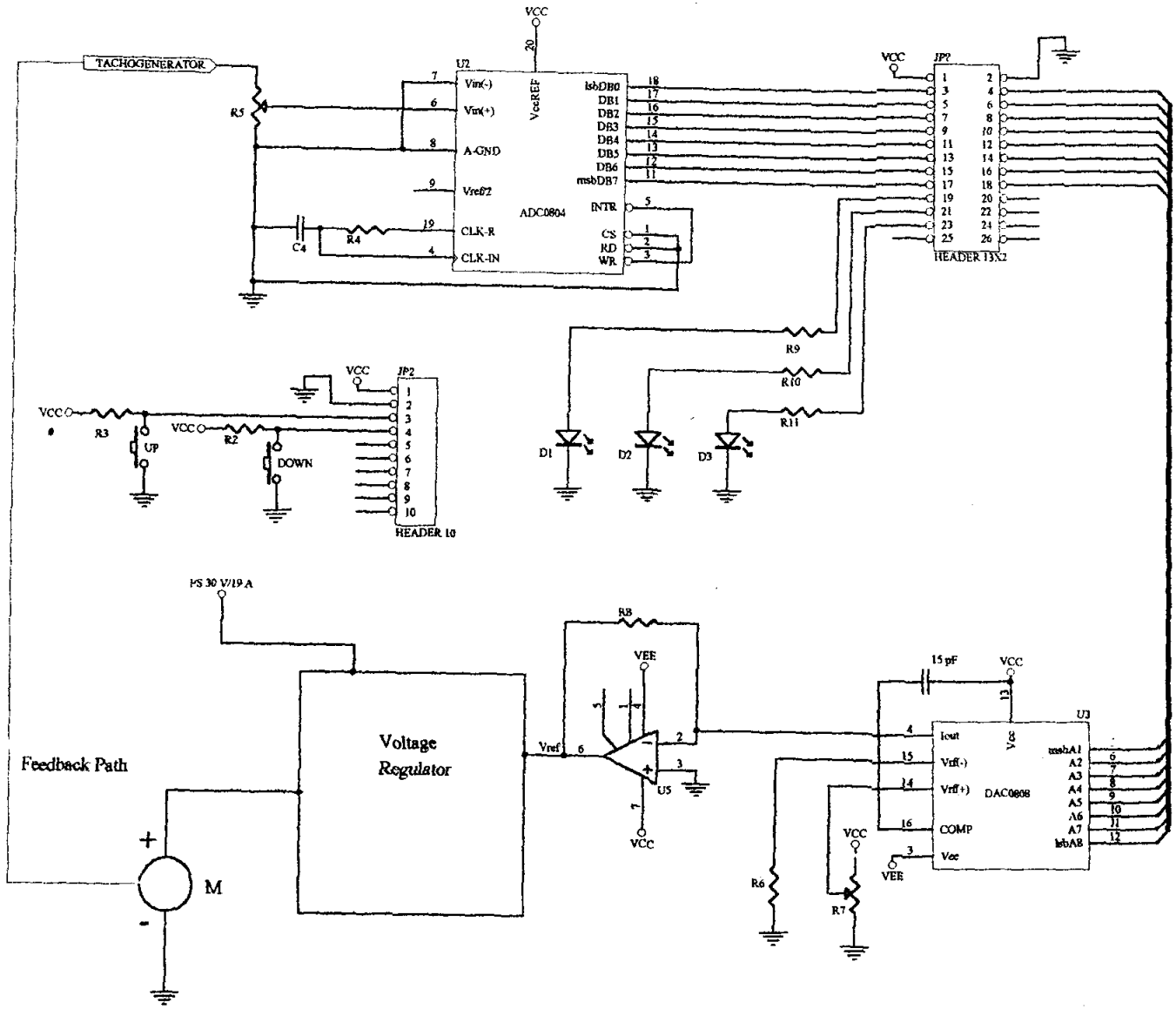
```
0180 85 09 25          MOV   hasilbagi+1,simpan+1
0183 7F 0C             MOV   R7,#12
0185              ulxx:
0185 11 DB      =00DB  ACALL POSISI2.1
0187 85 24 20          MOV   operand,hasilbagi
018A 85 25 21          MOV   operand+1,hasilbagi+1
018D 75 22 0A          MOV   pembagi,#10
0190 11 60      =0060  ACALL pembagian
0192 78 26             MOV   r0,#sisabagi
0194 E6                MOV   a,@r0
0195 C0 E0             PUSH  a
0197 78 24             MOV   r0,#hasilbagi
0199 E6                MOV   a,@r0
019A B4 00 08 =01A5    CJNE  a,#0,err
019D D0 E0             POP   a
019F 24 30             ADD   A,#30H
01A1 31 06      =0106  ACALL DATAOUT
01A3 21 B1      =01B1  AJMP  akhir
01A5              err:
01A5 D0 E0             POP   a
01A7 24 30             ADD   A,#30H
01A9 31 06      =0106  ACALL DATAOUT
01AB 1F                DEC   r7
01AC BF 08 D6 =0185    CJNE  r7,#8,ulxx
01AF 21 C7      =01C7  AJMP  selesai

01B1              akhir:
01B1 BF 01 08 =01BC    CJNE  r7,#1,ada
01B4 11 DB      =00DB  ACALL posisi2.1
01B6 74 30             MOV   a,#'0'
01B8 31 06      =0106  ACALL dataout
01BA 21 C7      =01C7  AJMP  selesai
01BC              ada:
01BC 1F                DEC   r7
01BD              bersih:
01BD 11 DB      =00DB  ACALL posisi2.1
01BF 74 20             MOV   a,#' '
01C1 31 06      =0106  ACALL dataout
01C3 1F                DEC   r7
01C4 BF 08 F6 =01BD    CJNE  r7,#8,bersih

01C7              selesai:
01C7 7F 0E             MOV   r7,#14
01C9 11 DB      =00DB  ACALL posisi2.1
01CB 74 52             MOV   a,#'R'
01CD 31 06      =0106  ACALL dataout
01CF 7F 0F             MOV   r7,#15
01D1 11 DB      =00DB  ACALL posisi2.1
01D3 74 50             MOV   a,#'P'
01D5 31 06      =0106  ACALL dataout
01D7 7F 10             MOV   r7,#16
01D9 11 DB      =00DB  ACALL posisi2.1
01DB 74 4D             MOV   a,#'M'
01DD 31 06      =0106  ACALL dataout
01DF 22                RET

01E0              hitung_rpm:
01E0 85 0A 20          MOV   operand,setuprpm
01E3 85 0B 21          MOV   operand+1,setuprpm+1
01E6 75 22 0A          MOV   pengali,#10
01E9 11 92      =0092  ACALL perkalian
```

```
01EB 85 24 0A          MOV   setuprpm,hasilkali
01EE 85 25 0B          MOV   setuprpm+1,hasilkali+1

01F1 85 08 20          MOV   operand,simpan
01F4 85 09 21          MOV   operand+1,simpan+1
01F7 75 22 20          MOV   pengali,#32
01FA 11 92     =0092   ACALL perkalian
01FC 85 24 08          MOV   simpan,hasilkali
01FF 85 25 09          MOV   simpan+1,hasilkali+1
0202 85 08 20          MOV   operand,simpan
0205 85 09 21          MOV   operand+1,simpan+1
0208 75 22 05          MOV   pembagi,#5
020B 11 60     =0060   ACALL pembagian
020D 85 24 08          MOV   simpan,hasilkali
0210 85 25 09          MOV   simpan+1,hasilkali+1
0213 22                RET

0214              MAIN:
0214 75 81 60          MOV   SP,#60H                ;
0217 75 A8 00          MOV   ie,#00H
021A 31 21     =0121   ACALL init.lcd
021C 71 68     =0368   ACALL INIT_PPI
021E 7E 01             MOV   r6,#1
0220 7F 01             MOV   r7,#1
0222 90 03 77          MOV   dptr,#header1
0225 11 F1     =00F1   ACALL printstring1
0227 90 03 88          MOV   dptr,#header2
022A 11 ED     =00ED   ACALL printstring2
022C 31 34     =0134   ACALL delay
022E 7E 01             MOV   r6,#1
0230 7F 01             MOV   r7,#1
0232 90 03 99          MOV   dptr,#header3
0235 11 F1     =00F1   ACALL printstring1
0237 90 03 AA          MOV   dptr,#header4
023A 11 ED     =00ED   ACALL printstring2
023C 31 34     =0134   ACALL delay
023E 7E 01             MOV   r6,#1
0240 7F 01             MOV   r7,#1
0242 90 03 BB          MOV   dptr,#header5
0245 11 F1     =00F1   ACALL printstring1
0247 90 03 CC          MOV   dptr,#header6
024A 11 ED     =00ED   ACALL printstring2
024C 31 34     =0134   ACALL delay
024E 7E 01             MOV   r6,#1
0250 7F 01             MOV   r7,#1
0252 90 03 DD          MOV   dptr,#header7
0255 11 F1     =00F1   ACALL printstring1
0257 90 03 EE          MOV   dptr,#header8
025A 11 ED     =00ED   ACALL printstring2
025C 31 34     =0134   ACALL delay

025E 75 0C 00          MOV   setup,#0
0261 75 0D 00          MOV   buffer,#0
0264 75 0E 00          MOV   input,#0
0267 75 0F 00          MOV   outputdac,#0

026A 74 01             MOV   A,#DISPCLR             ;DISPLAY CLEAR
026C 11 FD     =00FD   ACALL CONTROLOUT
026E 31 34     =0134   ACALL delay
0270 90 03 FF          MOV   dptr,#output
0273 7E 01             MOV   r6,#1
```

```
0275 11 F1    =00F1  ACALL printstring1
0277 90 04 07        MOV   dptr,#output2
027A 7F 01           MOV   r7,#1
027C 11 ED    =00ED  ACALL printstring2
027E 31 34    =0134  ACALL delay
0280 31 41    =0141  ACALL tamp_setup

0282             TEST:
0282 30 90 6B =02F0  JNB   P1.0,UP ;jika tb UP ditekan maka akan ke label UP
0285 30 91 7A =0302  JNB   P1.1,DOWN  ;jika tb DOWN ditekan ke label DOWN
0288 71 4A    =034A  ACALL READ_ADC                ;panggil label READ_ADC
028A 75 08 00        MOV   simpan,#0
028D 75 09 00        MOV   simpan+1,#0
0290 75 0A 00        MOV   setuprpm,#0
0293 75 0B 00        MOV   setuprpm+1,#0
0296 85 0E 08        MOV   simpan,input
0299 85 0C 0A        MOV   setuprpm,setup

029C 31 E0    =01E0  ACALL hitung_rpm

029E 78 08           MOV   r0,#simpan
02A0 79 0A           MOV   r1,#setuprpm
02A2 11 BE    =00BE  ACALL perbandingan
02A4 40 23    =02C9  JC    tambah_kecepatan

02A6 E5 0F           MOV   a,outputdac
02A8 B4 00 02 =02AD  CJNE  a,#0,kurang
02AB 41 EA    =02EA  AJMP  lompat
02AD             kurang:
02AD 15 0F           DEC   outputdac
02AF 7F 04           MOV   r7,#4
02B1 11 DB    =00DB  ACALL posisi2.1
02B3 74 28           MOV   a,#'('
02B5 31 06    =0106  ACALL dataout
02B7 7F 05           MOV   r7,#5
02B9 11 DB    =00DB  ACALL posisi2.1
02BB 74 4B           MOV   a,#'K'
02BD 31 06    =0106  ACALL dataout
02BF 7F 06           MOV   r7,#6
02C1 11 DB    =00DB  ACALL posisi2.1
02C3 74 29           MOV   a,#')'
02C5 31 06    =0106  ACALL dataout

02C7 41 EA    =02EA  AJMP  lompat

02C9             tambah_kecepatan:
02C9 E5 0F           MOV   a,outputdac
02CB B4 FF 02 =02D0  CJNE  a,#255,tambah
02CE 41 EA    =02EA  AJMP  lompat
02D0             tambah:
02D0 05 0F           INC   outputdac
02D2 7F 04           MOV   r7,#4
02D4 11 DB    =00DB  ACALL posisi2.1
02D6 74 28           MOV   a,#'('
02D8 31 06    =0106  ACALL dataout
02DA 7F 05           MOV   r7,#5
02DC 11 DB    =00DB  ACALL posisi2.1
02DE 74 54           MOV   a,#'T'
02E0 31 06    =0106  ACALL dataout
02E2 7F 06           MOV   r7,#6
02E4 11 DB    =00DB  ACALL posisi2.1
```

```
02E6 74 29           MOV   a,#')'
02E8 31 06     =0106 ACALL dataout

02EA             lompat:
02EA 71 59     =0359 ACALL DAC_OUT                ;panggil label DAC_OUT
02EC 31 7D     =017D ACALL tampilan

02EE 41 82     =0282 AJMP  TEST                   ;kembali ke label TEST

02F0             UP:
02F0 A8 0C           MOV   r0,setup
02F2 B8 A0 05 =02FA  CJNE  r0,#160,lom1
02F5 75 0C 00        MOV   setup,#0
02F8 41 FC     =02FC AJMP  lom3
02FA             lom1:
02FA 05 0C           INC   SETUP
02FC             lom3:
02FC 71 34     =0334 ACALL delay_2ss
02FE 31 41     =0141 ACALL tamp_setup
0300 41 82     =0282 AJMP  TEST

0302             DOWN:
0302 A8 0C           MOV   r0,setup
0304 B8 00 05 =030C  CJNE  r0,#0,lom2
0307 75 0C A0        MOV   setup,#160
030A 61 0E     =030E AJMP  lom4
030C             lom2:
030C 15 0C           DEC   SETUP
030E             lom4:
030E 71 34     =0334 ACALL delay_2ss
0310 31 41     =0141 ACALL tamp_setup
0312 41 82     =0282 AJMP  TEST

0314             DELAY_2S:
0314 C0 83           PUSH  DPH
0316 C0 82           PUSH  DPL
0318 C0 E0           PUSH  ACC
031A C0 D0           PUSH  PSW
031C 7D 01           MOV   R5,#01H
031E             DEL3:
031E 74 4F           MOV   A,#04FH
0320             DEL4:
0320 75 F0 FF        MOV   B,#0FFH
0323 D5 F0 FD =0323  DJNZ  B,$
0326 D5 E0 F7 =0320  DJNZ  ACC,DEL4
0329 DD F3     =031E DJNZ  R5,DEL3
032B D0 D0           POP   PSW
032D D0 E0           POP   ACC
032F D0 82           POP   DPL
0331 D0 83           POP   DPH
0333 22              RET

0334             DELAY_2SS:
0334 C0 83           PUSH  DPH
0336 C0 82           PUSH  DPL
0338 90 E0 02        MOV   DPTR,#PORT_C
033B 74 01           MOV   A,#00000001B
033D F0              MOVX  @DPTR,A
033E 71 14     =0314 ACALL DELAY_2s
0340 74 00           MOV   A,#00000000B
0342 F0              MOVX  @DPTR,A
```

```
0343 71 14     =0314  ACALL DELAY_2s
0345 D0 82            POP   DPL
0347 D0 83            POP   DPH
0349 22               RET
;-------------------------------------------------------------------------------
034A                READ_ADC:
034A C0 83            PUSH  DPH
034C C0 82            PUSH  DPL
034E 90 E0 00         MOV   DPTR,#PORT_A
0351 E0               MOVX  A,@DPTR
0352 F5 0E            MOV   input,a
0354 D0 82            POP   DPL
0356 D0 83            POP   DPH
0358 22               RET
;-------------------------------------------------------------------------------
0359                DAC_OUT:
0359 C0 83            PUSH  DPH
035B C0 82            PUSH  DPL
035D 90 E0 01         MOV   DPTR,#PORT_B
0360 E5 0F            MOV   A,outputdac
0362 F0               MOVX  @DPTR,A
0363 D0 82            POP   DPL
0365 D0 83            POP   DPH
0367 22               RET

0368                INIT_PPI:
0368 C0 83            PUSH  DPH
036A C0 82            PUSH  DPL
036C 90 E0 03         MOV   DPTR,#CONTROL_REG
036F 74 98            MOV   A,#98H
0371 F0               MOVX  @DPTR,A
0372 D0 82            POP   DPL
0374 D0 83            POP   DPH
0376 22               RET

;-------------------------------------------------------------------------------
0377                HEADER1:
0377 4D 49 43         DB    'MICROCONTROLLER ',0
0388                HEADER2:
0388 20 20 20         DB    '    DRIVEN      ',0
0399                HEADER3:
0399 20 44 49         DB    ' DIGITAL MOTOR  ',0
03AA                HEADER4:
03AA 53 50 45         DB    'SPEED CONTROLLER',0
03BB                HEADER5:
03BB 20 20 44         DB    '  DESIGNED BY:  ',0
03CC                HEADER6:
03CC 20 20 20         DB    '    BAMBANG     ',0
03DD                HEADER7:
03DD 20 20 20         DB    '   FTE  UNIKA   ',0
03EE                HEADER8:
03EE 20 20 57         DB    '  WIDYA MANDALA ',0
03FF                OUTPUT:
03FF 53 45 54         DB    'SETUP :',0
0407                OUTPUT2:
0407 52 50 4D         DB    'RPM   :',0

***** Successfull
```



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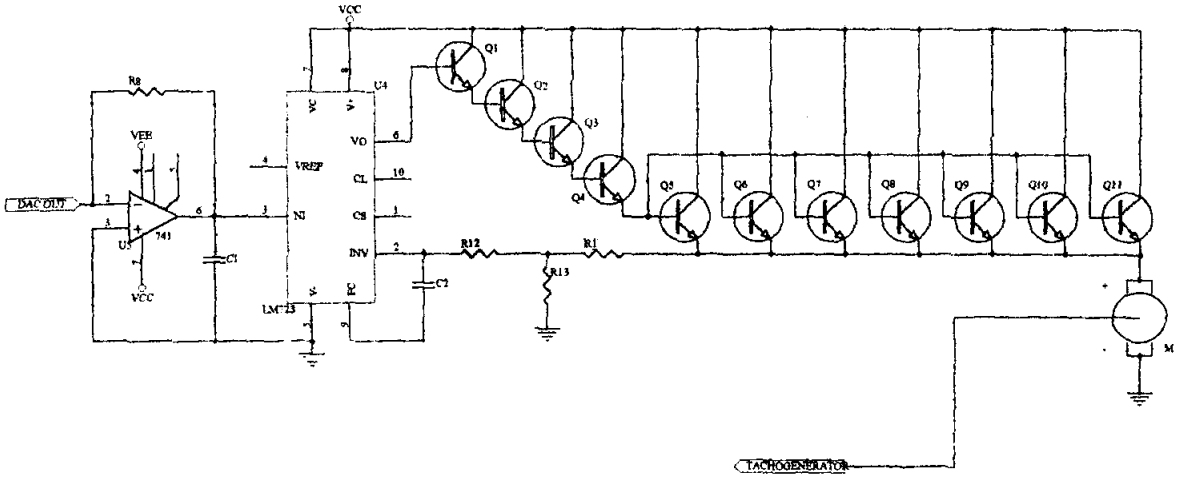
Date: 3-Apr-2002	Sheet of	
File: D:\Documents Mahasiswa\MYP\bambang	Drawn By:	



Title	Rangkaian Regulasi Tegangan	
Size: B	Number: Bambang Sugiarto / 5105095029	Revision:
Date: 3-Apr-2002	Sheet of: 2	
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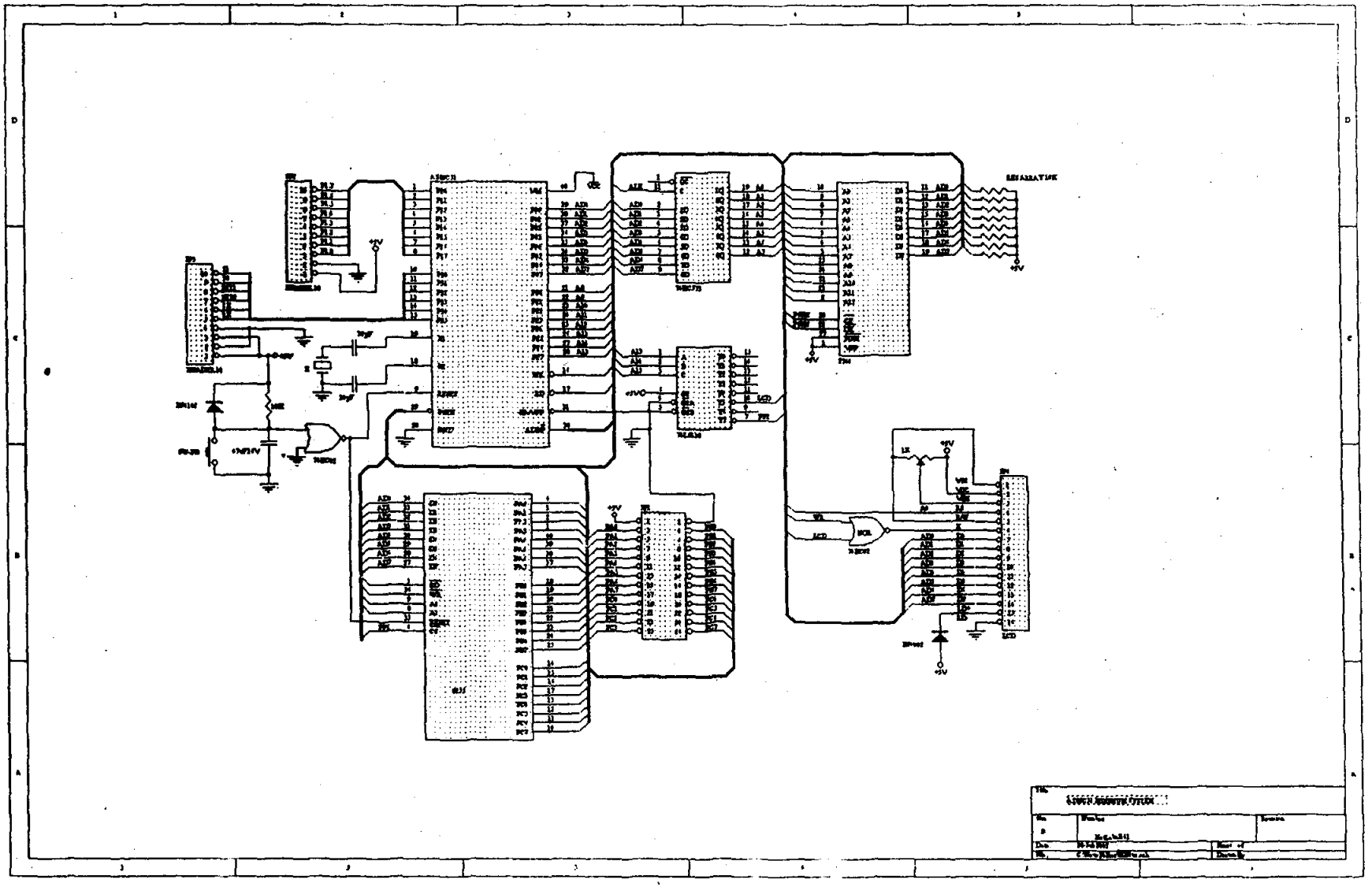


Features

- Compatible with MCS-51™ Products
- 4K Bytes of In-System Reprogrammable Flash Memory
  - Endurance: 1,000 Write/Erase Cycles
- Fully Static Operation: 0 Hz to 24 MHz
- Three-Level Program Memory Lock
- 128 x 8-Bit Internal RAM
- 32 Programmable I/O Lines
- Two 16-Bit Timer/Counters
- Six Interrupt Sources
- Programmable Serial Channel
- Low Power Idle and Power Down Modes

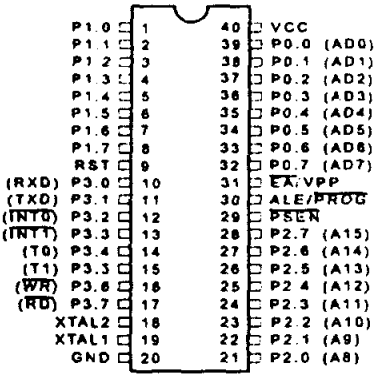
Description

The AT89C51 is a low-power, high-performance CMOS 8-bit microcomputer with 4K Bytes of Flash Programmable and Erasable Read Only Memory (PEROM). The device is manufactured using Atmel's high density nonvolatile memory technology and is compatible with the industry standard MCS-51™ instruction set and pinout. The on-chip Flash allows the program memory to be reprogrammed in-system or by a conventional nonvolatile memory programmer. By combining a versatile 8-bit CPU with Flash on a monolithic chip, the Atmel AT89C51 is a powerful microcomputer which provides a highly flexible and cost effective solution to many embedded control applications.

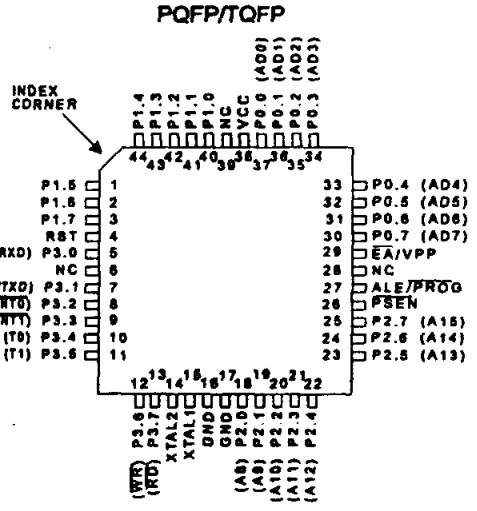
(continued)

Pin Configurations

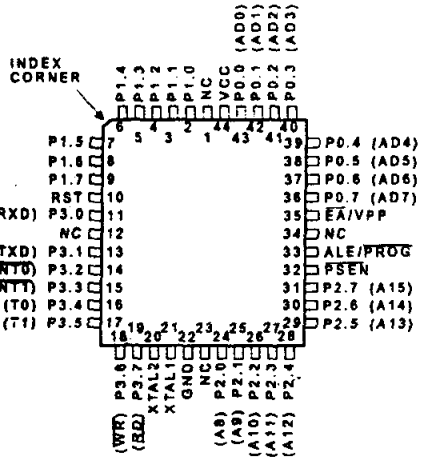
PDIP



PQFP/TQFP



PLCC



8-Bit Microcontroller with 4K Bytes Flash

AT89C51

0265F-A-12/97

National Semiconductor Corporation

DC0801, ADC0802, ADC0803, ADC0804, DC0805 8-Bit µP Compatible A/D Converters

eneral Description

ADC0801, ADC0802, ADC0803, ADC0804 and C0805 are CMOS 8-bit successive approximation A/D verters that use a differential potentiometric ladder—lar to the 256R products. These converters are de-ed to allow operation with the NSC800 and INS8080A vative control bus with TRI-STATE® output latches di-ly driving the data bus. These A/Ds appear like memory tions or I/O ports to the microprocessor and no inter-ng logic is needed.

erential analog voltage inputs allow increasing the com-n-mode rejection and offsetting the analog zero input age value. In addition, the voltage reference input can adjusted to allow encoding any smaller analog voltage n to the full 8 bits of resolution.

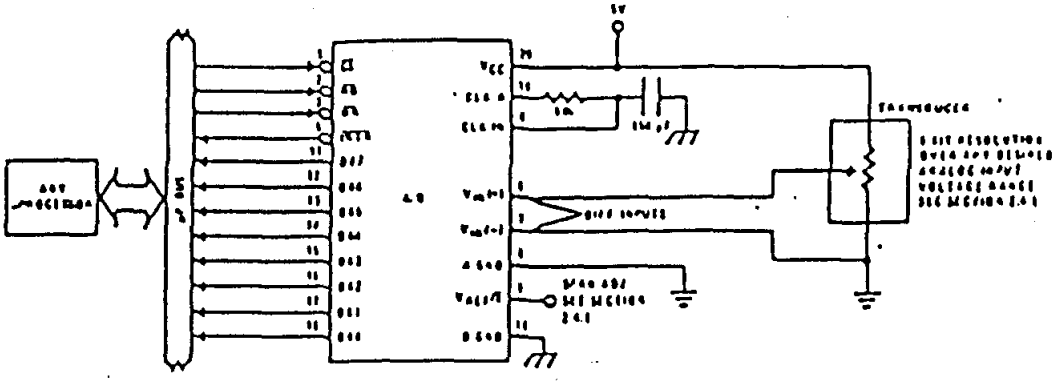
atures

- ompatible with 8080 µP derivatives—no interfacing ogic needed - access time - 135 ns
- asy interface to all microprocessors, or operates stand alone"
- Differential analog voltage inputs
- Logic inputs and outputs meet both MOS and TTL voltage level specifications
- Works with 2.5V (LM336) voltage reference
- On-chip clock generator
- 0V to 5V analog input voltage range with single 5V supply
- No zero adjust required
- 0.3" standard width 20-pin DIP package
- 20-pin molded chip carrier or small outline package
- Operates ratiometrically or with 5 V_{DC}, 2.5 V_{DC}, or analog span adjusted voltage reference

Key Specifications

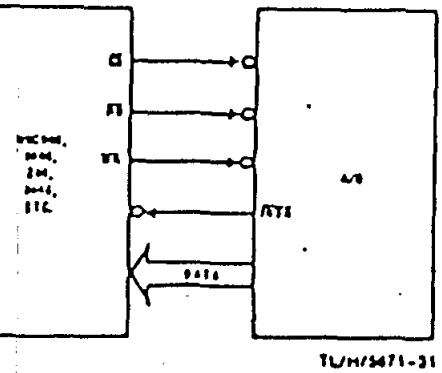
- Resolution: 8 bits
- Total error: ±¼ LSB, ±½ LSB and ±1 LSB
- Conversion time: 100 µs

pical Applications



TL/H/5671-1

8080 Interface



TL/H/5671-21

Error Specification (Includes Full-Scale, Zero Error, and Non-Linearity)			
Part Number	Full-Scale Adjusted	$V_{REF}/2 = 2.500\ V_{DC}$ (No Adjustments)	$V_{REF}/2$ = No Connection (No Adjustments)
ADC0801	±¼ LSB		
ADC0802		±½ LSB	
ADC0803	±½ LSB		
ADC0804		±1 LSB	
ADC0805			±1 LSB

te Maximum Ratings (Notes 1 & 2)

Aerospace specified devices are required, e - National Semiconductor Sales Office/ s for availability and specifications.

age (V_{CC}) (Note 3)	6.5V
ntrol Inputs	−0.3V to +18V
nput and Outputs	−0.3V to (V_{CC} + 0.3V)
(Soldering, 10 seconds)	
line Package (plastic)	260°C
line Package (ceramic)	300°C
Mount Package	
Phase (60 seconds)	215°C
d (15 seconds)	220°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation at T_A = 25°C	875 mW
ESD Susceptibility (Note 10)	800V

Operating Ratings (Notes 1 & 2)

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
ADC0801/02LJ	−55°C ≤ T_A ≤ +125°C
ADC0801/02/03/04LCJ	−40°C ≤ T_A ≤ +85°C
ADC0801/02/03/05LCN	−40°C ≤ T_A ≤ +85°C
ADC0804LCN	0°C ≤ T_A ≤ +70°C
ADC0802/03/04LCV	0°C ≤ T_A ≤ +70°C
ADC0802/03/04LCWM	0°C ≤ T_A ≤ +70°C
Range of V_{CC}	4.5 V_{DC} to 6.3 V_{DC}

cal Characteristics

ng specifications apply for V_{CC} = 5 V_{DC}, $T_{MIN} \le T_A \le T_{MAX}$ and f_{CLK} = 640 kHz unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Total Adjusted Error (Note 8)	With Full-Scale Adj. (See Section 2.5.2)			± ¼	LSB
Total Unadjusted Error (Note 8)	$V_{REF}/2$ = 2.500 V_{DC}			± ½	LSB
Total Adjusted Error (Note 8)	With Full-Scale Adj. (See Section 2.5.2)			± ½	LSB
Total Unadjusted Error (Note 8)	$V_{REF}/2$ = 2.500 V_{DC}			± 1	LSB
Total Unadjusted Error (Note 8)	$V_{REF}/2$-No Connection			± 1	LSB
ut Resistance (Pin 9)	ADC0801/02/03/05 ADC0804 (Note 9)	2.5 0.75	8.0 1.1		kΩ kΩ
t Voltage Range	(Note 4) V(+) or V(−)	Gnd−0.05		V_{CC} + 0.05	V_{DC}
n-Mode Error	Over Analog Input Voltage Range		± 1/16	± ⅛	LSB
ly Sensitivity	V_{CC} = 5 V_{DC} ± 10% Over Allowed $V_{IN}(+)$ and $V_{IN}(-)$ Voltage Range (Note 4)		± 1/16	± ⅛	LSB

ctrical Characteristics

g specifications apply for V_{CC} = 5 V_{DC} and T_A = 25°C unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Conversion Time	f_{CLK} = 640 kHz (Note 6)	103		114	μs
Conversion Time	(Note 5, 6)	66		73	$1/f_{CLK}$
Clock Frequency Clock Duty Cycle	V_{CC} = 5V, (Note 5) (Note 5)	100 40	640	1460 60	kHz %
Conversion Rate in Free-Running Mode	$\overline{INTR}$ tied to $\overline{WR}$ with $\overline{CS}$ = 0 V_{DC}, f_{CLK} = 640 kHz	8770		9708	conv/s
Width of $\overline{WR}$ Input (Start Pulse Width)	$\overline{CS}$ = 0 V_{DC} (Note 7)	100			ns
Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Data Valid)	C_L = 100 pF		135	200	ns
TRI-STATE Control (Delay from Rising Edge of $\overline{RD}$ to Hi-Z State)	C_L = 10 pF, R_L = 10k (See TRI-STATE Test Circuits)		125	200	ns
Delay from Falling Edge of $\overline{WR}$ or $\overline{RD}$ to Reset of $\overline{INTR}$			300	450	ns
Input Capacitance of Logic Control Inputs			5	7.5	pF
TRI-STATE Output Capacitance (Data Buffers)			5	7.5	pF
PUTS (Note: CLK IN (Pin 4) is the input of a Schmitt trigger circuit and is therefore specified separately)					
Logical "1" Input Voltage (Except Pin 4 CLK IN)	V_{CC} = 5.25 V_{DC}	2.0		15	V_{DC}

Electrical Characteristics (Continued)

llowing specifications apply for V_{CC} = 5 V_{DC} and $T_{MIN} \le T_A \le T_{MAX}$, unless otherwise specified.

ol	Parameter	Conditions	Min	Typ	Max	Units
ROL INPUTS (Note: CLK IN (Pin 4) is the input of a Schmitt trigger circuit and is therefore specified separately)						
)	Logical "0" Input Voltage (Except Pin 4 CLK IN)	V_{CC} = 4.75 V_{DC}			0.8	V_{DC}
	Logical "1" Input Current (All Inputs)	V_{IN} = 5 V_{DC}		0.005	1	μA_{DC}
)	Logical "0" Input Current (All Inputs)	V_{IN} = 0 V_{DC}	−1	−0.005		μA_{DC}
CK IN AND CLOCK R						
	CLK IN (Pin 4) Positive Going Threshold Voltage		2.7	3.1	3.5	V_{DC}
	CLK IN (Pin 4) Negative Going Threshold Voltage		1.5	1.8	2.1	V_{DC}
	CLK IN (Pin 4) Hysteresis $(V_T+)-(V_T-)$		0.6	1.3	2.0	V_{DC}
(0)	Logical "0" CLK R Output Voltage	I_O = 360 μA, V_{CC} = 4.75 V_{DC}			0.4	V_{DC}
(1)	Logical "1" CLK R Output Voltage	I_O = −360 μA, V_{CC} = 4.75 V_{DC}	2.4			V_{DC}
A OUTPUTS AND $\overline{INTR}$						
(0)	Logical "0" Output Voltage Data Outputs $\overline{INTR}$ Output	 I_{OUT} = 1.6 mA, V_{CC} = 4.75 V_{DC} I_{OUT} = 1.0 mA, V_{CC} = 4.75 V_{DC}			 0.4 0.4	 V_{DC} V_{DC}
(1)	Logical "1" Output Voltage	I_O = −360 μA, V_{CC} = 4.75 V_{DC}	2.4			V_{DC}
(1)	Logical "1" Output Voltage	I_O = −10 μA, V_{CC} = 4.75 V_{DC}	4.5			V_{DC}
	TRI-STATE Disabled Output Leakage (All Data Buffers)	V_{OUT} = 0 V_{DC} V_{OUT} = 5 V_{DC}	−3		 3	μA_{DC} μA_{DC}
ACE		V_{OUT} Short to Gnd, T_A = 25°C	4.5	6		mA_{DC}
		V_{OUT} Short to V_{CC}, T_A = 25°C	9.0	16		mA_{DC}
ER SUPPLY						
	Supply Current (Includes Ladder Current) ADC0801/02/03/04LCJ/05 ADC0804LCN/LCV/LCWM	f_{CLK} = 640 kHz, $V_{REF}/2$ = NC, T_A = 25°C and $\overline{CS}$ = 5V		 1.1 1.9	 1.8 2.5	 mA mA

: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating vice beyond its specified operating conditions.

: All voltages are measured with respect to Gnd, unless otherwise specified. The separate A Gnd point should always be wired to the D Gnd.

: A zener diode exists, internally, from V_{CC} to Gnd and has a typical breakdown voltage of 7 V_{DC}.

: For $V_{IN}(-) \ge V_{IN}(+)$ the digital output code will be 0000 0000. Two on-chip diodes are tied to each analog input (see block diagram) which will forward for analog input voltages one diode drop below ground or one diode drop greater than the V_{CC} supply. Be careful, during testing at low V_{CC} levels (4.5V), h level analog inputs (5V) can cause this input diode to conduct—especially at elevated temperatures, and cause errors for analog inputs near full-scale. The llows 50 mV forward bias of either diode. This means that as long as the analog V_{IN} does not exceed the supply voltage by more than 50 mV, the output ll be correct. To achieve an absolute 0 V_{DC} to 5 V_{DC} input voltage range will therefore require a minimum supply voltage of 4.950 V_{DC} over temperature ns, initial tolerance and loading.

: Accuracy is guaranteed at f_{CLK} = 640 kHz. At higher clock frequencies accuracy can degrade. For lower clock frequencies, the duty cycle limits can be ed so long as the minimum clock high time interval or minimum clock low time interval is no less than 275 ns.

: With an asynchronous start pulse, up to 8 clock periods may be required before the internal clock phases are proper to start the conversion process. The quest is internally latched, see *Figure 2* and section 2.0.

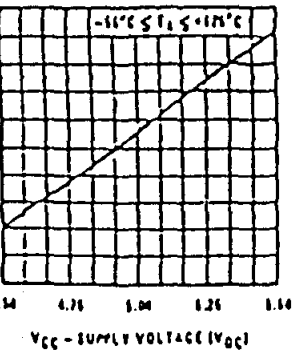
: The $\overline{CS}$ input is assumed to bracket the $\overline{WR}$ strobe input and therefore timing is dependent on the $\overline{WR}$ pulse width. An arbitrarily wide pulse width will hold verter in a reset mode and the start of conversion is initiated by the low to high transition of the $\overline{WR}$ pulse (see timing diagrams).

: None of these A/Ds requires a zero adjust (see section 2.5.1). To obtain zero code at other analog input voltages see section 2.5 and *Figure 5*.

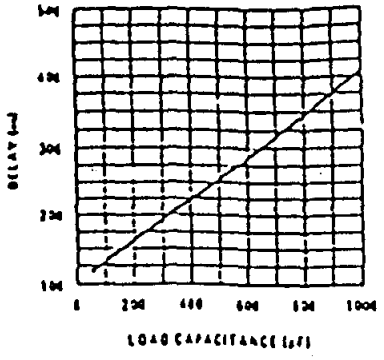
: The $V_{REF}/2$ pin is the center point of a two resistor divider connected from V_{CC} to ground. Each resistor is 2.2k, except for the ADC0804LCJ where each is 1Ω. Total ladder input resistance is the sum of the two equal resistors.

cal Performance Characteristics

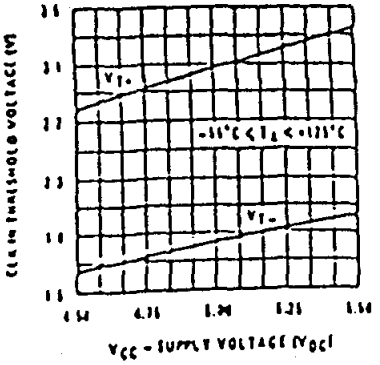
Logic Input Threshold Voltage vs. Supply Voltage



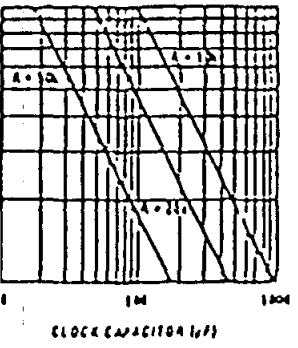
Delay From Falling Edge of $\overline{RD}$ to Output Data Valid vs. Load Capacitance



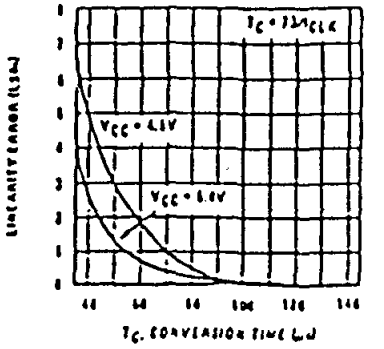
CLK IN Schmitt Trip Levels vs. Supply Voltage



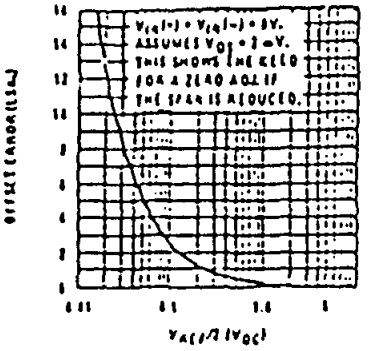
f_{CLK} vs. Clock Capacitor



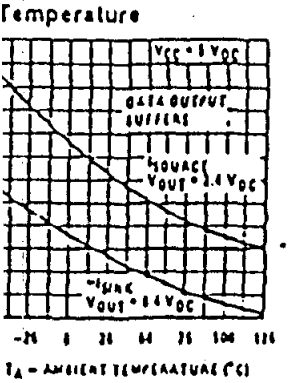
Full-Scale Error vs Conversion Time



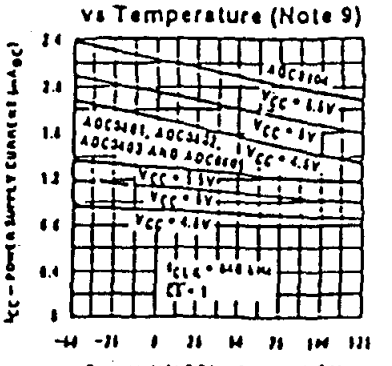
Effect of Unadjusted Offset Error vs. $V_{REF}/2$ Voltage



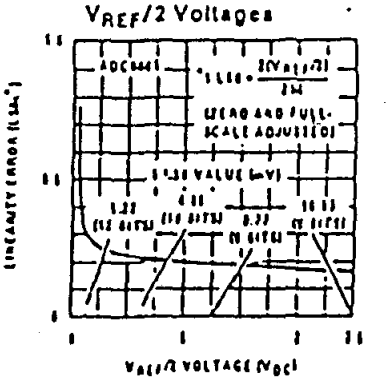
Output Current vs Temperature



Power Supply Current vs Temperature (Note 9)

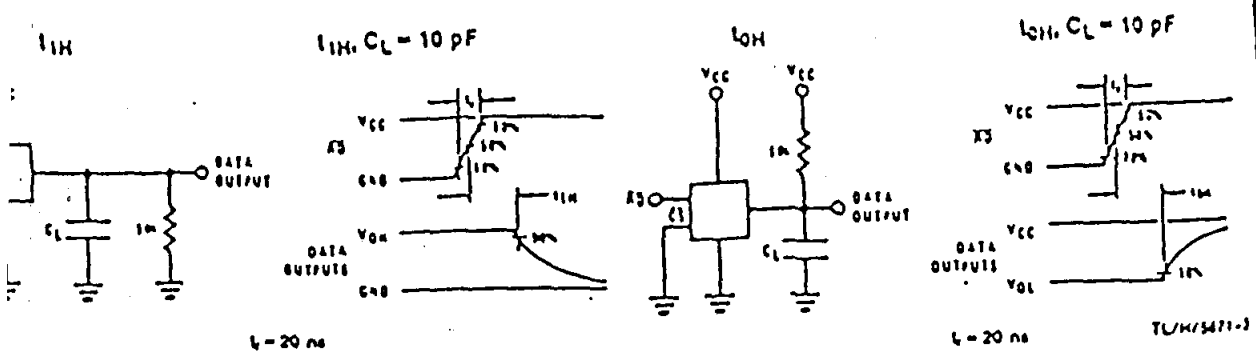


Linearity Error at Low $V_{REF}/2$ Voltages

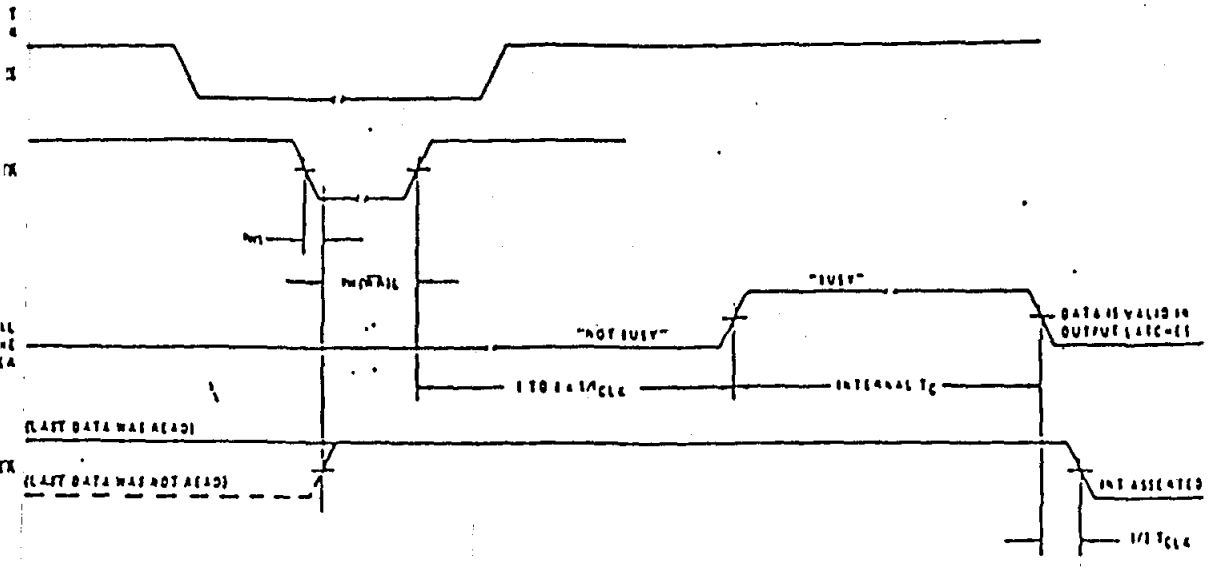


TL/H/5471-2

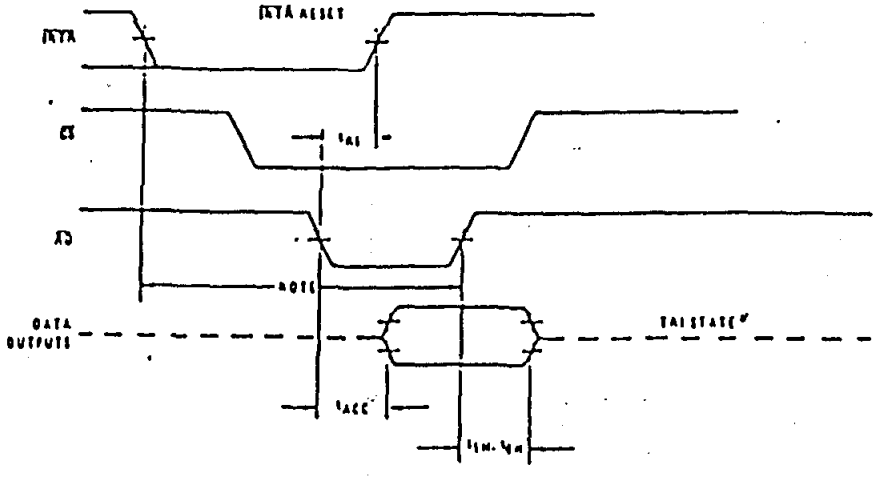
ATE Test Circuits and Waveforms



g Diagrams (All timing is measured from the 50% voltage points)



Output Enable and Reset $\overline{INTR}$

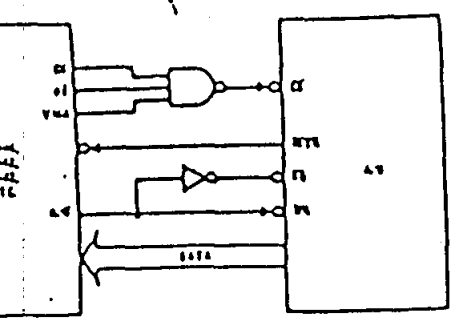


Note: Read strobe must occur 8 clock periods ($8/f_{CLK}$) after assertion of interrupt to guarantee reset of $\overline{INTR}$.

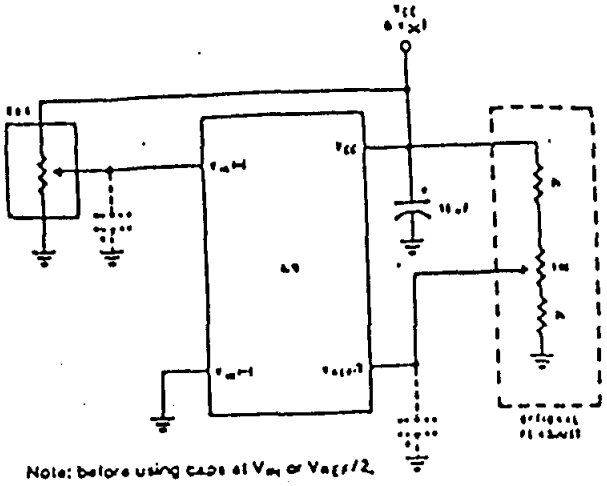
TL/H/5471-4

Applications (Continued)

6800 Interface

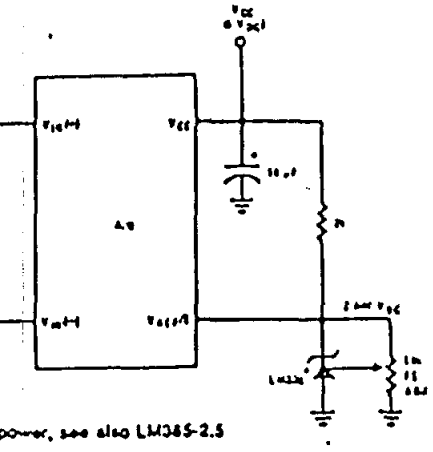


Ratiometric with Full-Scale Adjust



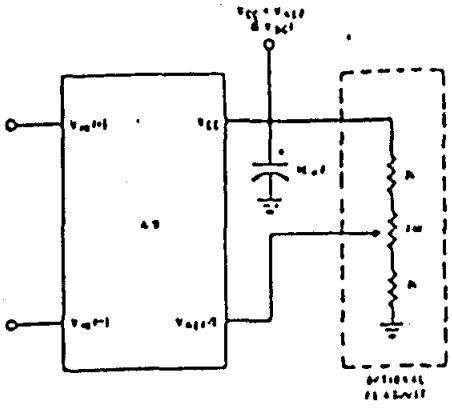
Note: before using taps at V_{IN} or $V_{REF}/2$, see section 2.3.2 Input Bypass Capacitors.

Absolute with a 2.500V Reference

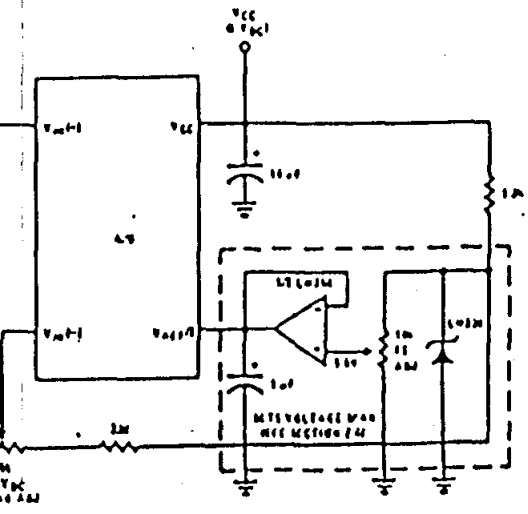


power, see also LM385-2.5

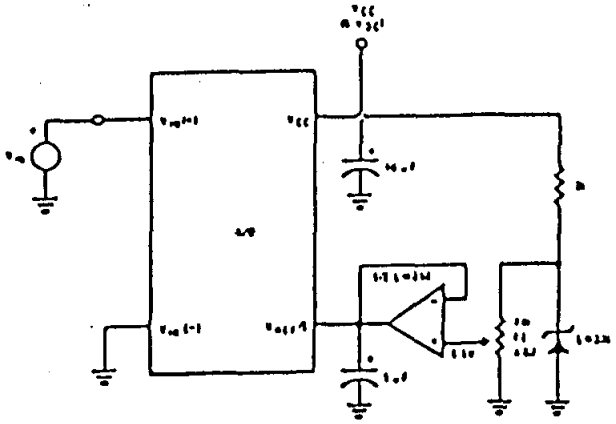
Absolute with a 5V Reference



Zero-Shift and Span Adjust: $2V \leq V_{IN} \leq 5V$



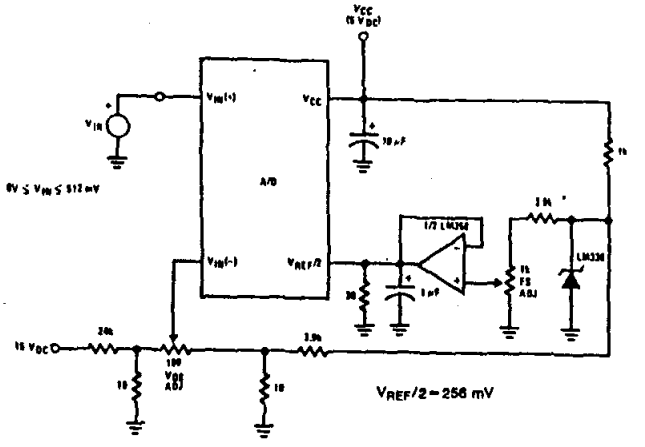
Span Adjust: $0V \leq V_{IN} \leq 3V$



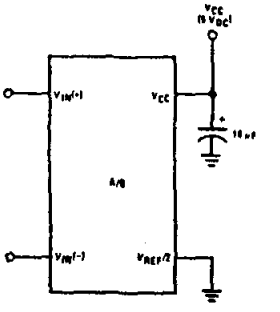
TL/H/5471-5

Typical Applications (Continued)

Directly Converting a Low-Level Signal



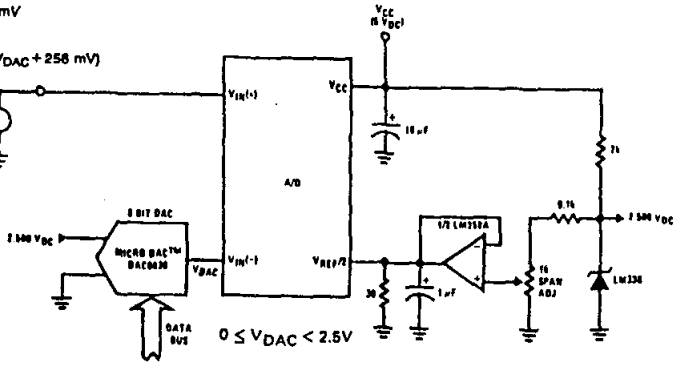
A µP Interfaced Comparator



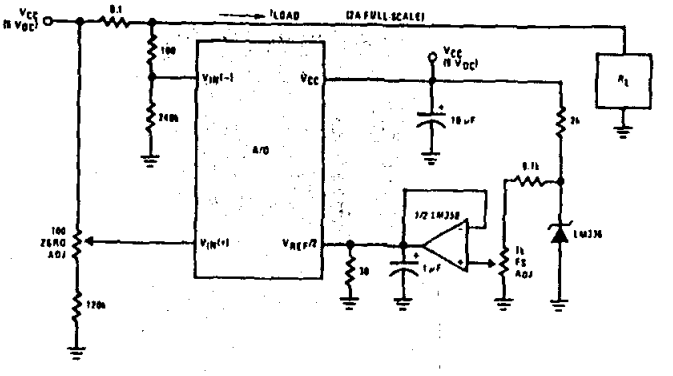
For: $V_{IN}(+) > V_{IN}(-)$
Output = FF_{HEX}
For: $V_{IN}(+) < V_{IN}(-)$
Output = 00_{HEX}

1 mV Resolution with µP Controlled Range

$V_{REF}/2$ = 128 mV
1 LSB = 1 mV
$V_{DAC} \leq V_{IN} \leq (V_{DAC} + 256\ mV)$



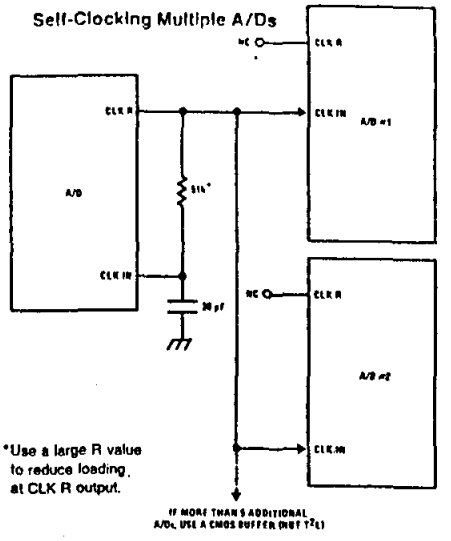
Digitizing a Current Flow



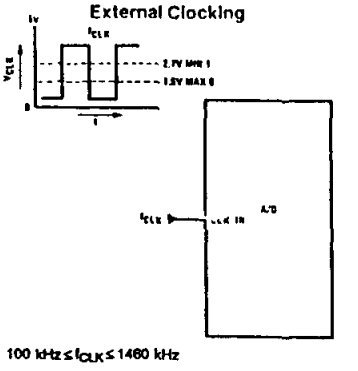
TL/H/5671-6

Typical Applications (Continued)

Self-Clocking Multiple A/Ds

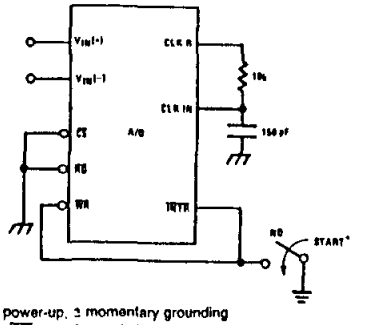


External Clocking



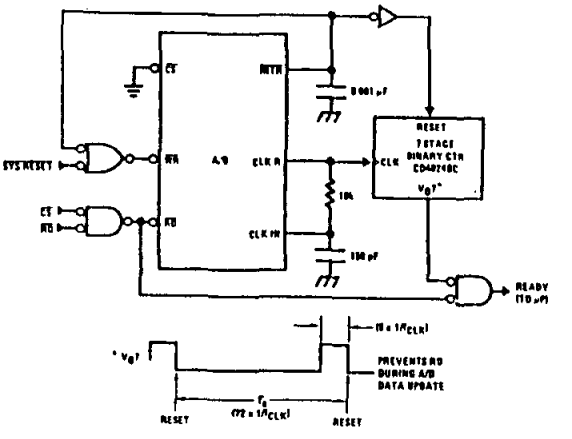
100 kHz ≤ f_{CLK} ≤ 1460 kHz

Self-Clocking in Free-Running Mode

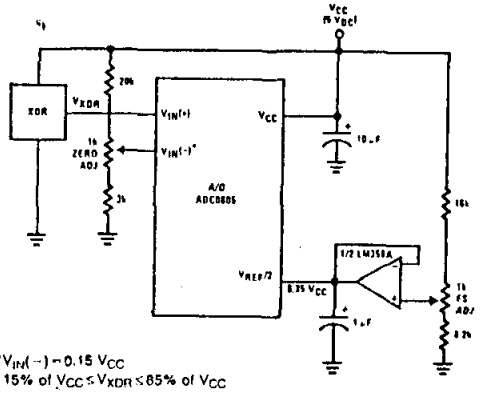


*After power-up, a momentary grounding of the $\overline{WR}$ input is needed to guarantee operation.

µP Interface for Free-Running A/D

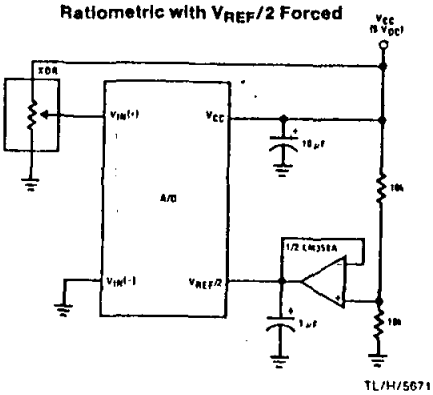


Operating with "Automotive" Ratiometric Transducers



*$V_{IN}(-) = 0.15\ V_{CC}$
15% of $V_{CC} \leq V_{XDR} \leq 85\%$ of V_{CC}

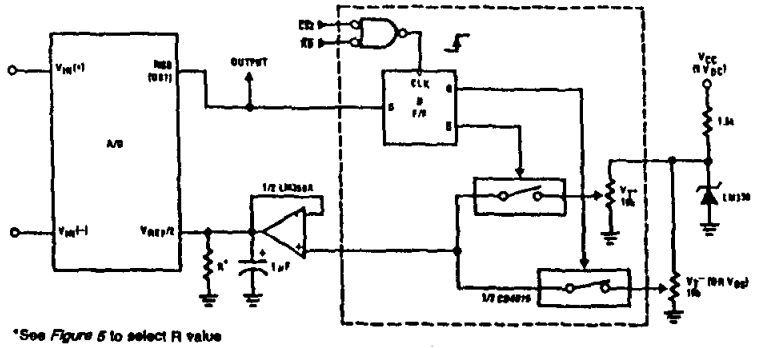
Ratiometric with $V_{REF}/2$ Forced



TL/H/5671–7

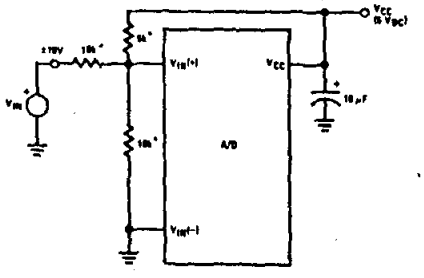
Typical Applications (Continued)

μP Compatible Differential-Input Comparator with Pre-Set V_{OS} (with or without Hysteresis)



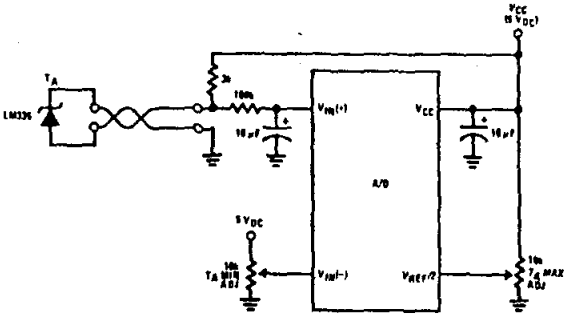
*See *Figure 5* to select R value
DB7 = "1" for $V_{IN}(+) > V_{IN}(-) + (V_{REF}/2)$
Omit circuitry within the dotted area if hysteresis is not needed

Handling ± 10V Analog Inputs

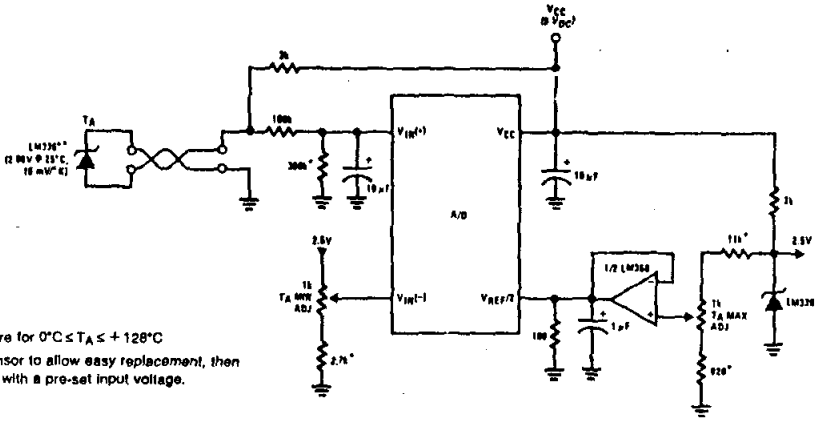


*Beckman Instruments #694-3-R10K resistor array

Low-Cost, μP Interfaced, Temperature-to-Digital Converter



μP Interfaced Temperature-to-Digital Converter

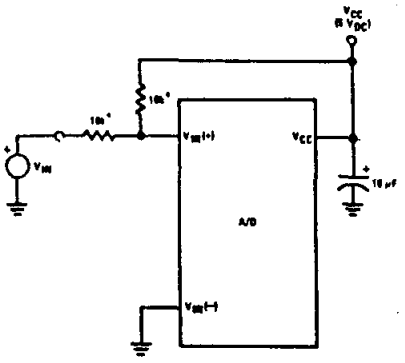


*Circuit values shown are for 0°C ≤ T_A ≤ +128°C
**Can calibrate each sensor to allow easy replacement, then A/D can be calibrated with a pre-set input voltage.

TL/H/5671–8

Typical Applications (Continued)

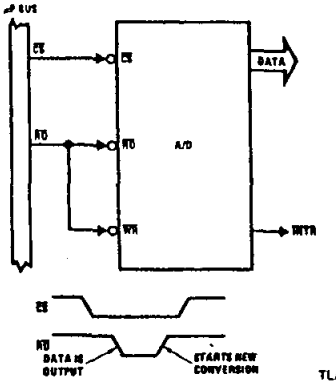
Handling ±5V Analog Inputs



TL/H/5671–33

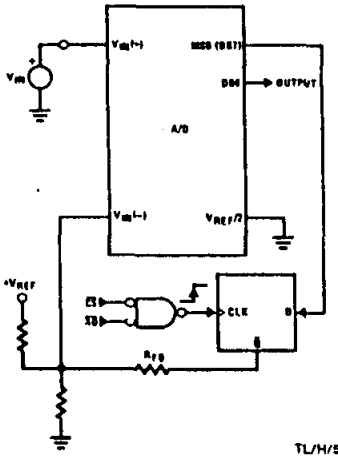
*Beckman Instruments # 694-3-R10K resistor array

Read-Only Interface



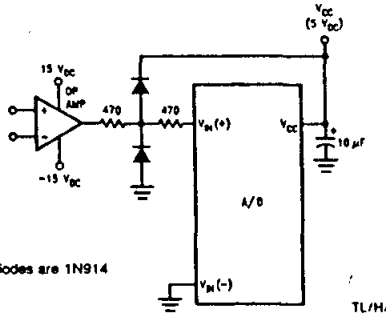
TL/H/5671–34

µP Interfaced Comparator with Hysteresis



TL/H/5671–35

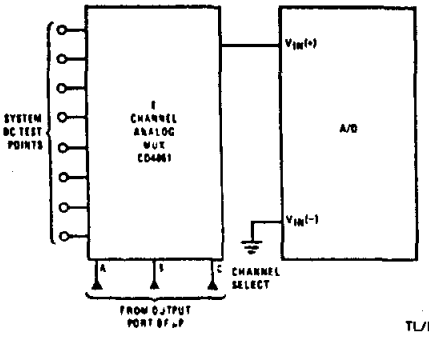
Protecting the Input



Diodes are 1N914

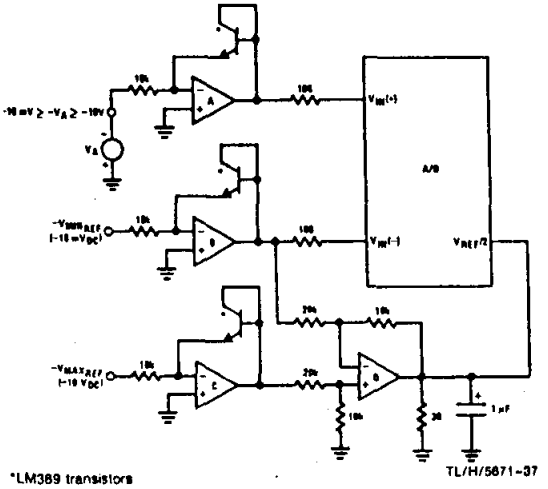
TL/H/5671–9

Analog Self-Test for a System



TL/H/5671–36

A Low-Cost, 3-Decade Logarithmic Converter



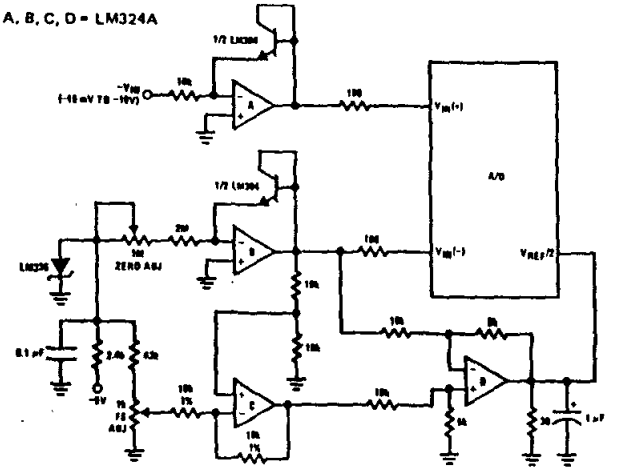
*LM389 transistors

A, B, C, D = LM324A quad op amp

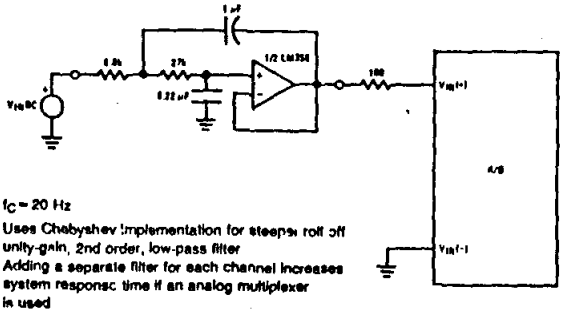
TL/H/5671–37

Typical Applications (Continued)

3-Decade Logarithmic A/D Converter



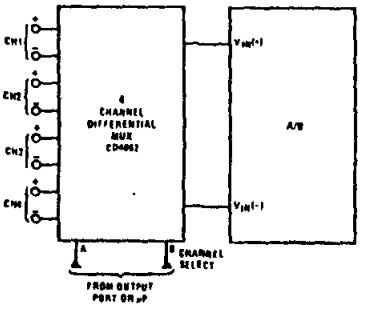
Noise Filtering the Analog Input



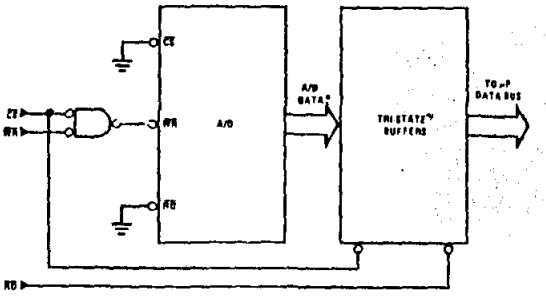
f_C = 20 Hz

Uses Chebyshev implementation for steeper roll off unity-gain, 2nd order, low-pass filter
Adding a separate filter for each channel increases system response time if an analog multiplexer is used

Multiplexing Differential Inputs

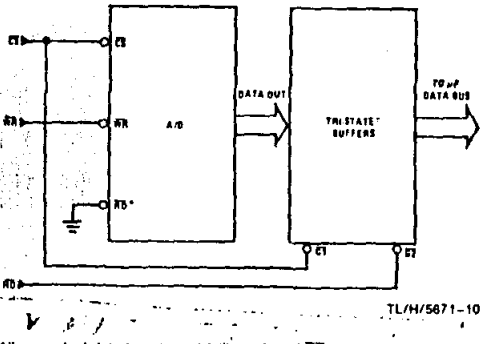


Output Buffers with A/D Data Enabled



*A/D output data is updated 1 CLK period prior to assertion of $\overline{INTR}$

Increasing Bus Drive and/or Reducing Time on Bus

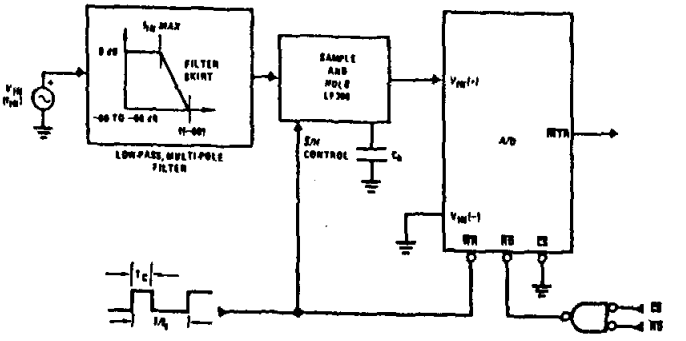


*Allows output data to set-up at falling edge of $\overline{CS}$

TL/H/5671–10

Typical Applications (Continued)

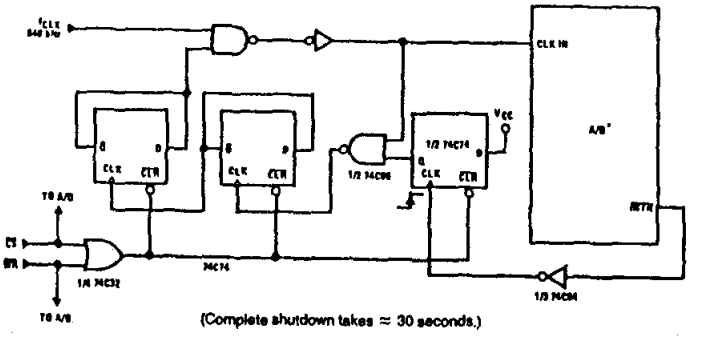
Sampling an AC Input Signal



Note 1: Oversample whenever possible [keep $f_S > 2(f_{-60})$] to eliminate input frequency folding (aliasing) and to allow for the skirt response of the filter.

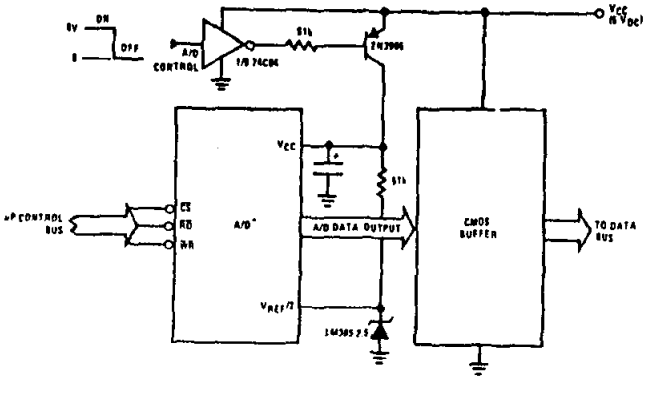
Note 2: Consider the amplitude errors which are introduced within the passband of the filter.

70% Power Savings by Clock Gating



(Complete shutdown takes ≈ 30 seconds.)

Power Savings by A/D and V_{REF} Shutdown



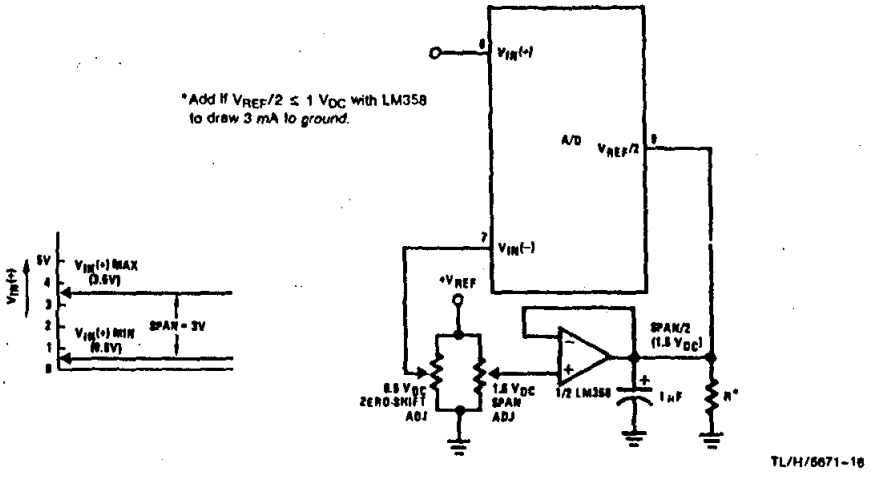
TL/H/5671–11

*Use ADC0801, 02, 03 or 05 for lowest power consumption.

Note: Logic inputs can be driven to V_{CC} with A/D supply at zero volts.

Buffer prevents data bus from overdriving output of A/D when in shutdown mode.

Functional Description (Continued)



TL/H/5671–16

a) Analog Input Signal Example

b) Accommodating an Analog Input from 0.5V (Digital Out = 00_{HEX}) to 3.5V (Digital Out = FF_{HEX})

FIGURE 5. Adapting the A/D Analog Input Voltages to Match an Arbitrary Input Signal Range

2.4.2 Reference Accuracy Requirements

The converter can be operated in a ratiometric mode or an absolute mode. In ratiometric converter applications, the magnitude of the reference voltage is a factor in both the output of the source transducer and the output of the A/D converter and therefore cancels out in the final digital output code. The ADC0805 is specified particularly for use in ratiometric applications with no adjustments required. In absolute conversion applications, both the initial value and the temperature stability of the reference voltage are important factors in the accuracy of the A/D converter. For $V_{REF}/2$ voltages of 2.4 V_{DC} nominal value, initial errors of ±10 mV_{DC} will cause conversion errors of ±1 LSB due to the gain of 2 of the $V_{REF}/2$ input. In reduced span applications, the initial value and the stability of the $V_{REF}/2$ input voltage become even more important. For example, if the span is reduced to 2.5V, the analog input LSB voltage value is correspondingly reduced from 20 mV (5V span) to 10 mV and 1 LSB at the $V_{REF}/2$ input becomes 5 mV. As can be seen, this reduces the allowed initial tolerance of the reference voltage and requires correspondingly less absolute change with temperature variations. Note that spans smaller than 2.5V place even tighter requirements on the initial accuracy and stability of the reference source.

In general, the magnitude of the reference voltage will require an initial adjustment. Errors due to an improper value of reference voltage appear as full-scale errors in the A/D transfer function. IC voltage regulators may be used for references if the ambient temperature changes are not excessive. The LM336B 2.5V IC reference diode (from National Semiconductor) has a temperature stability of 1.8 mV typ (6 mV max) over $0°C \leq T_A \leq +70°C$. Other temperature range parts are also available.

2.5 Errors and Reference Voltage Adjustments

2.5.1 Zero Error

The zero of the A/D does not require adjustment. If the minimum analog input voltage value, $V_{IN(MIN)}$, is not ground, a zero offset can be done. The converter can be made to output 0000 0000 digital code for this minimum input voltage by biasing the A/D $V_{IN}(-)$ input at this $V_{IN(MIN)}$ value (see Apolications section). This utilizes the differential mode operation of the A/D.

The zero error of the A/D converter relates to the location of the first riser of the transfer function and can be measured by grounding the $V_{IN}(-)$ input and applying a small magnitude positive voltage to the $V_{IN}(+)$ input. Zero error is the difference between the actual DC input voltage that is necessary to just cause an output digital code transition from 0000 0000 to 0000 0001 and the ideal ½ LSB value (½ LSB = 9.8 mV for $V_{REF}/2 = 2.500\ V_{DC}$).

2.5.2 Full-Scale

The full-scale adjustment can be made by applying a differential input voltage that is 1½ LSB less than the desired analog full-scale voltage range and then adjusting the magnitude of the $V_{REF}/2$ input (pin 9 or the V_{CC} supply if pin 9 is not used) for a digital output code that is just changing from 1111 1110 to 1111 1111.

National Semiconductor Corporation

DAC0808, DAC0807, DAC0806 8-Bit D/A Converters

General Description

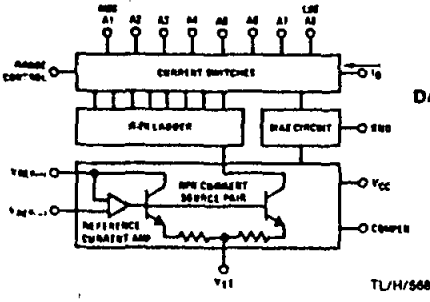
The DAC0808 series is an 8-bit monolithic digital-to-analog converter (DAC) featuring a full scale output current settling time of 150 ns while dissipating only 33 mW with ±5V supplies. No reference current (I_{REF}) trimming is required for most applications since the full scale output current is typically ±1 LSB of 255 I_{REF}/ 256. Relative accuracies of better than ±0.19% assure 8-bit monotonicity and linearity while zero level output current of less than 4 μA provides 8-bit zero accuracy for $I_{REF} \geq 2$ mA. The power supply currents of the DAC0808 series are independent of bit codes, and exhibits essentially constant device characteristics over the entire supply voltage range.

The DAC0808 will interface directly with popular TTL, DTL or CMOS logic levels, and is a direct replacement for the MC1508/MC1408. For higher speed applications, see DAC0800 data sheet.

Features

- Relative accuracy: ±0.19% error maximum (DAC0808)
- Full scale current match: ±1 LSB typ
- 7 and 6-bit accuracy available (DAC0807, DAC0806)
- Fast settling time: 150 ns typ
- Noninverting digital inputs are TTL and CMOS compatible
- High speed multiplying input slew rate: 8 mA/μs
- Power supply voltage range: ±4.5V to ±18V
- Low power consumption: 33 mW @ ±5V

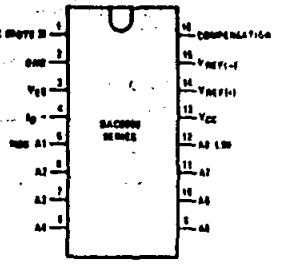
Block and Connection Diagrams



TL/H/5687–1

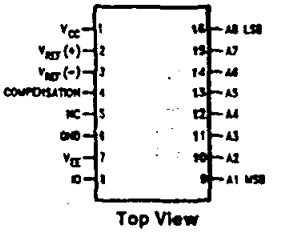
Order Number DAC0808, DAC0807, or DAC0806 See NS Package Number J16A, M16A or N16A

Dual-In-Line Package



TL/H/5687–2

Small-Outline Package



TL/H/5687–13

Top View

Ordering Information

ACCURACY	OPERATING TEMPERATURE RANGE	ORDER NUMBERS				
		J PACKAGE (J16A)*		N PACKAGE (N16A)*		SO PACKAGE (M16A)
8-bit	$-55°C \leq T_A \leq -125°C$	DAC0808LJ	MC1508L8			
8-bit	$0°C \leq T_A \leq -75°C$	DAC0808LCJ	MC1408L8	DAC0808LCN	MC1408P8	DAC0808LCM
7-bit	$0°C \leq T_A \leq -75°C$	DAC0807LCJ	MC1408L7	DAC0807LCN	MC1408P7	DAC0807LCM
6-bit	$0°C \leq T_A \leq -75°C$	DAC0806LCJ	MC1408L6	DAC0806LCN	MC1408P6	DAC0806LCM

*Note. Devices may be ordered by using either order number.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Power Supply Voltage	
V_{CC}	+18 V_{DC}
V_{EE}	−18 V_{DC}
Digital Input Voltage, V5–V12	−10 V_{DC} to +18 V_{DC}
Applied Output Voltage, V_O	−11 V_{DC} to +18 V_{DC}
Reference Current, I_{14}	5 mA
Reference Amplifier Inputs, V14, V15	V_{CC}, V_{EE}
Power Dissipation (Note 3)	1000 mW
ESD Susceptibility (Note 4)	TBD
Storage Temperature Range	−65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	
Dual-In-Line Package (Plastic)	260°C
Dual-In-Line Package (Ceramic)	300°C
Surface Mount Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

Operating Ratings

Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
DAC0808L	−55°C ≤ T_A ≤ +125°C
DAC0808LC Series	0 ≤ T_A ≤ +75°C

Electrical Characteristics

(V_{CC} = 5V, V_{EE} = −15 V_{DC}, $V_{REF}/R14$ = 2 mA, DAC0808: T_A = −55°C to +125°C, DAC0808C, DAC0807C, DAC0806C, T_A = 0°C to +75°C, and all digital inputs at high logic level unless otherwise noted.)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
E_r	Relative Accuracy (Error Relative to Full Scale I_O)	*(Figure 4)*				%
	DAC0808L (LM1508-8), DAC0808LC (LM1408-8)				±0.19	%
	DAC0807LC (LM1408-7), *(Note 5)*				±0.39	%
	DAC0806LC (LM1408-6), *(Note 5)*				±0.78	%
	Setting Time to Within ½ LSB (Includes t_{PLH})	T_A = 25°C *(Note 6)*, *(Figure 5)*		150		ns
t_{PLH}, t_{PHL}	Propagation Delay Time	T_A = 25°C, *(Figure 5)*		30	100	ns
TCI_O	Output Full Scale Current Drift			±20		ppm/°C
MSB	*Digital Input Logic Levels*	*(Figure 3)*				
V_{IH}	High Level, Logic "1"		2			V_{DC}
V_{IL}	Low Level, Logic "0"				0.8	V_{DC}
MSB	Digital Input Current	*(Figure 3)*				
	High Level	V_{IH} = 5V		0	0.040	mA
	Low Level	V_{IL} = 0.8V		−0.003	−0.8	mA
I_{15}	*Reference Input Bias Current*	*(Figure 3)*		−1	−3	μA
	Output Current Range	*(Figure 3)*				
		V_{EE} = −5V	0	2.0	2.1	mA
		V_{EE} = −15V, T_A = 25°C	0	2.0	4.2	mA
I_O	*Output Current*	V_{REF} = 2.000V, R14 = 1000Ω, *(Figure 3)*	1.9	1.99	2.1	mA
	Output Current, All Bits Low	*(Figure 3)*		0	4	μA
	Output Voltage Compliance *(Note 2)*	$E_r \le 0.19\%$, T_A = 25°C				
	V_{EE} = −5V, I_{REF} = 1 mA				−0.55, +0.4	V_{DC}
	V_{EE} Below −10V				−5.0, +0.4	V_{DC}

Electrical Characteristics (Continued)

(V_{CC} = 5V, V_{EE} = −15 V_{DC}, $V_{REF}/R14$ = 2 mA, DAC0808: T_A = −55°C to +125°C, DAC0808C, DAC0807C, DAC0806C, T_A = 0°C to +75°C, and all digital inputs at high logic level unless otherwise noted.)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
SR_{IREF}	Reference Current Slew Rate	*(Figure 6)*	4	8		mA/μs
	Output Current Power Supply Sensitivity	$-5V \le V_{EE} \le -16.5V$		0.05	2.7	μA/V
	Power Supply Current (All Bits Low)	*(Figure 3)*				
I_{CC}				2.3	22	mA
I_{EE}				−4.3	−13	mA
	Power Supply Voltage Range	T_A = 25°C, *(Figure 3)*				
V_{CC}			4.5	5.0	5.5	V_{DC}
V_{EE}			−4.5	−15	−16.5	V_{DC}
	Power Dissipation					
	All Bits Low	V_{CC} = 5V, V_{EE} = −5V		33	170	mW
		V_{CC} = 5V, V_{EE} = −15V		106	305	mW
	All Bits High	V_{CC} = 15V, V_{EE} = −5V		90		mW
		V_{CC} = 15V, V_{EE} = −15V		160		mW

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 2: Range control is not required.

Note 3: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation at any temperature is $P_D = (T_{JMAX} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For this device, T_{JMAX} = 125°C, and the typical junction-to-ambient thermal resistance of the dual-in-line J package when the board mounted is 100°C/W. For the dual-in-line N package, this number increases to 175°C/W and for the small outline M package this number is 100°C/W.

Note 4: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 5: All current switches are tested to guarantee at least 50% of rated current.

Note 6: All bits switched.

Note 7: Pin-out numbers for the DAL080X represent the dual-in-line package. The small outline package pinout differs from the dual-in-line package.

Typical Application

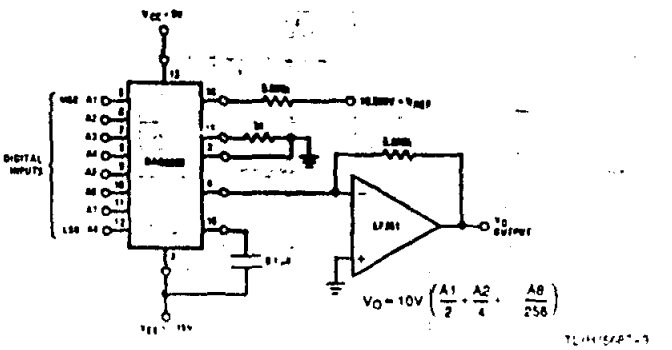


FIGURE 1. ± 10V Output Digital to Analog Converter (Note 7)