LAMPIRAN

```
PORT_A          EQU 2000H
PORT_B          EQU 2001H
PORT_C          EQU 2002H
CONTROL_REG     EQU 2003H
WAIT            EQU 20H
DIGIT1          EQU 21H
DIGIT2          EQU 22H
DIGIT3          EQU 23H
DIGIT4          EQU 24H
INPUT           EQU 25H
COUNTER         EQU 26H
BUFFER          EQU 27H
DATA_COS0       EQU 28H
DATA            EQU 29H
KEY_TEST        EQU 30H
DIGIT5          EQU 31H
REPEAT          EQU 32H
MAX_VAL         EQU 35H
KEY_BUFFER      EQU 36H
ENTRY           EQU 37H
READ_OUT        EQU 38H
LOOP            EQU 39H

            ORG 0000H
            AJMP MAIN

            ORG 100H

MAIN:       SETB EA
            SETB ET0
            SETB EX1

            CLR RS0
            CLR RS1

;-------------------------------------------------------------------------

MENU_SELECT:    MOV DIGIT3,#0H
            MOV DIGIT2,#0H
            MOV DIGIT1,#0H

            ACALL REFRESH_DISP

            MOV A,KEY_TEST
            CJNE A,#10,COS0     ; A = 10  SET_COS0

SET_COS0:       ACALL BCD2HEX
            ACALL BREEZE_BLINK
            MOV A,KEY_TEST
            CJNE A,#15,SET_COS0

            MOV KEY_TEST,#0
            AJMP MENU_SELECT

;-------------------------------------------------------------------------
COS0:       MOV A,KEY_TEST
            CJNE A,#11,SET_UP_DISP   ; A = 11  COS0_MEASUREMENT
            AJMP COS0_MEASUREMENT
```

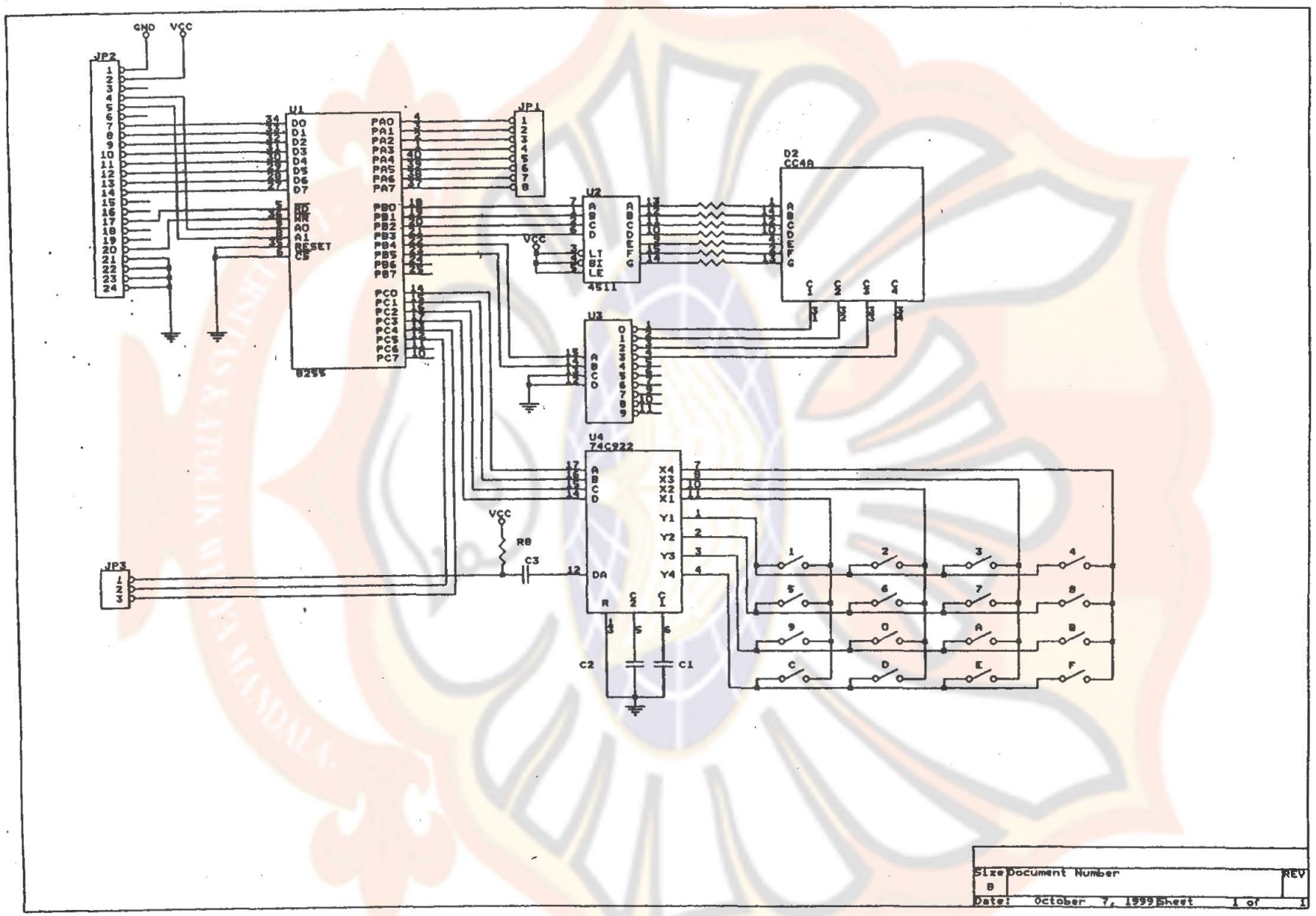
```
;-------------------------------------------------------------------------
SET_UP_DISP:      MOV A,KEY_TEST
          CJNE A,#12,OFF_RELAY    ; A = 12  SET_UP_DISP
          AJMP  SETUP_DISP

;-------------------------------------------------------------------------
OFF_RELAY:        MOV A,KEY_TEST
          CJNE A,#14,PROCESS

          MOV DPTR,#PORT_A
          MOV A,#0
          MOVX @DPTR,A

          AJMP COS0_MEASUREMENT

;-------------------------------------------------------------------------
PROCESS:          CJNE A,#13,MENU_SELECT   ; A = 13 COS0 ADJUSTMENT PROCESS

INTAKE:           ACALL P1_READ
          MOV INPUT,DATA
          ACALL HEX2BCD
          ACALL REFRESH_DISP

          ACALL P1_READ
          MOV A,DATA_COS0
          SUBB A,DATA
          JC RESTORE

          AJMP COS0_MEASUREMENT

RESTORE:          MOV DPTR,#PORT_A
          MOV A,#00000001B    ;1uF
          MOVX @DPTR,A

          ACALL SCAN_DELAY

INTAKE2:          ACALL P1_READ
          MOV INPUT,DATA
          ACALL HEX2BCD
          ACALL REFRESH_DISP

          ACALL P1_READ
          MOV A,DATA_COS0
          SUBB A,DATA
          JC RESTORE2

          AJMP COS0_MEASUREMENT

RESTORE2:         MOV DPTR,#PORT_A
          MOV A,#00000010B    ;2uF
          MOVX @DPTR,A

          ACALL SCAN_DELAY

INTAKE3:          ACALL P1_READ
          MOV INPUT,DATA
          ACALL HEX2BCD
```

```
            ACALL REFRESH_DISP

            ACALL P1_READ
            MOV A,DATA_COS0
            SUBB A,DATA
            JC RESTORE3

            AJMP COS0_MEASUREMENT

RESTORE3:       MOV DPTR,#PORT_A
            MOV A,#00000011B    ;3uF
            MOVX @DPTR,A

            ACALL SCAN_DELAY

INTAKE4:        ACALL P1_READ
            MOV INPUT,DATA
            ACALL HEX2BCD
            ACALL REFRESH_DISP

            ACALL P1_READ
            MOV A,DATA_COS0
            SUBB A,DATA
            JC RESTORE4

            AJMP COS0_MEASUREMENT

RESTORE4:       MOV DPTR,#PORT_A
            MOV A,#00000101B    ;4uF
            MOVX @DPTR,A

            ACALL SCAN_DELAY

INTAKE5:        ACALL P1_READ
            MOV INPUT,DATA
            ACALL HEX2BCD
            ACALL REFRESH_DISP

            ACALL P1_READ
            MOV A,DATA_COS0
            SUBB A,DATA
            JC RESTORE5

            AJMP COS0_MEASUREMENT

RESTORE5:       MOV DPTR,#PORT_A
            MOV A,#00000110B    ;5uF
            MOVX @DPTR,A

            ACALL SCAN_DELAY

INTAKE6:        ACALL P1_READ
            MOV INPUT,DATA
            ACALL HEX2BCD
            ACALL REFRESH_DISP

            ACALL P1_READ
            MOV A,DATA_COS0
```

```
            SUBB A,DATA
            JC RESTORE6

            AJMP COS0_MEASUREMENT

RESTORE6:   MOV DPTR,#PORT_A
            MOV A,#00001100B    ;6uF
            MOVX @DPTR,A

            ACALL SCAN_DELAY

INTAKE7:    ACALL P1_READ
            MOV INPUT,DATA
            ACALL HEX2BCD
            ACALL REFRESH_DISP

            ACALL P1_READ
            MOV A,DATA_COS0
            SUBB A,DATA
            JC RESTORE7

            AJMP COS0_MEASUREMENT

RESTORE7:   MOV DPTR,#PORT_A
            MOV A,#00001101B    ;7uF
            MOVX @DPTR,A

            ACALL SCAN_DELAY

INTAKE8:    ACALL P1_READ
            MOV INPUT,DATA
            ACALL HEX2BCD
            ACALL REFRESH_DISP

            ACALL P1_READ
            MOV A,DATA_COS0
            SUBB A,DATA
            JC RESTORE8

            AJMP COS0_MEASUREMENT

RESTORE8:   MOV DPTR,#PORT_A
            MOV A,#00001110B    ;8uF
            MOVX @DPTR,A

            ACALL SCAN_DELAY

INTAKE9:    ACALL P1_READ
            MOV INPUT,DATA
            ACALL HEX2BCD
            ACALL REFRESH_DISP

            ACALL P1_READ
            MOV A,DATA_COS0
            SUBB A,DATA
            JC RESTORE9

            AJMP COS0_MEASUREMENT
```

```
RESTORE9:       MOV DPTR,#PORT_A
                MOV A,#00001111B
                MOVX @DPTR,A

                AJMP COS0_MEASUREMENT
;-------------------------------------------------------------------------------
COS0_MEASUREMENT:   MOV B,READ_OUT
                ACALL REFRESH_DISP
                MOV A,KEY_TEST
                CJNE A,#15,COS0_MEASUREMENT
                AJMP MENU_SELECT


SETUP_DISP:     MOV INPUT,DATA_COS0
                ACALL HEX2BCD
                ACALL REFRESH_DISP
                MOV A,KEY_TEST
                CJNE A,#15,SETUP_DISP
                AJMP MENU_SELECT

;-------------------------------------------------------------------------------
DELAY_LOOP:     PUSH DPH
                PUSH DPL

DEL_LOOP:       DEC R1
                NOP
                NOP
                NOP
                CJNE R1,#0H,DEL_LOOP

                POP DPL
                POP DPH
                RET

;-------------------------------------------------------------------------------
DELAY_5S:       PUSH DPH
                PUSH DPL

                MOV R7,#0FH
DEL2:               MOV A,#0FFH
DEL3:               MOV B,#0FFH
                DJNZ B,$
                DJNZ ACC,DEL3
                DJNZ R7,DEL2

                POP DPL
                POP DPH
                RET

;-------------------------------------------------------------------------------
DELAY_2S:       PUSH DPH
                PUSH DPL

                MOV R7,#0FH
DEL4:               MOV A,#0FH
DEL5:               MOV B,#0FFH
                DJNZ B,$
```

```
            DJNZ ACC,DEL5
            DJNZ R7,DEL4

            POP DPL
            POP DPH
            RET
;-------------------------------------------------------------------------
DELAY_1S:       PUSH DPH
            PUSH DPL

            MOV R7,#02H
DEL6:           MOV A,#02H
DEL7:           MOV B,#0FAH
            DJNZ B,$
            DJNZ ACC,DEL7
            DJNZ R7,DEL6

            POP DPL
            POP DPH
            RET

;-------------------------------------------------------------------------
BREEZE_BLINK:     PUSH DPH
            PUSH DPL

            MOV REPEAT,#03DH
F:           ACALL REFRESH_DISP
            DJNZ REPEAT,F

            ACALL DELAY_2S

            MOV REPEAT,#0DDH
G:           ACALL REFRESH_DISP_OFF
            DJNZ REPEAT,G

            POP DPL
            POP DPH
            RET
;-------------------------------------------------------------------------
SCAN_DELAY:       PUSH DPH
            PUSH DPL

            MOV LOOP,#5

LOOP_DEC:       MOV COUNTER,#255
SCAN:           ACALL P1_READ
            ACALL REFRESH_DISP
            DJNZ COUNTER,SCAN
            DJNZ LOOP,LOOP_DEC

            POP DPL
            POP DPH
            RET
;-------------------------------------------------------------------------

            END
```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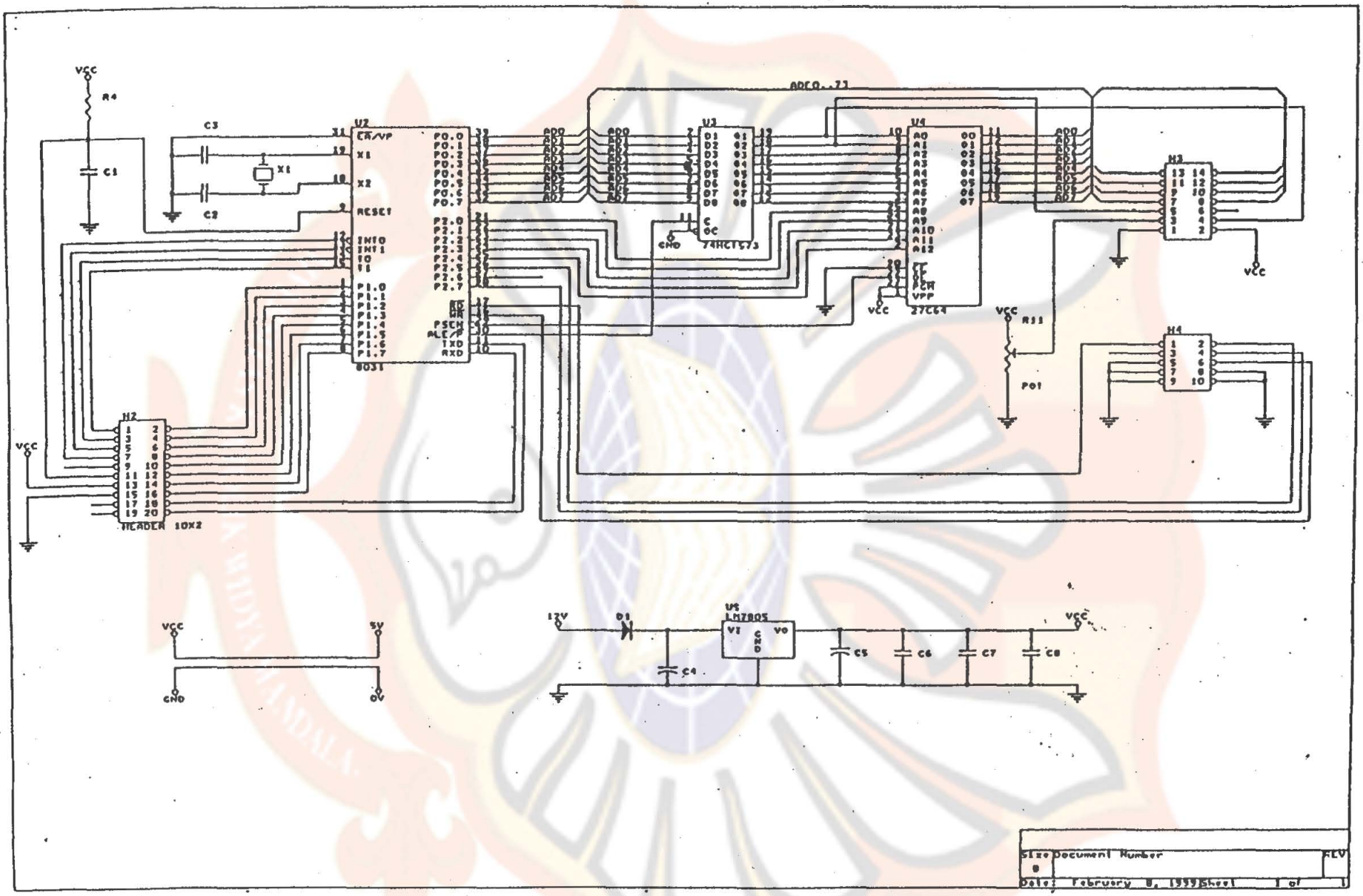
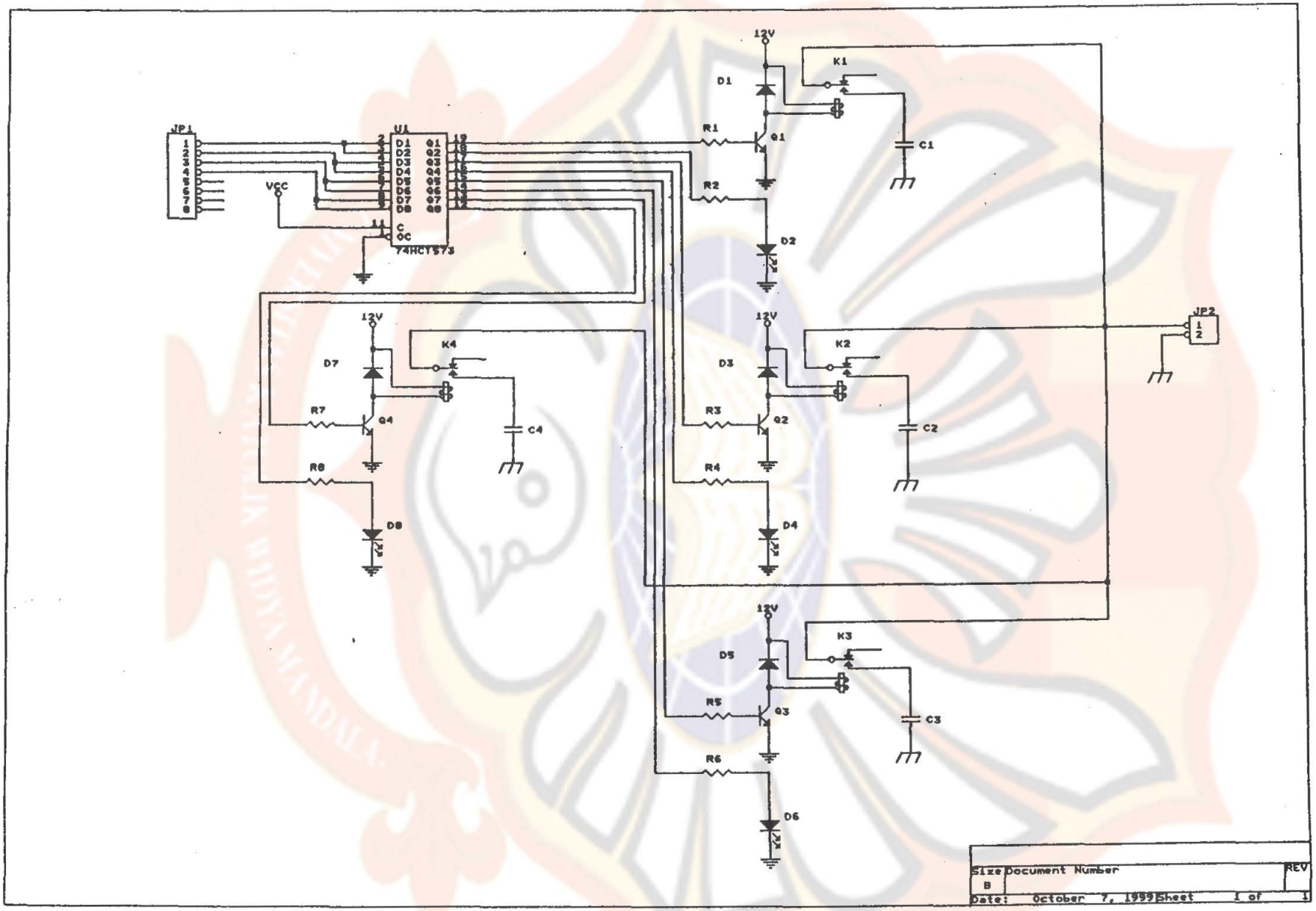
JP2
U1
8255
JP1
U2
4511
VCC
D2
CC4A
U3
U4
74C922
VCC
R8
C3
JP3
C2
C1
Size
B
Document Number
REV
Date: October 7, 1999 Sheet 1 of 1


VCC
R4
C1
C3
C2
X1
U2
8031
RESET
INT0
INT1
T0
T1
P1.0
P1.1
P1.2
P1.3
P1.4
P1.5
P1.6
P1.7
PSEN
ALE/
TXD
RXD
P0.0
P0.1
P0.2
P0.3
P0.4
P0.5
P0.6
P0.7
P2.0
P2.1
P2.2
P2.3
P2.4
P2.5
P2.6
P2.7
ADC0..7
U3
74HCT573
GND
U4
27C64
VPP
R11
P01
H1
H2
HEADER 10X2
H3
H4
5V
0V
12V
D1
U5
LM7805
VI
VO
C4
C5
C6
C7
C8
Size
Document Number
REV
Date: February 8, 1999
Sheet 1 of 1


JP1
U1
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VCC
12V
K1
D1
R1
Q1
C1
R2
D2
JP2
K4
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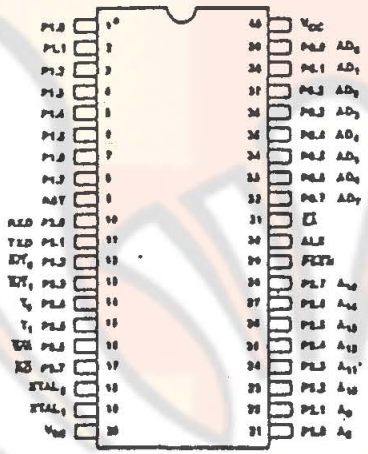
R7
Q4
C4
R8
D8
K2
D3
R3
Q2
C2
R4
D4
K3
D5
R5
Q3
C3
R6
D6
Size
Document Number
REV
Date: October 7, 1999
Sheet 1 of 1

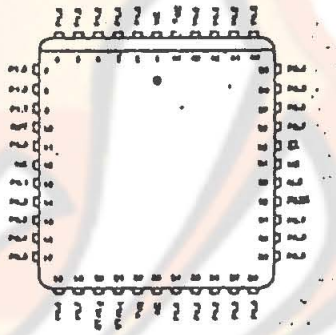
CONNECTION DIAGRAMS
Top View

DIP
80C51BH/80C31BH
80C52T2/80C32T2



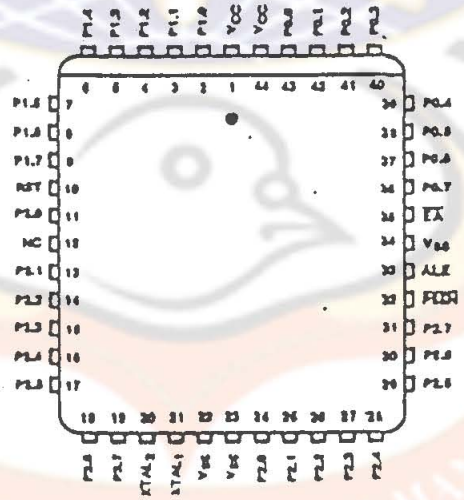
CD00555A

PLCC
80C51BH/80C31BH



CD00844A

PLCC
80C52T2/80C32T2

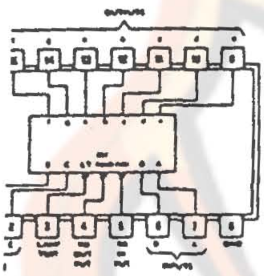


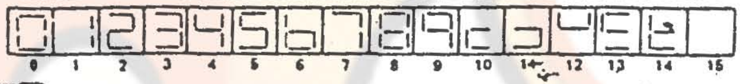
CD00844A

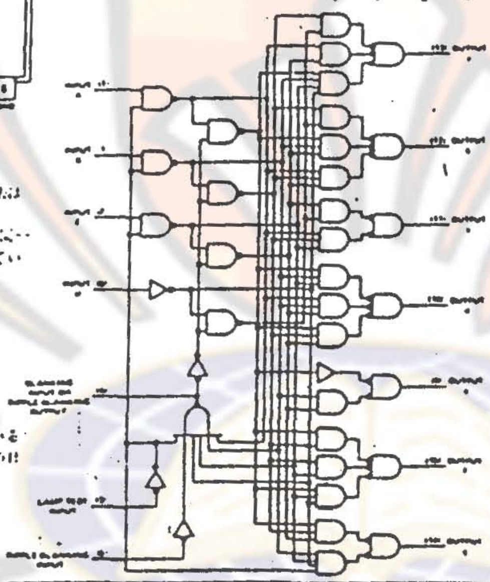
Note: Pin 1 is marked for orientation.

BCD to 7 Segment Decoder, Driver

項目	入力	出力	max/min	N	LS	ALS	ALS 1000	F	S	AS	AC	HC	HCT	単位
[illegible]	A～D	a～g	max	100	100									ns
	RBI		max	100	(100)									ns
Icc	全入力H	全出力Open	max	90	38									mA







* RBI, BI·RBO, LT の使用法は7と同一（7446等か）
6と9の字形が異なるほか，[illegible]
[illegible]

7とはa～gの論理が逆になっている。[illegible]
[illegible]

代替品種
74248

	N	LS	ALS	ALS 1000	F	S	AS		単位
	–	–							μA
	4	1							mA
	40	20							μA
	1.6	0.36							mA

出力電流特性		N	LS	ALS	ALS 1000	F	S	AS	AC	HC	HCT	単位
BI RBO	H →	0.2	50μA									mA
	L →	8	3.2									mA
a～g	H →	0.4	0.1									mA
	L →	6.4	6									mA

社名	記号	N	LS	ALS	ALS 1000	F	S	AS	AC	HC	HCT
FC		●	●								
富士通	MB		●								
日立	HD		●								
松下	DN/MN										
三菱	M	●	●								
MOT	MC/SN	●	●								
NS	DM/MM	●	●								
日電	μPB/D										
RAY											
RCA	CD									●	●
SIG	N	●									
TI	SN	●	●								
東芝	TD/TC										
SGS	T'M										
沖	MSM		●								

National Semiconductor

LM741/LM741A/LM741C/LM741E Operational Amplifier

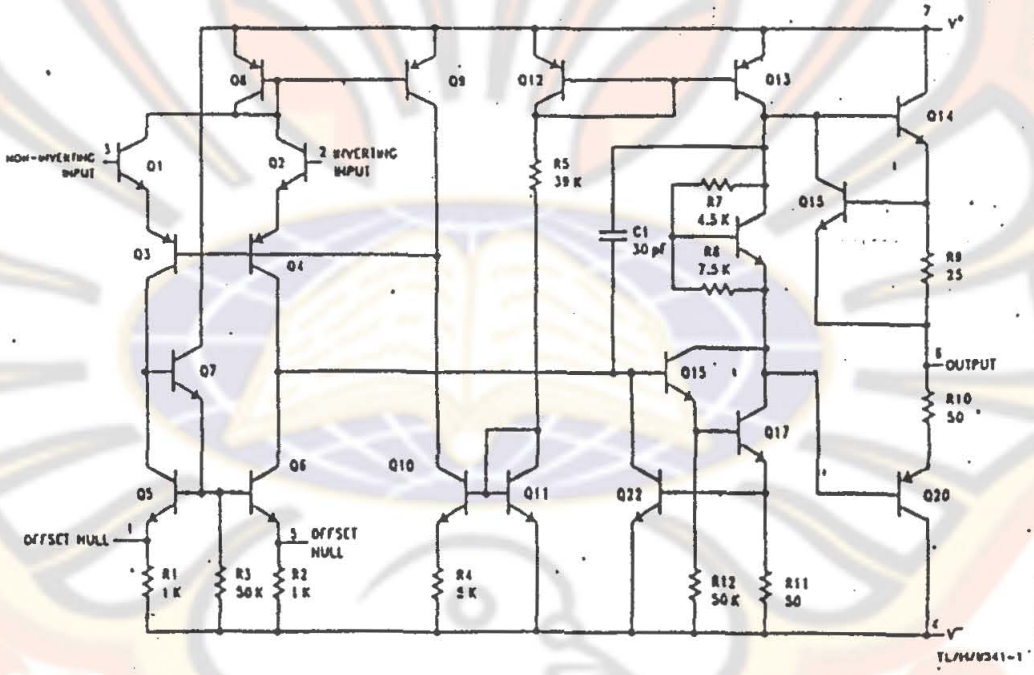
General Description

The LM741 series are general purpose operational amplifiers which feature improved performance over industry standards like the LM709. They are direct, plug-in replacements for the 709C, LM201, MC1439 and 748 in most applications.

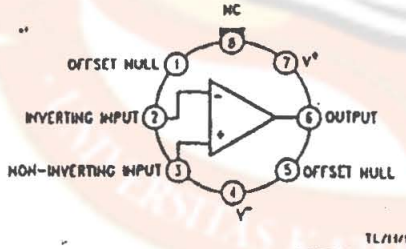
The amplifiers offer many features which make their application nearly foolproof: overload protection on the input and output, no latch-up when the common mode range is exceeded, as well as freedom from oscillations.

The LM741C/LM741E are identical to the LM741/LM741A except that the LM741C/LM741E have their performance guaranteed over a 0°C to +70°C temperature range, instead of −55°C to +125°C.

Schematic and Connection Diagrams (Top Views)

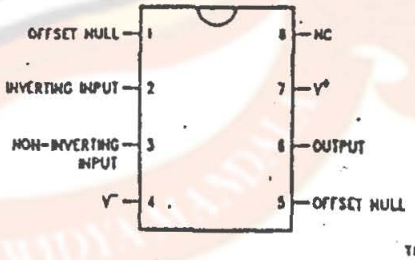


Metal Can Package



Order Number LM741H, LM741AH, LM741CH or LM741EH
See NS Package Number H08C

Dual-In-Line or S.O. Package



Order Number LM741J, LM741AJ, LM741CJ, LM741CM, LM741CN or LM741EN
See NS Package Number J08A, M08A or N08E

Electrical Characteristics (Note 3) (Continued)

Parameter	Conditions	LM741A/LM741E			LM741			LM741C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Output Voltage Swing	$V_S = \pm 20V$										
	$R_L \geq 10\ k\Omega$	± 16									V
	$R_L \geq 2\ k\Omega$	± 15									V
	$V_S = \pm 15V$										
	$R_L \geq 10\ k\Omega$				± 12	± 14		± 12	± 14		V
	$R_L \geq 2\ k\Omega$				± 10	± 13		± 10	± 13		V
Output Short Circuit Current	$T_A = 25°C$	10	25	35		25			25		mA
	$T_{AMIN} \leq T_A \leq T_{AMAX}$	10		40							mA
Common-Mode Rejection Ratio	$T_{AMIN} \leq T_A \leq T_{AMAX}$										
	$R_S \leq 10\ k\Omega$, $V_{CM} = \pm 12V$				70	90		70	90		dB
	$R_S \leq 50\Omega$, $V_{CM} = \pm 12V$	80	95								dB
Supply Voltage Rejection Ratio	$T_{AMIN} \leq T_A \leq T_{AMAX}$, $V_S = \pm 20V$ to $V_S = \pm 5V$										
	$R_S \leq 50\Omega$	86	96								dB
	$R_S \leq 10\ k\Omega$				77	96		77	96		dB
Transient Response	$T_A = 25°C$, Unity Gain										
Rise Time			0.25	0.8		0.3			0.3		μs
Overshoot			6.0	20		5			5		%
Bandwidth (Note 4)	$T_A = 25°C$	0.437	1.5								MHz
Slew Rate	$T_A = 25°C$, Unity Gain	0.3	0.7			0.5			0.5		V/μs
Supply Current	$T_A = 25°C$					1.7	2.8		1.7	2.8	mA
Power Consumption	$T_A = 25°C$										
	$V_S = \pm 20V$		80	150							mW
	$V_S = \pm 15V$					50	85		50	85	mW
LM741A	$V_S = \pm 20V$										
	$T_A = T_{AMIN}$			165							mW
	$T_A = T_{AMAX}$			135							mW
LM741E	$V_S = \pm 20V$										
	$T_A = T_{AMIN}$			150							mW
	$T_A = T_{AMAX}$			150							mW
LM741	$V_S = \pm 15V$										
	$T_A = T_{AMIN}$					60	100				mW
	$T_A = T_{AMAX}$					45	75				mW

Note 1: For operation at elevated temperatures, these devices must be derated based on thermal resistance, and T_j max. (listed under "Absolute Maximum Ratings"). $T_j = T_A + (\theta_{jA} P_D)$.

Thermal Resistance	Cerdip (J)	DIP (N)	HO8 (H)	SO-8 (M)
θ_{jA} (Junction to Ambient)	100°C/W	100°C/W	170°C/W	195°C/W
θ_{jC} (Junction to Case)	N/A	N/A	25°C/W	N/A

Note 2: For supply voltages less than ± 15V, the absolute maximum input voltage is equal to the supply voltage.

Note 3: Unless otherwise specified, these specifications apply for $V_S = \pm 15V$, $-55°C \leq T_A \leq +125°C$ (LM741/LM741A). For the LM741C/LM741E, these specifications are limited to $0°C \leq T_A \leq +70°C$.

Note 4: Calculated value from: BW (MHz) = 0.35/Rise Time(μs).

Note 5: For military specifications see RETS741X for LM741 and RETS741AX for LM741A.

Note 6: Human body model, 1.5 kΩ in series with 100 pF.

8255A FUNCTIONAL DESCRIPTION

General

The 8255A is a programmable peripheral interface (PPI) device designed for use in Intel® microcomputer systems. Its function is that of a general purpose I/O component to interface peripheral equipment to the microcomputer system bus. The functional configuration of the 8255A is programmed by the system software so that normally no external logic is necessary to interface peripheral devices or structures.

Data Bus Buffer

This 3-state bidirectional 8-bit buffer is used to interface the 8255A to the system data bus. Data is transmitted or received by the buffer upon execution of input or output instructions by the CPU. Control words and status information are also transferred through the data bus buffer.

Read/Write and Control Logic

The function of this block is to manage all of the internal and external transfers of both Data and Control or Status words. It accepts inputs from the CPU Address and Control busses and in turn, issues commands to both of the Control Groups.

($\overline{CS}$)

Chip Select. A "low" on this input pin enables the communication between the 8255A and the CPU.

($\overline{RD}$)

Read. A "low" on this input pin enables the 8255A to send the data or status information to the CPU on the data bus. In essence, it allows the CPU to "read from" the 8255A.

($\overline{WR}$)

Write. A "low" on this input pin enables the CPU to write data or control words into the 8255A.

(A_0 and A_1)

Port Select 0 and Port Select 1. These input signals, in conjunction with the RD and WR inputs, control the selection of one of the three ports or the control word registers. They are normally connected to the least significant bits of the address bus (A_0 and A_1).

8255A BASIC OPERATION

A_1	A_0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	INPUT OPERATION (READ)
0	0	0	1	0	PORT A – DATA BUS
0	1	0	1	0	PORT B – DATA BUS
1	0	0	1	0	PORT C – DATA BUS
					OUTPUT OPERATION (WRITE)
0	0	1	0	0	DATA BUS – PORT A
0	1	1	0	0	DATA BUS – PORT B
1	0	1	0	0	DATA BUS – PORT C
1	1	1	0	0	DATA BUS – CONTROL
					DISABLE FUNCTION
X	X	X	X	1	DATA BUS – 3-STATE
1	1	0	1	0	ILLEGAL CONDITION
X	X	1	1	0	DATA BUS – 3-STATE

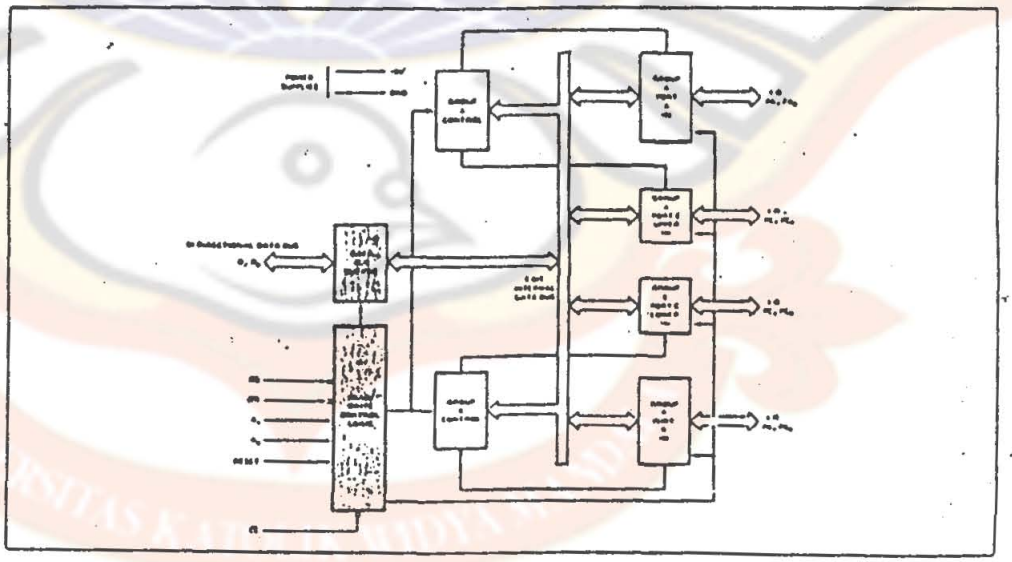
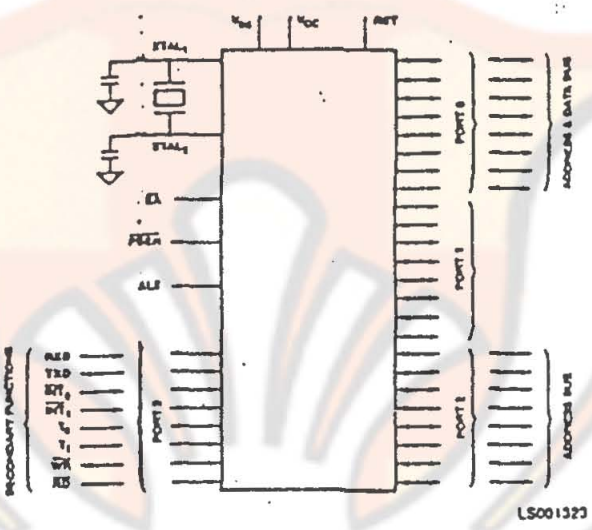


Figure 3. 8255A Block Diagram Showing Data Bus Buffer and Read/Write Control Logic Functions

LOGIC SYMBOL



Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

(Note 5)

	LM741A	LM741E	LM741	LM741C
Supply Voltage	±22V	±22V	±22V	±18V
Power Dissipation (Note 1)	500 mW	500 mW	500 mW	500 mW
Differential Input Voltage	±30V	±30V	±30V	±30V
Input Voltage (Note 2)	±15V	±15V	±15V	±15V
Output Short Circuit Duration	Continuous	Continuous	Continuous	Continuous
Operating Temperature Range	−55°C to +125°C	0°C to +70°C	−55°C to +125°C	0°C to +70°C
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C
Junction Temperature	150°C	100°C	150°C	100°C
Soldering Information				
N-Package (10 seconds)	260°C	260°C	260°C	260°C
J- or H-Package (10 seconds)	300°C	300°C	300°C	300°C
M-Package				
Vapor Phase (60 seconds)	215°C	215°C	215°C	215°C
Infrared (15 seconds)	215°C	215°C	215°C	215°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

ESD Tolerance (Note 6)	400V	400V	400V	400V

Electrical Characteristics (Note 3)

Parameter	Conditions	LM741A/LM741E			LM741			LM741C		
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
Input Offset Voltage	$T_A = 25°C$ $R_S \le 10\ k\Omega$ $R_S \le 50\Omega$		0.8	3.0		1.0	5.0		2.0	6.0
	$T_{AMIN} \le T_A \le T_{AMAX}$ $R_S \le 50\Omega$ $R_S \le 10\ k\Omega$			4.0			6.0			7.5
Average Input Offset Voltage Drift				15						
Input Offset Voltage Adjustment Range	$T_A = 25°C, V_S = \pm 20V$	±10				±15			±15	
Input Offset Current	$T_A = 25°C$		3.0	30		20	200		20	200
	$T_{AMIN} \le T_A \le T_{AMAX}$			70		85	500			300
Average Input Offset Current Drift				0.5						
Input Bias Current	$T_A = 25°C$		30	80		80	500		80	500
	$T_{AMIN} \le T_A \le T_{AMAX}$			0.210			1.5			0.8
Input Resistance	$T_A = 25°C, V_S = \pm 20V$	1.0	6.0		0.3	2.0		0.3	2.0	
	$T_{AMIN} \le T_A \le T_{AMAX}$, $V_S = \pm 20V$	0.5								
Input Voltage Range	$T_A = 25°C$							±12	±13	
	$T_{AMIN} \le T_A \le T_{AMAX}$				±12	±13				
Large Signal Voltage Gain	$T_A = 25°C, R_L \ge 2\ k\Omega$ $V_S = \pm 20V, V_O = \pm 15V$ $V_S = \pm 15V, V_O = \pm 10V$	50			50	200		20	200	
	$T_{AMIN} \le T_A \le T_{AMAX}$, $R_L \ge 2\ k\Omega$, $V_S = \pm 20V, V_O = \pm 15V$ $V_S = \pm 15V, V_O = \pm 10V$ $V_S = \pm 5V, V_O = \pm 2V$	32 10			 25			 15		

8255A/8255A-5
PROGRAMMABLE PERIPHERAL INTERFACE

- MCS-85™ Compatible 8255A-5
- 24 Programmable I/O Pins
- Completely TTL Compatible
- Fully Compatible with Intel® Microprocessor Families
- Improved Timing Characteristics
- Direct Bit Set/Reset Capability Easing Control Application Interface
- 40-Pin Dual In-Line Package
- Reduces System Package Count
- Improved DC Driving Capability

The Intel® 8255A is a general purpose programmable I/O device designed for use with Intel® microprocessors. It has 24 I/O pins which may be individually programmed in 2 groups of 12 and used in 3 major modes of operation. In the first mode (MODE 0), each group of 12 I/O pins may be programmed in sets of 4 to be input or output. In MODE 1, the second mode, each group may be programmed to have 8 lines of input or output. Of the remaining 4 pins, 3 are used for handshaking and interrupt control signals. The third mode of operation (MODE 2) is a bidirectional bus mode which uses 8 lines for a bidirectional bus, and 5 lines, borrowing one from the other group, for handshaking.

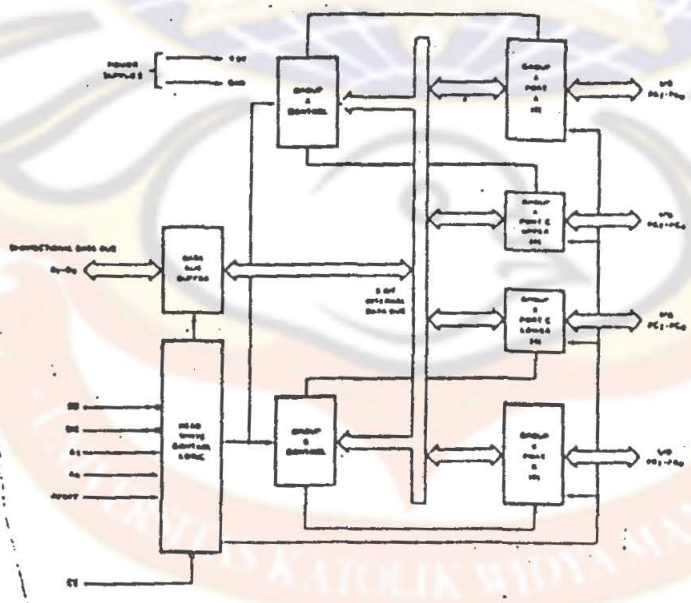


Figure 1. 8255A Block Diagram

Figure 2. Pin Configuration

(RESET)

Reset. A "high on this input clears the control register and all ports (A, C, C) are set to the input mode.

Group A and Group B Controls

The functional configuration of each port is programmed by the systems software. In essence, the CPU "outputs" a control word to the 8255A. The control word contains information such as "mode", "bit set", "bit reset", etc., that initializes the functional configuration of the 8255A.

Each of the Control blocks (Group A and Group B) accepts "commands" from the Read/Write Control Logic, receives "control words" from the internal data bus and issues the proper commands to its associated ports.

Control Group A – Port A and Port C upper (C7-C4)
Control Group B – Port B and Port C lower (C3-C0)

The Control Word Register can Only be written into. No Read operation of the Control Word Register is allowed.

Ports A, B, and C

The 8255A contains three 8-bit ports (A, B, and C). All can be configured in a wide variety of functional characteristics by the system software but each has its own special features or "personality" to further enhance the power and flexibility of the 8255A.

Port A. One 8-bit data output latch/buffer and one 8-bit data input latch.

Port B. One 8-bit data input/output latch/buffer and one 8-bit data input buffer.

Port C. One 8-bit data output latch/buffer and one 8-bit data input buffer (no latch for input). This port can be divided into two 4-bit ports under the mode control. Each 4-bit port contains a 4-bit latch and it can be used for the control signal outputs and status signal inputs in conjunction with ports A and B.

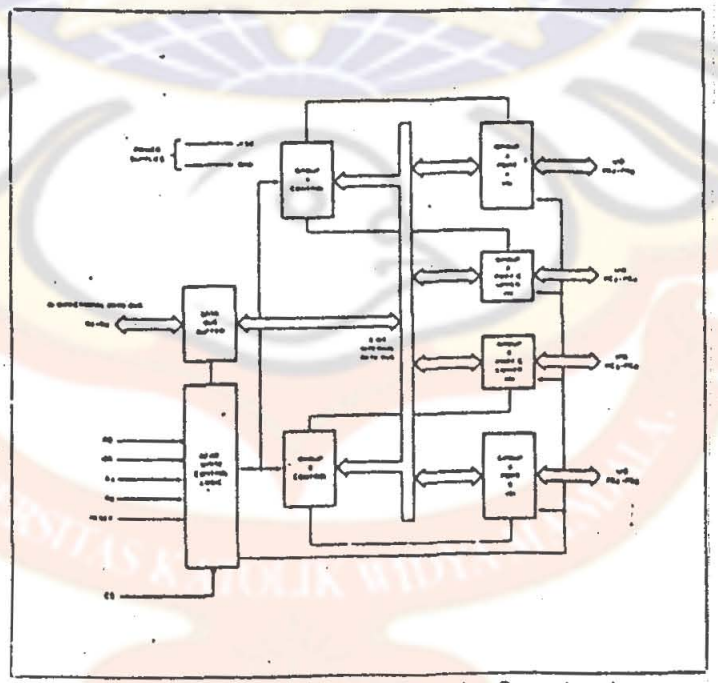


Figure 4. 8225A Block Diagram Showing Group A and Group B Control Functions

PIN CONFIGURATION

PIN NAMES

D_0-D_7	DATA BUS (BI-DIRECTIONAL)
RESET	RESET INPUT
$\overline{CS}$	CHIP SELECT
$\overline{RD}$	READ INPUT
$\overline{WR}$	WRITE INPUT
A0, A1	PORT ADDRESS
PA7-PA0	PORT A (BIT)
PB7-PB0	PORT B (BIT)
PC7-PC0	PORT C (BIT)
V_{CC}	+5 VOLTS
GND	0 VOLTS