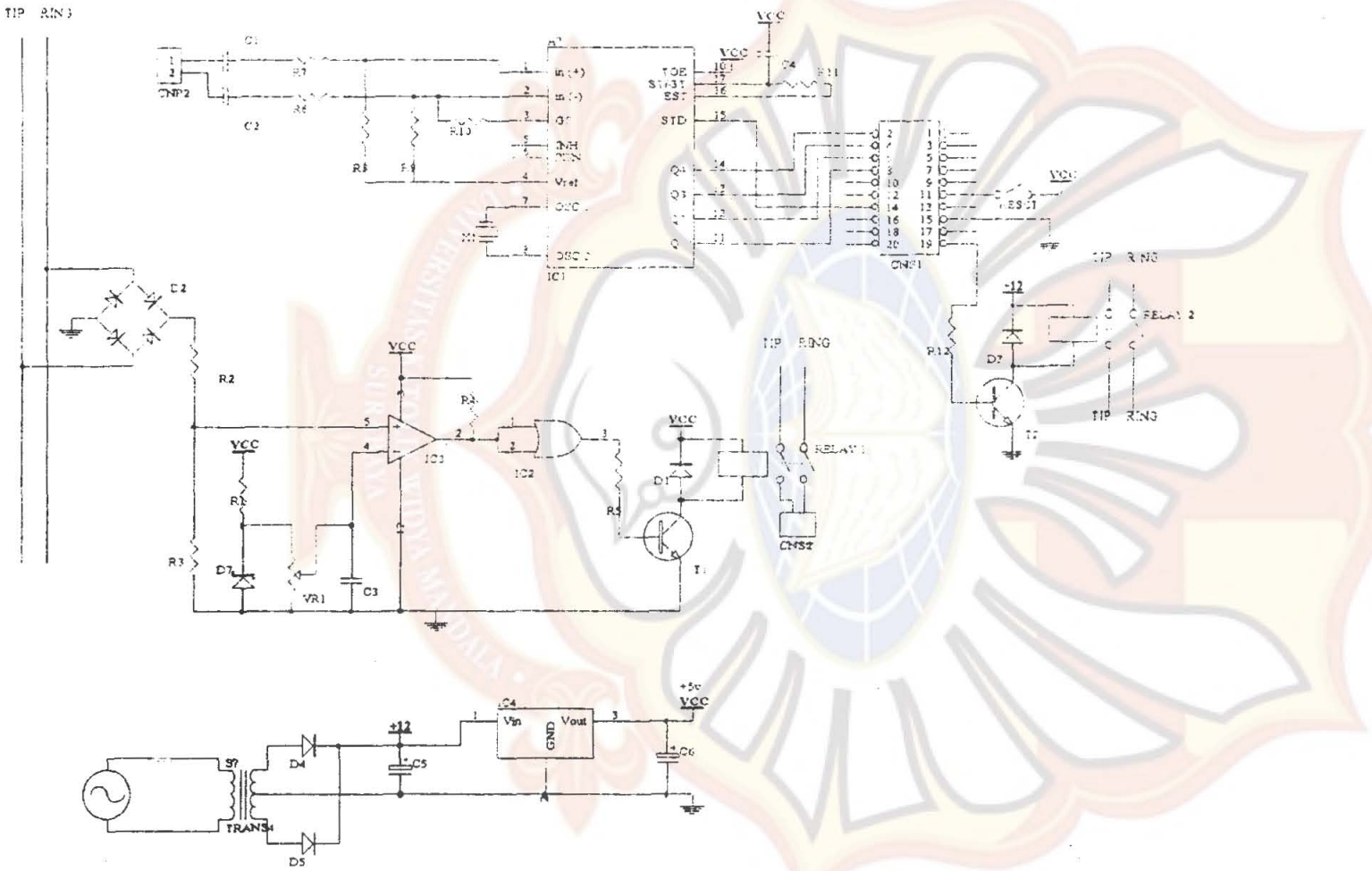
LAMPIRAN

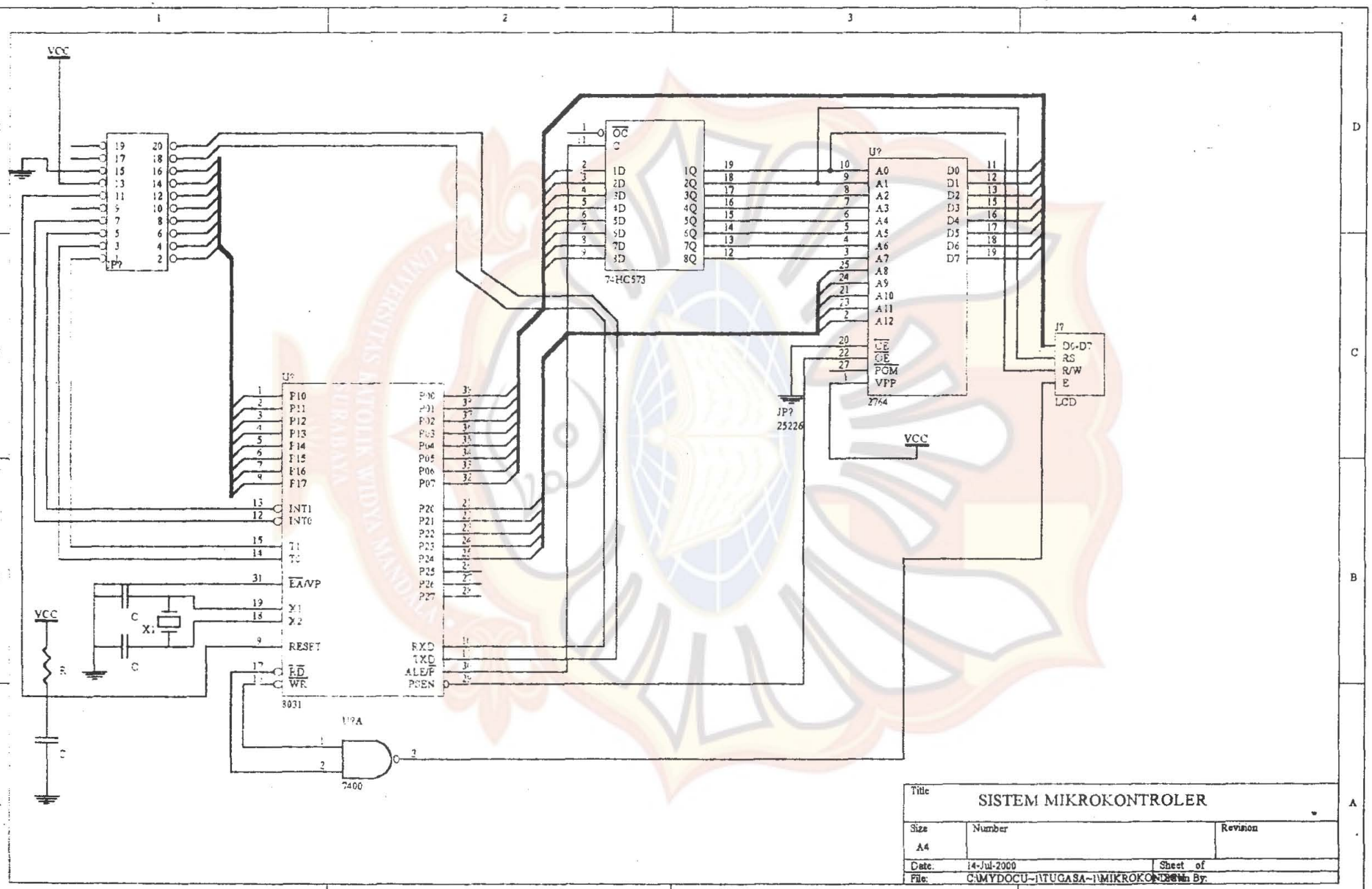


Komponen

Resistor	
R1,R5,R12	1K
R2	47K
R3	4,7K
R4	3,9K
R6,R7,R10	100K
R9	39K
VR1	10K
Capasitor	
C1,C2,C3	10n
C4	4,7n
C5,C6	2200u
Semikonduktor	
D1,D3,D4,D5	1n4002
D2,	4x1n4002
zener	3v
IC1	8870
IC2	7432
IC3	LM339
IC4	7805
T1,T2	BD139

Switch
1xSPST switch
2xRelay 2spdt

CN31


VCC
JP?
74HC573
OC
C
1D
2D
3D
4D
5D
6D
7D
8D
1Q
2Q
3Q
4Q
5Q
6Q
7Q
8Q
U?
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
D0
D1
D2
D3
D4
D5
D6
D7
CE
OE
PGM
VPP
2764
JP?
25226
J?
D0-D7
RS
R/W
E
LCD
U?
P10
P11
P12
P13
P14
P15
P16
P17
P00
P01
P02
P03
P04
P05
P06
P07
P20
P21
P22
P23
P24
P25
P26
P27
INT1
INT0
T1
T0
EA/VP
X1
X2
RESET
RXD
TXD
RD
WR
ALE/P
PSEN
8031
U?A
7400
C
X1
R
Title
SISTEM MIKROKONTROLER
Size
A4
Number
Revision
Date:
14-Jul-2000
Sheet of
File:
C:\MYDOCU~1\TUGASA~1\MIKROKON.DSN
Drawn By:

```
WR_CTRL_REG       EQU 2000H
WR_DATA_REG       EQU 2001H
RD_CTRL_REG       EQU 2002H
RD_DATA_REG       EQU 2003H
COUNTER           EQU 39H


                  ORG 0000H
                  AJMP MAIN

                  ORG 100H

MAIN:             MOV SP,#70H

                  ACALL INIT_LCD

LOGO:             ACALL PRT_TITLE1
                  ACALL PRT_TITLE2

                  JB P1.7,ZERO_DIAL          ;OFF HOOK?
                  SJMP LOGO

ZERO_DIAL:        ACALL PRT_MESSAGE2         ;ENTER YOUR NUMBER
WAIT:             JB P1.6,NEXT
                  SJMP WAIT

NEXT:             ACALL ZERO_TEST
                  JNB P15,STOP               ;P15 =0= PROTECTED
                  JBC P14,LOGO

PROCESS:          JB P1.6,DATA_READ          ;DIAL DITEKAN?
                  JNB P1.7,LOGO              ;OFF HOOK?
                  SJMP PROCESS

STOP:             SETB P3.0       ;relay on
                  ACALL PRT_FAIL
                  SJMP STOP
;-------------------------------------------------------------
ZERO_TEST:        PUSH DPH
                  PUSH DPL
                  PUSH PSW

                  ACALL READ_DATA
                  ACALL DATA_OUT
```

```
                CJNE A,#0,ASSIGN2
                AJMP SLJJ
ASSIGN2:        CJNE A,#1,ASSIGNX
                SJMP READ33
ASSIGNX:        AJMP ASSIGN
READ33:         JB P1.6,SECOND          ;DIAL DITEKAN?
                SJMP READ33

SECOND:         ACALL READ_DATA
                MOV A,BUFFER
                ACALL DATA_OUT

                CJNE A,#0,ASSIGN

READ333:        JB P1.6,THIRD           ;DIAL DITEKAN?
                SJMP READ333


THIRD:          MOV R7,#6               ;READ 3Th NUMBER
                ACALL READ_DATA
                ACALL DATA_OUT

                CJNE A,#1,ASSIGN

SLJJ:           ACALL PRT_MESSAGE1      ;SLJJ
                ACALL PASSWORD_READ
                ACALL COMPARE

                JNB EOS,UNPROTECT

                ACALL PRT_MESSAGE4      ;ILEGAL CONTACT
                SJMP CONTINUED

UNPROTECT:      ACALL PRT_MESSAGE3      ;LEGAL CONTACT

                SETB P3.0               ;INIT CONTACT
                CLR P3.0

                ACALL PRT_MESSAGE2

PROCESS2:       JB P1.6,DATA_READ2      ;DIAL DITEKAN?
                JNB P1.7,LOGO3
                SJMP PROCESS2

LOGO3:          AJMP LOGO
```

```
DATA_READ2:     ACALL READ_DATA

NORMAL2:        ACALL DATA_OUT
                MOV COUNTER,#1
                SJMP PROCESS2

CONTINUED:      POP PSW
                POP DPL
                POP DPH
                RET
;-------------------------------------------------------------------
PASSWORD_READ:  PUSH DPH
                PUSH DPL
                PUSH PSW


READ:           JB P1.6,PASSWORD_RD     ;DIAL DITEKAN?
                SJMP READ

PASSWORD_RD:    ACALL READ_DATA
                ACALL DATA_OUT

                POP PSW
                POP DPL
                POP DPH

                RET
;-------------------------------------------------------------------
COMPARE:        PUSH DPH
                PUSH DPL
                PUSH PSW


UNFAIL2:        MOV A,DIGIT2
                CJNE A,#5,FAIL
                CLR EOS         ;EOT =1 IF MATCH


UNFAIL3:        MOV A,DIGIT3
                CJNE A,#1,FAIL
                CLR EOS         ;EOT =1 IF MATCH

UNFAIL4:        MOV A,DIGIT4
                CJNE A,#9,FAIL
```

```
                CLR EOS             ;EOT =1 IF MATCH

UNFAIL5:        MOV A,DIGIT5
                CJNE A,#4,FAIL
                CLR EOS             ;EOT =1 IF MATCH

UNFAIL6:        MOV A,DIGIT6
                CJNE A,#5,FAIL
                CLR EOS             ;EOT =1 IF MATCH
                SJMP EXIT

FAIL:           SETB EOS


EXIT:           POP PSW
                POP DPL
                POP DPH
                RET
;-------------------------------------------------------------------------
PRT_TITLE1:     PUSH DPH
                PUSH DPL
                MOV DPTR,#HEADER1
                ACALL OUT_CHAR
                ACALL LOCATE2
                MOV DPTR,#HEADER2
                ACALL OUT_CHAR

                MOV DPTR,#HEADER3
                ACALL OUT_CHAR
                MOV DPTR,#HEADER4
                ACALL OUT_CHAR


                POP DPL
                POP DPH
                RET

;-------------------------------------------------------------------------
PRT_TITLE2:     PUSH DPH
                PUSH DPL

                MOV DPTR,#HEADER5
                ACALL OUT_CHAR
                MOV DPTR,#HEADER6
                ACALL OUT_CHAR
```

```
                MOV DPTR,#HEADER7
                ACALL OUT_CHAR
                MOV DPTR,#HEADER8
                ACALL OUT_CHAR

                POP DPL
                POP DPH
                RET

;-----------------------------------------------------------------
PRT_MESSAGE1:   PUSH DPH
                PUSH DPL
                MOV DPTR,#HEADER9
                ACALL OUT_CHAR
                MOV DPTR,#HEADER10
                ACALL OUT_CHAR

                POP DPL
                POP DPH
                RET
;-----------------------------------------------------------------
PRT_MESSAGE2:   PUSH DPH
                PUSH DPL
                MOV DPTR,#HEADER11
                ACALL OUT_CHAR
                MOV DPTR,#HEADER12
                ACALL OUT_CHAR
                POP DPL
                POP DPH
                RET
;-----------------------------------------------------------------
PRT_MESSAGE3:   PUSH DPH
                PUSH DPL
                MOV DPTR,#HEADER13
                ACALL OUT_CHAR
                MOV DPTR,#HEADER14
                ACALL OUT_CHAR
                POP DPL
                POP DPH
                RET
;-----------------------------------------------------------------
PRT_MESSAGE4:   PUSH DPH
                PUSH DPL
                MOV DPTR,#HEADER15
```

```
                ACALL OUT_CHAR
                MOV DPTR,#HEADER16
                ACALL OUT_CHAR
                POP DPL
                POP DPH
                RET
;-------------------------------------------------------------------
INIT_LCD:       PUSH DPH
                PUSH DPL
                PUSH PSW
                PUSH ACC
                MOV R0,#0FFH
                ACALL DELAY_LOOP
                MOV R0,#0FFH
                ACALL DELAY_LOOP
                MOV R0,#0FFH
                ACALL DELAY_LOOP
                MOV R0,#0FFH
                ACALL DELAY_LOOP
                MOV A,#00111000B
                ACALL CTRL_OUT
                MOV R0,#0FFH
                ACALL DELAY_LOOP
                MOV A,#00111000B
                ACALL CTRL_OUT
                MOV R0,#0FFH
                ACALL DELAY_LOOP
                MOV R0,#0FFH
                ACALL DELAY_LOOP
                MOV R0,#0FFH
                ACALL DELAY_LOOP
                MOV A,#00111000B
                ACALL CTRL_OUT
                MOV R0,#0FFH
                ACALL DELAY_LOOP
                MOV A,#00111000B
                ACALL CTRL_OUT
                MOV R0,#0FFH
                ACALL DELAY_LOOP
                MOV A,#00001000B
                ACALL CTRL_OUT
                MOV R0,#0FFH
                ACALL DELAY_LOOP
                MOV A,#00000001B
                ACALL CTRL_OUT
```

```
                MOV R0,#0FFH
                ACALL DELAY_LOOP
                MOV A,#00000110B
                ACALL CTRL_OUT
                POP ACC
                POP PSW
                POP DPL
                POP DPH
                RET
;-------------------------------------------------------------------
CLEAR_DISPLAY:      PUSH DPH
                PUSH DPL
                MOV A,#00000001B
                ACALL CTRL_OUT
                MOV R0,#0FFH
                ACALL DELAY_LOOP
                POP DPL
                POP DPH
                RET

;-------------------------------------------------------------------
DELAY_5S:           PUSH DPH
                PUSH DPL
DEL3:               MOV R5,#8H
                DJNZ R5,DEL3
                POP DPL
                POP DPH
                RET
;-------------------------------------------------------------------
PRT_FAIL:           PUSH DPH
                PUSH DPL
                MOV DPTR,#FAIL1
                ACALL OUT_CHAR
                MOV DPTR,#FAIL2
                ACALL OUT_CHAR
                POP DPL
                POP DPH
                RET
;-------------------------------------------------------------------
HEADER1         DB ' MICROCONTROLLER'
HEADER2         DB '    DRIVEN    '
HEADER3         DB '  TELEPHONE   '
HEADER4         DB '  PROTECTOR   '
HEADER5         DB ' DESIGNED BY: '
HEADER6         DB 'HIDAYAT SETIAWAN'
```

```
HEADER7         DB ' FTE UNIKA '
HEADER8         DB ' WIDYA MANDALA '
HEADER9         DB ' ENTER YOUR '
HEADER10        DB 'PASSWORD NUMBER'
HEADER11        DB ' ENTER YOUR '
HEADER12        DB 'TELEPHONE NUMBER'
HEADER13        DB ' LEGAL CONTACT '
HEADER14        DB 'PLEASE CONTINUE'
HEADER15        DB 'ILEGAL CONTACT '
HEADER16        DB 'SYSTEM DISABLE '
FAIL1         DB '   FAIL   '
FAIL2         DB '  CONTACT   '

              END
```

Absolute Maximum Ratings[1]

	Parameter	Symbol	Min	Max	Units
1	Power supply voltage V_{DD}-V_{SS}			6	V
2	Voltage on any pin		V_{SS} - 0.3	V_{DD} + 0.3	V
3	Current at any pin (other than supply)			10	mA
4	Operating temperature	T_A	- 40	+ 85	°C
5	Storage temperature		- 65	+ 150	°C
6	Package power dissipation			1000	mW

[1] Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.
Derate above 75 °C at 16 mW/°C. All leads soldered to board.

Recommended Operating Conditions - Voltages are with respect to ground (V_{SS}) unless otherwise stated

		Characteristics	Sym	Min	Typ[1]	Max	Units	Test Conditions
1		Positive Supply Voltages	V_{DD}		5		V	V_{SS} = 0V
2		Oscillator Clock Frequency	fc		3.579545		MHz	
3		Oscillator Frequency Tolerance	Δfc		± 0.1		%	

[1] Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics - V_{DD} = 5.0V ± 5%, V_{SS} = 0V. Voltages are with respect to ground (V_{SS}) unless otherwise stated

		Characteristics	Sym	Min	Typ[1]	Max	Units	Test Conditions
1	SUPPLY	Operating supply voltage	V_{DD}	4.75	5.0	5.25	V	
2		Operating supply current	I_{DD}		3.0	9.0	mA	
3		Power consumption	P_D		15	45	mW	f = 3.58 MHz, V_{DD} = 5V
4	INPUTS	High level input	V_{IH}	3.5			V	
5		Low level input voltage	V_{IL}			1.5	V	
6		Input leakage current	I_{IH}/I_{IL}		0.1		μA	V_{IN} = V_{SS} or V_{DD}
7		Pull-up (source) current	I_{PU}		7.5	15	μA	TOE (pin 10) = 0V
8		Input impedance (IN+, IN-)	R_{IN}		10		MΩ	@ 1 kHz
9		Steering threshold voltage	V_{TSt}	2.2		2.5	V	
10	OUTPUTS	Low level output voltage	V_{OL}			V_{SS} + 0.03	V	No load
11		High level output voltage	V_{OH}	V_{DD}-0.03			V	No load
12		Output low (sink) current	I_{OL}	1	2.5		mA	V_{OUT} = 0.4 V
13		Output high (source) current	I_{OH}	0.4	0.8		mA	V_{OUT} = 4.6 V
14		V_{Ref} output voltage	V_{Ref}	2.4		2.7	V	No load
15		V_{Ref} output resistance	R_{OR}		10		kΩ	

[1] Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

ISO²-CMOS MT8870B/MT8870B-1
Integrated DTMF Receiver

9161-002-051-NA ISSUE 2 December 1987

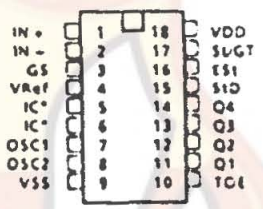
Features

- Complete DTMF Receiver
- Low Power Consumption
- Internal Gain Setting Amplifier
- Adjustable Guard Time
- Central Office Quality

Applications

- Receiver System for British Telecom (BT) or CEPT Spec (MT8870B-1)
- Paging Systems
- Repeater Systems/Mobile Radio
- Credit Card Systems
- Remote Control
- Personal Computers

Pin Connections



* Connected to VSS

Ordering Information

MT8870BE/MT8870BE-1 Plastic DIP
MT8870BC/MT8870BC-1 Ceramic DIP
-40°C to +85°C

Description

The MT8870B/MT8870B-1 is a complete DTMF receiver integrating both the bandsplit filter and digital decoder functions, fabricated in Mitel's double poly ISO²-CMOS technology. The filter section uses switched capacitor techniques for high and low group filters; the decoder uses digital counting techniques to detect and decode all 16 DTMF tone pairs into a 4-bit code. External component count is minimized by on chip provision of a differential input amplifier, clock oscillator and latched three-state bus interface.

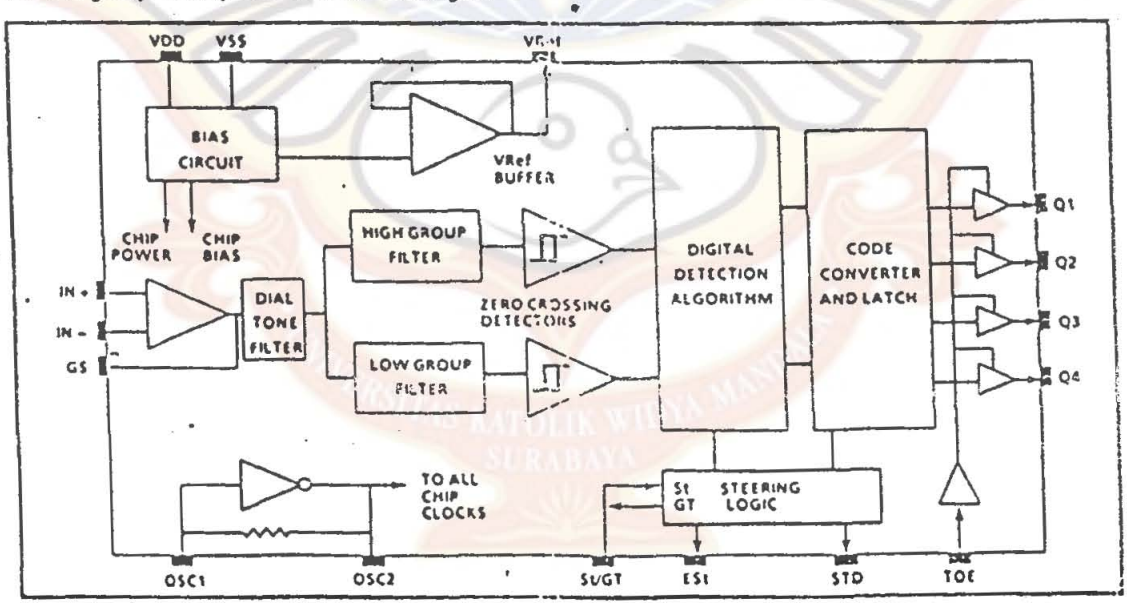


Figure 1 - Functional Block Diagram

Operating Characteristics[1] - Voltages are with respect to ground (V_{SS}) unless otherwise stated

Gain Setting Amplifier

	Characteristics	Sym	Min	Typ[2]	Max	Units	Test Conditions
1	Input leakage current	I_{IN}		100		nA	$V_{SS} \le V_{IN} \le V_{DD}$
2	Input resistance	R_{IN}		10		MΩ	
3	Input offset voltage	V_{OS}		25		mV	
4	Power supply rejection	PSRR		60		dB	1 KHz
5	Common mode rejection	CMRR		60		dB	$-3.0V \le V_{IN} \le 3.0V$
6	DC open loop voltage gain	A_{VOL}		65		dB	
7	Open loop unity gain bandwidth	f_C		1.5		MHz	
8	Output voltage swing	V_O		4.5		V_{pp}	$R_L \ge 100K\Omega$ to V_{SS}
9	Maximum capacitive load (GS)	C_L		100		pF	
10	Maximum resistive load (GS)	R_L		50		KΩ	
11	Common mode range	V_{CM}		3.0		V_{pp}	No Load

[1] $V_{DD} = 5\ V, V_{SS} = 0\ V, T_A = 25°C$

[2] Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

MT8870B AC Electrical Characteristics[1] - Voltages are with respect to ground (V_{SS}) unless otherwise stated

		Characteristics	Sym	Min	Typ	Max	Units	Notes
1	SIGNAL CONDITIONS	Valid input signal levels (each tone of composite signal)		-29			dBm	1,2,3,5,6,9
				27.5			mV_{RMS}	1,2,3,5,6,9
						+1	dBm	1,2,3,5,6,9
						869	mV_{RMS}	1,2,3,5,6,9
2		Positive twist accept			10		dB	2,3,6,9
3		Negative twist accept			10		dB	2,3,6,9
4		Freq. deviation accept		± 1.5% ± 2Hz			Nom.	2,3,5,9
5		Freq. deviation reject		± 3.5%			Nom.	2,3,5,9
6		Third tone tolerance			-16		dB	2,3,4,5,9
7		Noise tolerance			-12		dB	2,3,4,5,7,9,10
8		Dial tone tolerance			+22		dB	2,3,4,5,8,9,11

[1] $V_{DD} = 5\ V, V_{SS} = 0, T_A = 25°C$ and $f_C = 3.579545$ MHz using test circuit shown in Figure 2

NOTES

1. dBm = decibels above or below a reference power of 1 mW into a 600 ohm load.
2. Digit sequence consists of all DTMF tones
3. Tone duration = 40 ms, tone pause = 40 ms
4. Signal condition consists of nominal DTMF frequencies
5. Both tones in composite signal have an equal amplitude
6. Tone pair is deviated by ± 1.5% ± 2 Hz.
7. Bandwidth limited (3 kHz) Gaussian noise.
8. The precise dial tone frequencies are (350 Hz and 440 Hz) ± 2 %
9. For an error rate of better than 1 in 10,000.
10. Referenced to lowest level frequency component in DTMF signal
11. Referenced to the minimum valid accept level.

MT8870B-1 AC Electrical Characteristics[1] - Voltages are with respect to ground (V_{SS}) unless otherwise stated

		Characteristics	Sym	Min	Typ	Max	Units	Notes
1	SIGNAL CONDITIONS	Valid input signal levels (each tone of composite signal)		-31			dBm	1,2,3,5,6,9
				21.8			mV_{RMS}	1,2,3,5,6,9
						+1	dBm	1,2,3,5,6,9
						869	mV_{RMS}	1,2,3,5,6,9
2		Input Signal Level Reject		-37			dBm	1,2,3,5,6,9
				10.9			mV_{RMS}	1,2,3,5,6,9
3		Positive twist accept				6	dB	2,3,6,9
4		Negative twist accept				6	dB	2,3,6,9
5		Freq. deviation accept		± 1.5% ± 2Hz				2,3,5,9
6		Freq. deviation reject		± 3.5%				2,3,5,9
7		Third tone tolerance		-18.5			dB	2,3,4,5,9,12
8		Noise tolerance			-12		dB	2,3,4,5,7,9,10
9		Dial tone tolerance			+22		dB	2,3,4,5,8,9,11

[1] V_{DD} = 5 V, V_{SS} = 0, T_A = 25°C and f_C = 3.579545 MHz using test circuit shown in Figure 2.

NOTES

1. dBm = decibels above or below a reference power of 1 mW into a 600 ohm load.
2. Digit sequence consists of all DTMF tones
3. Tone duration = 40 ms, tone pause = 40 ms.
4. Signal condition consists of nominal DTMF frequencies
5. Both tones in composite signal have an equal amplitude.
6. Tone pair is deviated by ± 1.5% ± 2 Hz.
7. Bandwidth limited (3 kHz) Gaussian noise.
8. The precise dial tone frequencies are (350 Hz and 440 Hz) ± 2 %.
9. For an error rate of better than 1 in 10,000.
10. Referenced to lowest level frequency component in DTMF signal.
11. Referenced to the minimum valid accept level.
12. Referenced to Fig. 10 Input DTMF Tone Level at -25 dBm (-28 dBm at GS Pin) Interference Frequency Range between 480-3400 Hz

AC Electrical Characteristics -- Voltages are with respect to ground (V_{SS}) unless otherwise stated

		Characteristics	Sym	Min	Typ[2]	Max	Units	Test Conditions
1	TIMING	Tone present detect time	t_{DP}	5	11	14	ms	see Figure 3
2		Tone absent detect time	t_{DA}	0.5	4	8.5	ms	see Figure 3
3		Tone duration accept	t_{REC}			40	ms	User adjustable
4		Tone duration reject	$t_{\overline{REC}}$	20			ms	User adjustable
5		Interdigit pause accept	t_{ID}			40	ms	User adjustable
6		Interdigit pause reject	$t_{\overline{ID}}$	20			ms	User adjustable
7	OUTPUTS	Propagation delay (St to Q)	t_{PQ}		8	11	µs	TOE = V_{DD}
8		Propagation delay (St to StD)	t_{PStD}		12		µs	TOE = V_{DD}
9		Output data set up (Q to StD)	t_{QStD}		3.4		µs	TOE = V_{DD}
10		Propagation delay (TOE to Q ENABLE)	t_{PTE}		50		ns	RL = 10KΩ CL = 50 pF
11		Propagation delay (TOE to Q DISABLE)	t_{PTD}		300		ns	RL = 10KΩ CL = 50 pF
12	CLOCK	Crystal /clock frequency	f_C	3.5759	3.5795	3.5831	MHz	
13		Clock input rise time	t_{LHCL}			110	ns	Ext. clock
14		Clock input fall time	t_{HLCL}			110	ns	Ext. clock
15		Clock input duty cycle	DC_{CL}	40	50	60	%	Ext. clock
16		Capacitive load (OSC2)	C_{LO}			30	pF	

[1] V_{DD} = 5.0V, V_{SS} = 0V, T_A = 25°C and f_C = 3.579545 MHz, using test circuit shown in Figure 2

[2] Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing

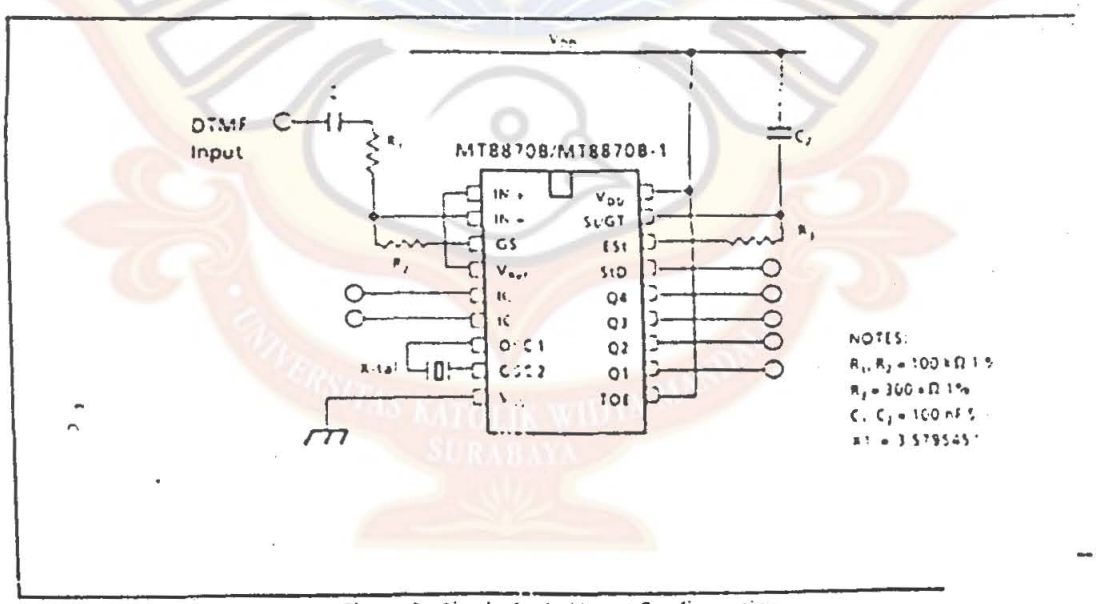


Figure 2 - Single-Ended Input Configuration

Pin Description

Pin #	Name	Description
1	IN +	Non-Inverting Op-Amp (Input).
2	IN –	Inverting Op-Amp (Input).
3	GS	Gain Select. Gives access to output of front end differential amplifier for connection of feedback resistor.
4	V_{Ref}	Reference Voltage (Output). Nominally $V_{DD}/2$ is used to bias inputs at mid-rail (see Fig.2).
5	IC	Internal Connection. Must be tied to V_{SS}.
6	IC	Internal Connection. Must be tied to V_{SS}.
7	OSC1	Clock (Input)
8	OSC2	Clock (Output). A 3.579545 MHz crystal connected between pins OSC1 and OSC2 completes the internal oscillator circuit.
9	V_{SS}	Negative Power Supply (Input).
10	TOE	Three State Output Enable (Input). Logic high enables the outputs Q1-Q4. This pin is pulled up internally.
11-14	Q1-Q4	Three State Data (Output). When enabled by TOE, provide the code corresponding to the last valid tone-pair received (see Table 1). When TOE is logic low, the data outputs are high impedance.
15	StD	Delayed Steering (Output). Presents a logic high when a received tone-pair has been registered and the output latch updated; returns to logic low when the voltage on St/GT falls below V_{TSt}.
16	ESt	Early Steering (Output). Presents a logic high once the digital algorithm has detected a valid tone pair (signal condition). Any momentary loss of signal condition will cause ESt to return to a logic low.
17	St/GT	Steering Input/Guard time (Output) Bidirectional. A voltage greater than V_{TSt} detected at St causes the device to register the detected tone pair and update the output latch. A voltage less than V_{TSt} frees the device to accept a new tone pair. The GT output acts to reset the external steering time-constant; its state is a function of ESt and the voltage on St.
18	V_{DD}	Positive power supply (Input).

80C51BH/80C31BH

CHMOS SINGLE-CHIP 8-BIT MICROCOMPUTER

80C51BH—4 KBYTES OF FACTORY MASK-PROGRAMMABLE ROM
80C31BH—CPU WITH RAM AND I/O

80C51BH/80C31BH—3.5 to 12 MHz, V_{CC} = 5V ±20%
80C51BH-1/80C31BH-1—3.5 to 16 MHz, V_{CC} = 5V ±20%
80C51BH-2/80C31BH-2—0.5 to 12 MHz, V_{CC} = 5V ±20%

- Power Control Modes
- 128 x 8-Bit RAM
- 32 Programmable I/O Lines
- Two 16-Bit Timer/Counters
- 64K Program Memory Space
- High Performance CHMOS Process
- Boolean Processor
- 5 Interrupt Sources
- Programmable Serial Port
- 64K Data Memory Space
- ONCE™ (On-Circuit Emulation) Mode

The MCS®-51 CHMOS products are fabricated on Intel's CHMOS III process and are functionally compatible with the standard MCS-51 HMOS and EPROM products. CHMOS III is a technology which combines the high speed and density characteristics of HMOS with the low power attributes of CHMOS. This combination expands the effectiveness of the powerful MCS-51 architecture and instruction set.

Like the MCS-51 HMOS versions, the MCS-51 CHMOS products have the following features: 4 Kbyte of ROM (80C51BH/80C51BH-1/80C51BH-2 only); 128 bytes of RAM; 32 I/O lines; two 16-bit timer/counters; a five-source two-level interrupt structure; a full duplex serial port; and on-chip oscillator and clock circuitry. In addition, the MCS-51 CHMOS products have two software selectable modes of reduced activity for further power reduction—Idle and Power Down.

The Idle mode freezes the CPU while allowing the RAM, timer/counters serial port and interrupt system to continue functioning. The Power Down mode saves the RAM contents but freezes the oscillator, causing all other chip functions to be inoperative.

October 1990
Order Number: 270064-006

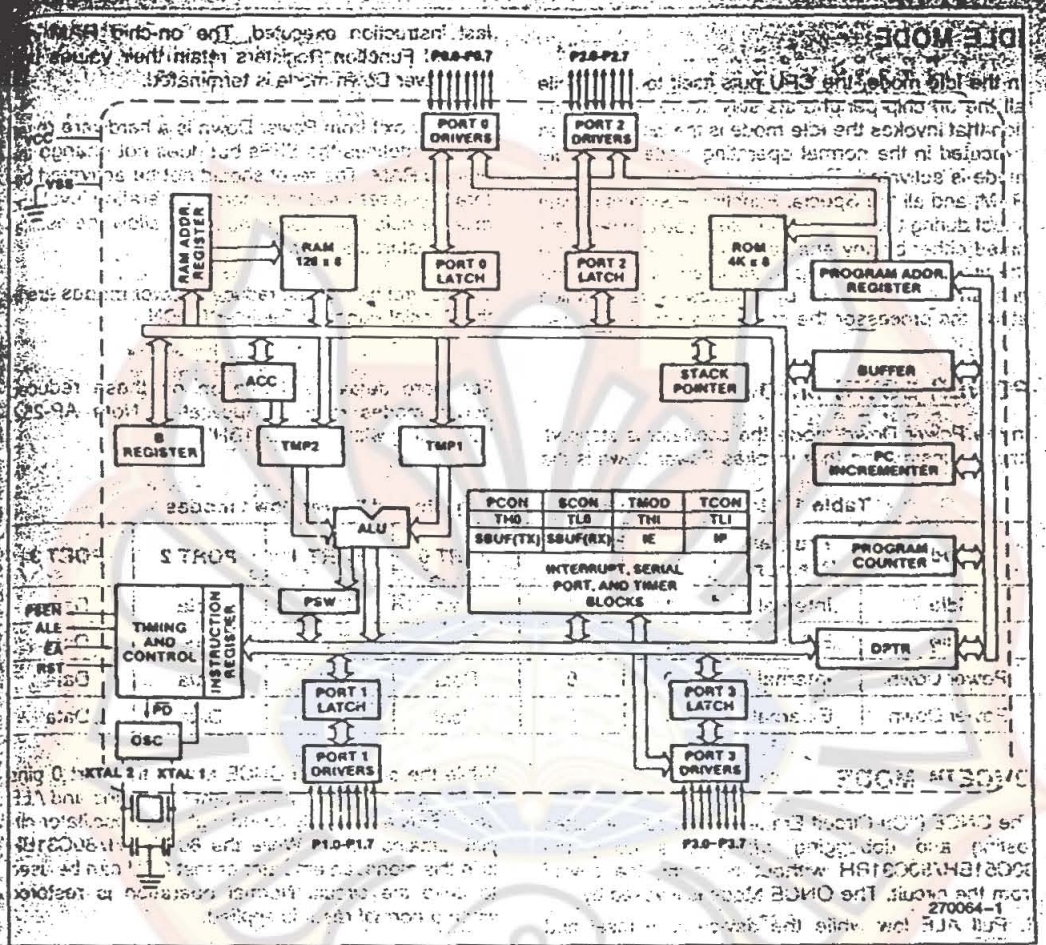


Figure 1. Block Diagram

7

IDLE MODE

In the Idle mode, the CPU puts itself to sleep while all the on chip peripherals stay active. The instruction that invokes the Idle mode is the last instruction executed in the normal operating mode before Idle mode is activated. The content of CPU, the on chip RAM, and all the Special Function Registers remain intact during this mode. The Idle mode can be terminated either by any enabled interrupt, at which time the process is picked up at the interrupt service routine and continued, or by a hardware reset which starts the processor the same as a power on reset.

POWER DOWN MODE

In the Power Down mode the oscillator is stopped, and the instruction that invokes Power Down is the last instruction executed. The on-chip RAM Special Function Registers retain their value the Power Down mode is terminated.

The only exit from Power Down is a hardware r Reset redefines the SFRs but does not change on-chip RAM. The reset should not be activated fore V_{CC} is restored to its normal operating level must be held active long enough to allow the osc tor to restart and stabilize.

The control bits for the reduced power modes are the Special Function Register PCON.

NOTE:
For more detailed information on these reduc power modes refer to Application Note AP-252 "Designing with the 80C51BH".

Table 1. Status of the external pins during Idle and Power Down modes

Mode	Program Memory	ALE	PSEN	PORT 0	PORT 1	PORT 2	PORT 3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power Down	Internal	0	0	Data	Data	Data	Data
Power Down	External	0	0	Float	Data	Data	Data

ONCE™ MODE

The ONCE ("On-Circuit Emulation") Mode facilitates testing and debugging of systems using the 80C51BH/80C31BH without removing the device from the circuit. The ONCE Mode is invoked by:

1. Pull ALE low while the device is in reset and $\overline{PSEN}$ is high;
2. Hold ALE low as RST is deactivated.

While the device is in ONCE Mode, the Port 0 pins go into a float state, and the other port pins and ALE and $\overline{PSEN}$ are weakly pulled high. The oscillator circuit remains active. While the 80C51BH/80C31BH is in this mode, an emulator or test CPU can be used to drive the circuit. Normal operation is restored when a normal reset is applied.

PACKAGES

Part	Prefix	Package Type
80C51BH/ 80C31BH*	P	40-Pin Plastic DIP
	D	40-Pin CERDIP
	N	44-Pin PLCC
	S	44-Pin QFP

*The 80C51BH-1, 80C51BH-2, 80C31BH-1, and 80C31BH-2 have the same package types.

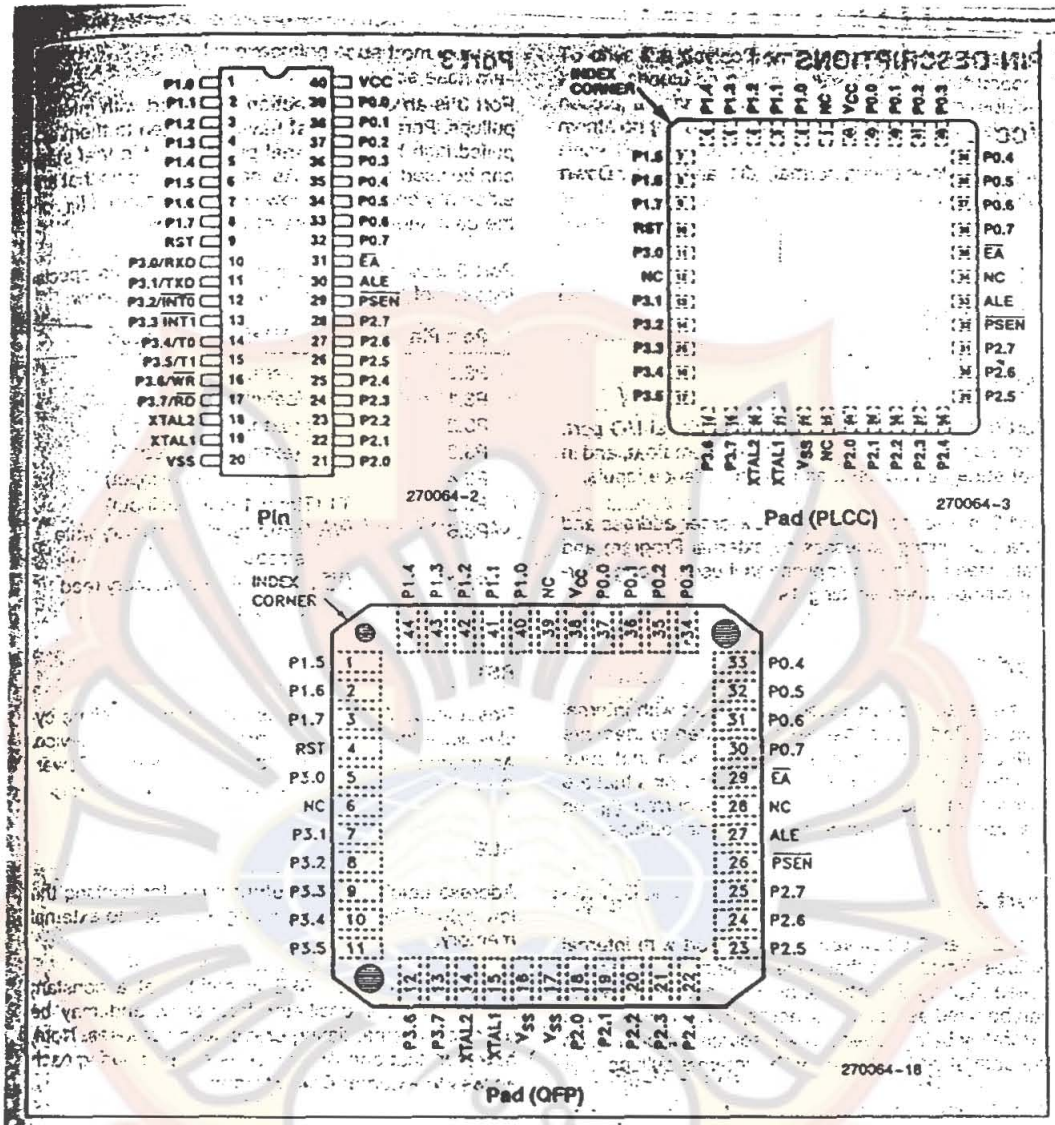


Figure 2. Connection Diagrams

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias ..... 0°C to +70°C

Storage Temperature ..... −65°C to +150°C

Voltage on any Pin to V_{SS} ..... −0.5V to V_{CC} +0.5V

Voltage on V_{CC} to V_{SS} ..... −0.5V to 6.5V

Maximum I_{OL} per I/O pin ..... 15 mA

Power Dissipation 1.0W*

*This value is based on the maximum allowable die temperature and the thermal resistance of the package.

NOTICE: This data sheet contains preliminary information on new products in production. The specifications are subject to change without notice. Verify with your local Intel Sales office that you have the latest data sheet before finalizing a design.

***WARNING:** *Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operation beyond the "Operating Conditions" is not recommended and extended exposure beyond the "Operating Conditions" may affect device reliability.*

Operating Conditions:

T_A (under Bias) = 0°C to +70°C; V_{CC} = 5V ±20%; V_{SS} = 0V

D.C. CHARACTERISTICS (under Operating Conditions)

Symbol	Parameter	Min	Typ(3)	Max	Unit	Test Conditions
V_{IL}	Input Low Voltage (Except $\overline{EA}$)	−0.5		0.2 V_{CC} −0.1	V	
V_{IL1}	Input Low Voltage ($\overline{EA}$)	−0.5		0.2 V_{CC} − 0.3	V	
V_{IH}	Input High Voltage (Except XTAL1, RST)	0.2 V_{CC} + 0.9		V_{CC} + 0.5	V	
V_{IH1}	Input High Voltage (XTAL1, RST)	0.7 V_{CC}		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage (5) (Ports 1, 2, 3)			0.45	V	I_{OL} = 1.6 mA (1)
V_{OL1}	Output Low Voltage (6) (Port 0, ALE, $\overline{PSEN}$)			0.45	V	I_{CL} = 3.2 mA (1)
V_{OH}	Output High Voltage (Ports 1, 2, 3, ALE, $\overline{PSEN}$)	2.4			V	I_{OH} = −60 µA V_{CC} = 5V ±10%
		0.75 V_{CC}			V	I_{OH} = −25 µA
		0.9 V_{CC}			V	I_{OH} = −10 µA
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode)	2.4			V	I_{OH} = −800 µA V_{CC} = 5V ±10%
		0.75 V_{CC}			V	I_{OH} = −300 µA
		0.9 V_{CC}			V	I_{OH} = −80 µA (2)
I_{IL}	Logical 0 Input Current (Ports 1, 2, 3)			−50	µA	V_{IN} = 0.45V
I_{TL}	Logical 1 to 0 Transition Current (Ports 1, 2, 3)			−650	µA	V_{IN} = 2V
I_{LI}	Input Leakage Current (Port 0, $\overline{EA}$)			±10	µA	0.45 < V_{IN} < V_{CC}
RRST	Reset Pulldown Resistor	50		150	KΩ	
CIO	Pin Capacitance			10	pF	Test Freq = 1 MHz, T_A = 25°C
I_{CC}	Power Supply Current: Active Mode, 12 MHz (4)		11	20	mA	(5)
	Idle Mode, 12 MHz (4)		1.7	5	mA	
	Power Down Mode		5	50	µA	

NOTES:

1. Capacitive loading on Ports 0 and 2 may cause spurious noise pulses to be superimposed on the V_{OL}s of ALE and Ports 1 and 3. The noise is due to external bus capacitance discharging into the Port 0 and Port 2 pins when these pins make 1-to-0 transitions during bus operations. In the worst cases (capacitive loading > 100 pF), the noise pulse on the ALE line may exceed 0.8V. In such cases it may be desirable to qualify ALE with a Schmitt Trigger, or use an address latch with a Schmitt Trigger STROBE input.
2. Capacitive loading on Ports 0 and 2 may cause the V_{OH} on ALE and $\overline{PSEN}$ to momentarily fall below the 0.9 V_{CC} specification when the address bits are stabilizing.
3. "Typicals" are based on a limited number of samples taken from early manufacturing lots and are not guaranteed. The values listed are at room temperature, 5V.
4. ICCMAX at other frequencies is given by

   Active Mode: ICCMAX = 1.47 × FREQ + 2.35

   Idle Mode: ICCMAX = 0.33 × FREQ + 1.05

   where FREQ is the external oscillator frequency in MHz. ICCMAX is given in mA. See Figure 5.
5. See Figures 6 through 9 for I_{CC} test conditions. Minimum V_{CC} for Power Down is 2V.
6. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:

   Maximum I_{OL} per port pin: 10 mA

   Maximum I_{OL} per 8-bit port:

   Port 0: 26 mA

   Ports 1, 2, and 3: 15 mA

   Maximum total I_{OL} for all output pins: 71 mA

If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

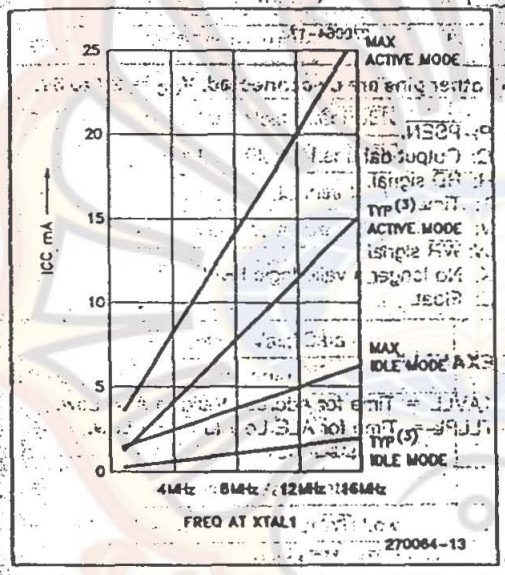


Figure 5. I_{CC} vs. Frequency
Valid only within frequency specifications of the device under test.

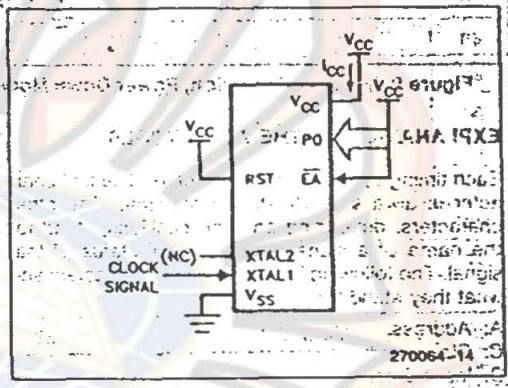


Figure 6. I_{CC} Test Condition, Active Mode
All other pins are disconnected.

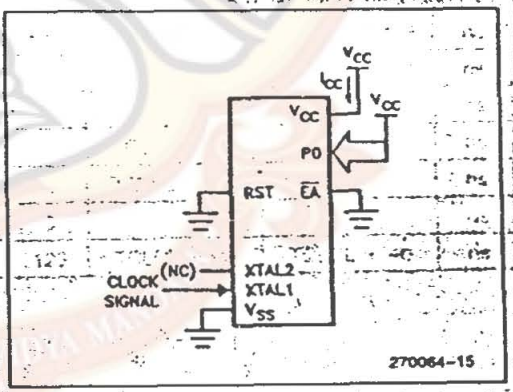


Figure 7. I_{CC} Test Condition, Idle Mode
All other pins are disconnected.

National Semiconductor

LM139/LM239/LM339/LM139A/LM239A/LM339A/ LM2901/LM3302 Low Power Low Offset Voltage Quad Comparators

General Description

The LM139 series consists of four independent precision voltage comparators with an offset voltage specification as low as 2 mV max for all four comparators. These were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common-mode voltage range includes ground, even though operated from a single power supply voltage.

Application areas include limit comparators, simple analog to digital converters; pulse, squarewave and time delay generators; wide range VCO; MOS clock timers; multivibrators and high voltage digital logic gates. The LM139 series was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, they will directly interface with MOS logic— where the low power drain of the LM339 is a distinct advantage over standard comparators.

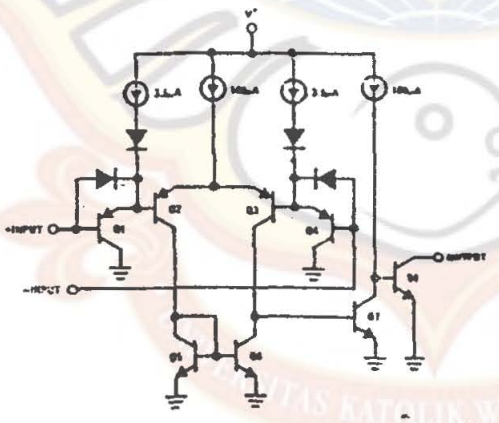
Advantages

- High precision comparators
- Reduced V_{OS} drift over temperature
- Eliminates need for dual supplies
- Allows sensing near GND
- Compatible with all forms of logic
- Power drain suitable for battery operation

Features

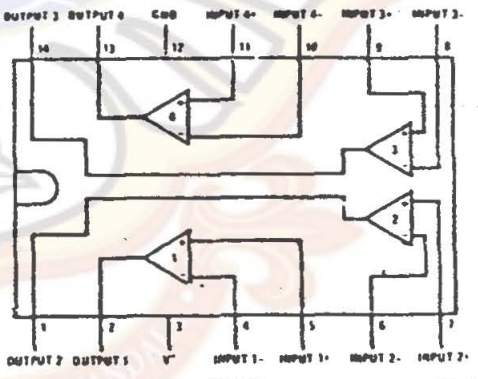
- Wide single supply voltage range of dual supplies
  LM139 series. 2 V_{DC} to 36 V_{DC} or
  LM139A series, LM2901 ±1 V_{DC} to ±18 V_{DC}
  LM3302 2 V_{DC} to 28 V_{DC}
  or ±1 V_{DC} to ±14 V_{DC}
- Very low supply current drain (0.8 mA) — independent of supply voltage
- Low input biasing current 25 nA
- Low input offset current ±5 nA
- and offset voltage ±3 mV
- Input common-mode voltage range includes GND
- Differential input voltage range equal to the power supply voltage
- Low output saturation voltage 250 mV at 4 mA
- Output voltage compatible with TTL, DTL, ECL, MOS and CMOS logic systems

Schematic and Connection Diagrams



TL/H/5706–1

Dual-In-Line Package



TOP VIEW TL/H/5706–2

Order Number LM139J, LM139AJ, LM239J, LM239AJ, LM339J, LM339AJ, LM2901J or LM3302J
See NS Package Number J14A
Order Number LM339AM, LM339M or LM2901M
See NS Package Number M14A
Order Number LM339N, LM339AN, LM2901N or LM3302N
See NS Package Number N14A

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 10)

	LM139/LM239/LM339 LM139A/LM239A/LM339A LM2901	LM3302
Supply Voltage, V^+	36 V_{DC} or ±18 V_{DC}	28 V_{DC} or ±14 V_{DC}
Differential Input Voltage (Note 8)	36 V_{DC}	28 V_{DC}
Input Voltage	−0.3 V_{DC} to +36 V_{DC}	−0.3 V_{DC} to +28 V_{DC}
Input Current (V_{IN} < −0.3 V_{DC}), (Note 3)	50 mA	50 mA
Power Dissipation (Note 1)		
Molded DIP	1050 mW	1050 mW
Cavity DIP	1190 mW	
Small Outline Package	760 mW	
Output Short-Circuit to GND, (Note 2)	Continuous	Continuous
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	260°C	260°C

	LM139/LM239/LM339 LM139A/LM239A/LM339A LM2901	LM3302
Operating Temperature Range		−40°C to +85°C
LM339/LM339A	0°C to +70°C	
LM239/LM239A	−25°C to +85°C	
LM2901	−40°C to +85°C	
LM139/LM139A	−55°C to +125°C	
Soldering Information		
Dual-In-Line Package		
Soldering (10 seconds)	260°C	260°C
Small Outline Package		
Vapor Phase (60 seconds)	215°C	215°C
Infrared (15 seconds)	220°C	220°C
ESD rating (1.5 kΩ in series with 100 pF)	600V	600V

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics (V^+ = 5 V_{DC}, T_A = 25°C, unless otherwise stated)

Parameter	Conditions	LM139A			LM239A, LM339A			LM139			LM239, LM339			LM2901			LM3302			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	(Note 9)		±1.0	±2.0		±1.0	±2.0		±2.0	±5.0		±2.0	±5.0		±2.0	±7.0		±3	±30	mV
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$ with Output in Linear Range, (Note 5), V_{CM} = 0V		25	100		25	250		25	100		25	250		25	250		25	500	nA
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$, V_{CM} = 0V		±3.0	±25		±5.0	±50		±3.0	±25		±5.0	±50		±5	±50		±3	±100	nA
Input Common-Mode Voltage Range	V^+ = 30 V_{DC} (LM3302, V^+ = 28 V_{DC}) (Note 8)	0		$V^+ - 1.5$	0		$V^+ - 1.5$	0		$V^+ - 1.5$	0		$V^+ - 1.5$	0		$V^+ - 1.5$	0		$V^+ - 1.5$	V
Supply Current	R_L = ∞ on all Comparators, R_L = ∞, V^+ = 36V, (LM3302, V^+ = 28 V_{DC})		0.8	2.0		0.8	2.0		0.8	2.0		0.8	2.0		0.8	2.0		0.8	2.0	mA
			1.0	2.5		1.0	2.5		1.0	2.5		1.0	2.5		1.0	2.5		1.0	2.5	mA
Voltage Gain	R_L ≥ 15 kΩ, V^+ = 15 V_{DC}, V_O = 1 V_{DC} to 11 V_{DC}	50	200		50	200		50	200		50	200		25	100		2	30		V/mV
Large Signal Response Time	V_{IN} = TTL Logic Swing, V_{REF} = 1.4 V_{DC}, V_{RL} = 5 V_{DC}, R_L = 5.1 kΩ,		300			300			300			300			300			300		ns
Response Time	V_{RL} = 5 V_{DC}, R_L = 5.1 kΩ, (Note 7)		1.3			1.3			1.3			1.3			1.3			1.3		μs
Output Sink Current	$V_{IN(-)}$ = 1 V_{DC}, $V_{IN(+)}$ = 0, V_O ≤ 1.5 V_{DC}	6.0	16		6.0	16		6.0	16		6.0	16		6.0	16		6.0	16		mA

Electrical Characteristics ($V^+ = 5\ V_{DC}$, $T_A = 25°C$, unless otherwise stated) (Continued)

Parameter	Conditions	LM139A			LM239A, LM339A			LM139			LM239, LM339			LM2901			LM3302			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Saturation Voltage	$V_{IN(-)} = 1\ V_{DC}$, $V_{IN(+)} = 0$, $I_{SINK} \leq 4\ mA$		250	400		250	400		250	400		250	400		250	400		250	500	mV_{DC}
Output Leakage Current	$V_{IN(+)} = 1\ V_{DC}$, $V_{IN(-)} = 0$, $V_O = 5\ V_{DC}$		0.1			0.1			0.1			0.1			0.1			0.1		nA_{DC}

Electrical Characteristics ($V^+ = 5.0\ V_{DC}$, Note 4)

Parameter	Conditions	LM139A			LM239A, LM339A			LM139			LM239, LM339			LM2901			LM3302			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage	(Note 9)			±4.0			±4.0			±9.0			±9.0		±9	±15			±40	mV_{DC}
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$, $V_{CM} = 0V$			±100			±150			±100			±150		±50	±200			±300	nA_{DC}
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$ with Output in Linear Range, $V_{CM} = 0V$ (Note 5)			300			400			300			400		200	500			1000	nA_{DC}
Input Common-Mode Voltage Range	$V^+ = 30\ V_{DC}$ (LM3302, $V^+ = 28\ V_{DC}$) (Note 6)	0		$V^+ - 2.0$	0		$V^+ - 2.0$	0		$V^+ - 2.0$			$V^+ - 2.0$	0		$V^+ - 2.0$	0		$V^+ - 2.0$	V_{DC}
Saturation Voltage	$V_{IN(-)} = 1\ V_{DC}$, $V_{IN(+)} = 0$, $I_{SINK} \leq 4\ mA$			700			700			700			700		400	700			700	mV_{DC}
Output Leakage Current	$V_{IN(+)} = 1\ V_{DC}$, $V_{IN(-)} = 0$, $V_O = 30\ V_{DC}$, (LM3302, $V_O = 28\ V_{DC}$)			1.0			1.0			1.0			1.0			1.0			1.0	μA_{DC}
Differential Input Voltage	Keep all V_{IN}'s $\geq 0\ V_{DC}$ (or V^-, if used), (Note 8)			36			36			36			36			36			28	V_{DC}

Note 1: For operating at high temperatures, the LM339/LM339A, LM2901, LM3302 must be derated based on a 125°C maximum junction temperature and a thermal resistance of 95°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM239 and LM139 must be derated based on a 150°C maximum junction temperature. The low bias dissipation and the "ON-OFF" characteristic of the outputs keeps the chip dissipation very small ($P_D \leq 100$ mW), provided the output transistors are allowed to saturate.

Note 2: Short circuits from the output to V^+ can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately 20 mA independent of the magnitude of V^+.

Note 3: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than $-0.3\ V_{DC}$ (at 25°C).

Note 4: These specifications are limited to $-55°C \leq T_A \leq +125°C$, for the LM139/LM139A. With the LM239/LM239A, all temperature specifications are limited to $-25°C \leq T_A \leq +85°C$, the LM339/LM339A temperature specifications are limited to $0°C \leq T_A \leq +70°C$, and the LM2901, LM3302 temperature range is $-40°C \leq T_A \leq +85°C$.

Note 5: The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.

Note 6: The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is $V^+ - 1.5V$ at 25°C, but either or both inputs can go to $+30\ V_{DC}$ without damage (25V for LM3302), independent of the magnitude of V^+.

Note 7: The response time specified is a 100 mV input step with 5 mV overdrive. For larger overdrive signals 300 ns can be obtained, see typical performance characteristics section.

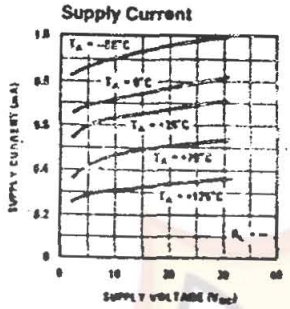
Note 8: Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than $-0.3\ V_{DC}$ (or $0.3\ V_{DC}$ below the magnitude of the negative power supply, if used) (at 25°C).

Note 9: At output switch point, $V_O = 1.4\ V_{DC}$, $R_S = 0\Omega$ with V^+ from $5\ V_{DC}$ to $30\ V_{DC}$ and over the full input common-mode range ($0\ V_{DC}$ to $V^+ - 1.5\ V_{DC}$), at 25°C. For LM3302, V^+ from $5\ V_{DC}$ to $28\ V_{DC}$.

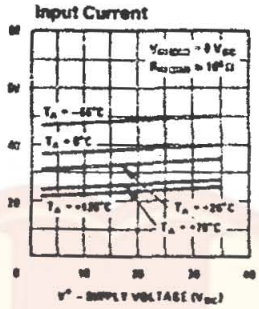
Note 10: Refer to RETS139AX for LM139AJ military specifications and to RETS139X for LM139J military specifications.

Typical Performance Characteristics LM139/LM239/LM339, LM139A/LM239A/LM339A, LM3302

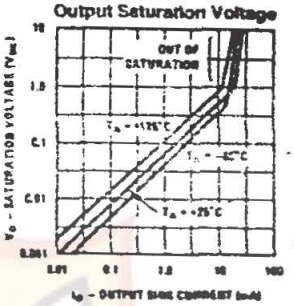
Supply Current



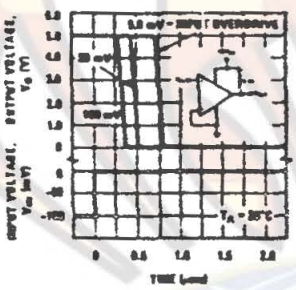
Input Current



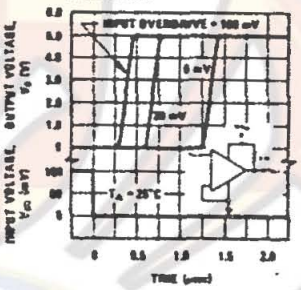
Output Saturation Voltage



Response Time for Various Input Overdrives—Negative Transition



Response Time for Various Input Overdrives—Positive Transition



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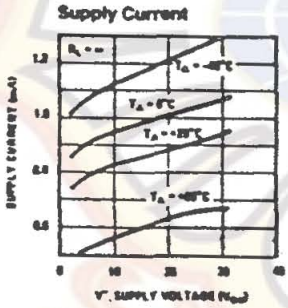
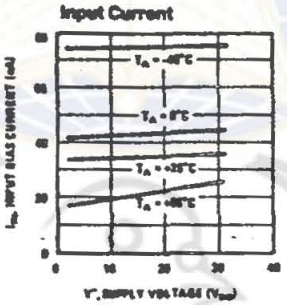
Typical Performance Characteristics LM2901

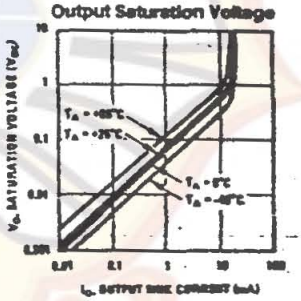
Supply Current



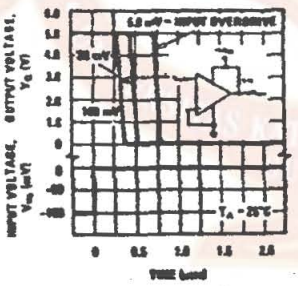
Input Current



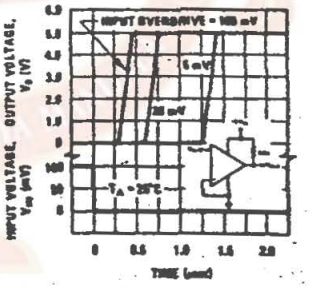
Output Saturation Voltage



Response Time for Various Input Overdrives-Negative Transition



Response Time for Various Input Overdrives-Positive Transition



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