LAMPIRAN

Lampiran 1

***Listing* Program Pemancar**

```
$mod51

;---------------
;port definition
;---------------
d0_mt equ    p0.0
d1_mt equ    p0.1
d2_mt equ    p0.2
d3_mt equ    p0.3
angkat equ   p0.4
rd_mt  equ   p2.0
rs0_mt       equ     p2.1
wr_mt equ    p2.2
cs_mt  equ   p2.3
 ;---------------------

delay_3      equ     18h
delay_2      equ     19h
delay_1      equ     20h

org    0000h
acall  reset
ajmp   start


       org     100h

scanKeypad:
       MOV P3,#11101111B
       MOV A,P3
       ANL A,#00001111B
CEK_1:
       CJNE A,#00001110B,CEK_2
       MOV  R0,#1
       ajmp keluarScanning
CEK_2:
       CJNE A,#00001101B,CEK_3
       MOV  R0,#4
       ajmp keluarScanning
CEK_3:
       CJNE A,#00001011B,CEK_COR
```

```
        MOV  R0,#7
        ajmp keluarScanning
CEK_COR:
        CJNE A,#00000111B,CEK_BARIS2
        MOV  R0,#14
        ajmp keluarScanning


CEK_BARIS2:
        MOV P3,#11011111B
        MOV A,P3
        ANL A,#00001111B
CEK_4:
        CJNE A,#00001110B,CEK_5
        MOV  R0,#2
        ajmp keluarScanning
CEK_5:
        CJNE A,#00001101B,CEK_6
        MOV R0,#5
        ajmp keluarScanning
CEK_6:
        CJNE A,#00001011B,CEK_MEN
        MOV R0,#8
        ajmp keluarScanning
CEK_MEN:
        CJNE A,#00000111B,CEK_BARIS3
        MOV R0,#0
        ajmp keluarScanning

CEK_BARIS3:
        MOV P3,#10111111B
        MOV A,P3
        ANL A,#00001111B
CEK_7:
        CJNE A,#00001110B,CEK_8
        MOV  R0,#3
        ajmp keluarScanning
CEK_8:
        CJNE A,#00001101B,CEK_9
        MOV R0,#6
        ajmp keluarScanning
CEK_9:
        CJNE A,#00001011B,CEK_ATAS
        MOV R0,#9
        ajmp keluarScanning
CEK_ATAS:
```

```
        CJNE A,#00000111B,CEK_BARIS4
        MOV R0,#15
        ajmp keluarScanning


CEK_BARIS4:
        MOV P3,#01111111B
        MOV A,P3
        ANL A,#00001111B
CEK_CAN:
        CJNE A,#00001110B,CEK_0
        MOV  R0,#11
        ajmp keluarScanning
CEK_0:
        CJNE A,#00001101B,CEK_ENT
        MOV R0,#12
        ajmp keluarScanning
CEK_ENT:
        CJNE A,#00001011B,CEK_BAWAH
        MOV R0,#13
        ajmp keluarScanning
CEK_BAWAH:
        CJNE A,#00000111B,TIDAKADA
        MOV R0,#16
        ajmp keluarScanning

TIDAKADA:
        MOV R0,#10

keluarScanning :
;PROGRAM TRANSMITTER        ;
;PROGRAM LCD;
ret
 ;-------------------
 ;write_8888
 ;-------------------
 wr_8888:
                clr     cs_mt                                   ;cs active low,
    mov         rs0_mt,c        ;rs0 = 0, reg data, rs0=1, reg kontrol
    anl p0,#0f0h                                        ; p1 = 00001111
    anl a,#0fh
    orl p0,a                                            ;00001111 or 00001111 = 00001111
    setb        wr_mt
    clr wr_mt
    setb        wr_mt
    setb        rs0_mt
```

```
    setb    cs_mt                                   ;tulis ke register kontrol
selesai
    ret

;------------------
;read_8888
;------------------
rd_8888:
            orl     p0,#0fh                         ; 11111111 or 00001111 =
11111111 = p1
            clr     cs_mt                                   ;cs active low,
            mov     rs0_mt,c                                ;baca register
status
            setb    rd_mt
            clr     rd_mt
            mov     a,p0
            setb    rd_mt
            anl     a,#0fh              ; 11111111 and 00001111 = 00001111 = a
            setb    rs0_mt
            setb    cs_mt                                   ;baca register status
selesai
            ret

;------------------
;send_8888
;------------------
sd_8888:
            clr     c                               ;send reg data
            acall wr_8888
            setb    c
            mov     a,#01h              ;kirim data (Tout)
            acall   wr_8888
            acall   delay500ms
            setb    c
            mov     a,#00h              ;Tout mati
            acall   wr_8888
            acall   delay500ms
            ret

;------------------
;receive_8888
;------------------
;rc_8888:
;clr    c
;acall rd_8888
;setb   c
```

```
;
jnb acc.2,esc_rc_8888 ;karena bit2 register status set=ada baru diambill
;mov  a,#04h ; IRQ = 1 di register A
;acall  rd_8888
;acall  delay500ms
;setb  c
;mov  a,#00h
;acall  rd_8888
;acall  delay500ms
;esc_rc_8888: ret



;------------------
;init_8888
;------------------
init_8888:
                setb    c                               ;
                acall   rd_8888
                setb    c
                mov     a,#0
                acall   wr_8888
                setb    c
                mov     a,#0
                acall   wr_8888
                setb    c
                mov     a,#08h
                acall   wr_8888
                setb    c
                mov     a,#01h                  ;reg kontrol A burst disable
                acall   wr_8888
                setb    c
                acall   rd_8888
                ret

;------------------
;delay
;------------------
delay500ms   :
                                                mov     delay_3,#4
delay1 :                mov     delay_2,#255
delay2   :                      mov     delay_1,#225
                                                djnz    delay_1,$
```

```
                djnz    delay_2,delay2

                djnz    delay_3,delay1

                ret

delay100ms:     mov     delay_2,#200
loop_delay100ms: mov    delay_1,#250
                djnz    delay_1,$
                djnz    delay_2,loop_delay100ms
                ret


;-------------------------
;procedure program
;-------------------------

reset:
        mov     a,#00h
        mov     p0,#00h
        mov     p1,#00h
        mov     p2,#00h
;       mov     a,#00h
;       mov     r0,#00h
;       mov     r1,#00h
;       mov     r2,#00h
        ret

;---------------------------

;org 4000h      ;inisialisasi lcd

;rs bit p2.5
;rw bit p2.6


                ;org     00h
                ;ljmp    start

                ;

                InitLCD:
                acall   delay4m
                acall   delay4m
                acall   delay4m
                ACALL       Delay4m
```

```
        acall   delay4m

        Mov     a,#00110000B
        ACALL   CommandLCD
        acall   delay4m

        Mov     a,#00110000B
        ACALL   CommandLCD
        acall   delay4m

        Mov     a,#00110000B
        ACALL   CommandLCD

        Mov     a,#00110000B
        ACALL   CommandLCD


        Mov     a,#00111000B    ;Function Set 8 bit     ;N = 2 Lines    ;F =
        5x8 DotMatrix
        ACALL   CommandLCD              ;N = 2 Lines ;F = 5x8
        DotMatrix

        Mov     a,#00001110B    ;Display On     ; D=On C=On B=Off
        ACALL   CommandLCD              ; D=On C=On B=Off


        Mov     a,#00000001B    ;Display Clear
        ACALLCommandLCD
        acall   delay4m

        Mov     a,#00000110B    ;Entry Mode Set     ;I/D = Inc      ;S =
        No Display Shift (Off)
        ACALL   CommandLCD              ;I/D = Inc
                                ;S  = No Display Shift (Off)

        Mov     a,#00000001B    ;Display Clear
        ACALL   CommandLCD
        acall   delay4m
        Mov     a,#00001101B    ;Display On     ; D=On C=On B=Off
        ACALL   CommandLCD              ; D=On C=On B=Off

        RET

CommandLCD:
        MOV  P1,A
        clr     p2.5
```

```
                setb    p2.7
                nop
                nop
                nop
                nop
                nop
                nop
                clr     p2.7
                MOV             R3,#100
                DJNZ    R3,$
                RET

WriteLCD:
                MOV     P1,A
                setb    p2.5
                setb    p2.7
                nop
                nop
                nop
                nop
                nop
                nop
                clr     p2.7
                MOV             R3,#100
                DJNZ    R3,$
                RET

DELAY4M:
;               push    03h
;               push    02h
                MOV             R2,#255
DEL4M:                  MOV             R3,#255
                DJNZ    R3,$
                DJNZ    R2,DEL4M
;               pop     02h
;               pop     03h
                RET

WriteString:
        CLR     A
        MOVC            A,@A+DPTR
        JZ      EndWriteString
        acall   writelcd
        INC     DPTR
        ajmp    WriteString
EndWriteString:
```

```
        RET

Delay:
        push 07h
        push 06h
        push 05h
        MOV  R5,#1H
delay1x:
        MOV  R6,#020H
Delay0:
        MOV  R7,#0ffH
        DJNZ R7,$
        DJNZ R6,Delay0
        DJNZ R5,Delay1x
        pop 05h
        pop 06h
        pop 07h
        RET

lDelay:
        push 07h
        push 06h
        push 05h
        MOV  R5,#4H
ldelay1:
        MOV  R6,#0ffH
lDelay0:
        MOV  R7,#0ffH
        DJNZ R7,$
        DJNZ R6,lDelay0
        DJNZ R5,lDelay1
        pop 05h
        pop 06h
        pop 07h
        RET
go:

        mov    a,#080h
               acall   commandlcd
               mov     dptr,#comman1
               acall   writestring

               mov     a,#0c0h
               acall   commandlcd
               mov     dptr,#comman2
               acall   writestring
```

```
                ret

oke:

                ajmp    oke

comman1:        db      'TX System',0
comman2:        db      'Press Menu!',0

;------------------
;main program
;------------------

start:


        mov     ie,#0
        MOV     SP,#60H
        clr     p2.6            ;rw

        acall   delay500ms
        acall   delay500ms
        acall   delay500ms
        acall   delay500ms
        acall   init_8888


        acall   ldelay
        lcall   initlcd

                Mov     a,#89H
                ACALL   CommandLCD

                ;Mov    a,#'A'
                ;ACALL  WriteLCD

                mov     a,#080h
                acall   commandlcd
                mov     dptr,#comman1
                acall   writestring

                mov     a,#0c0h
                acall   commandlcd
                mov     dptr,#comman2
                acall   writestring
```

```
kirim:
        acall   delay500ms
        ;acall  delay500ms
        ;acall  delay500ms
        ;acall  delay500ms


scanLg:
 acall scankeypad
 cjne r0,#10,ada_yg_ditekan
 sjmp scanLg
ada_yg_ditekan:

        mov  a,#80h
        acall commandlcd
        mov    a,r0
        add    a,#30h
        acall writelcd

        cjne r0,#1,lihat_2
        Mov    a,#00000001B          ;Display Clear
        ACALL       CommandLCD
        acall   delay4m
                mov    a,#080h
                acall   commandlcd
                mov    dptr,#commanX
                acall   writestring
                mov    a,#0c0h
                acall   commandlcd
                mov    dptr,#commanZ
                acall   writestring

        setb p0.4
        mov    a,#1                                ;code data 1
        clr    c
        acall   sd_8888
        acall   delay500ms
        clr p0.4
        sjmp scanLg

lihat_2:
        cjne r0,#2,lihat_3
        Mov    a,#00000001B          ;Display Clear
        ACALL       CommandLCD
        acall   delay4m
        mov    a,#080h
```

```
        acall   commandlcd
        mov     dptr,#commanY
        acall   writestring

        mov     a,#0c0h
        acall   commandlcd
        mov     dptr,#commanZ
        acall   writestring

        setb p0.4
        mov     a,#2                                    ;code data 2
        clr     c
        acall   sd_8888
        acall   delay500ms
        clr p0.4
        ljmp scanLg

lihat_3:
        cjne r0,#3,lihat_4
        Mov     a,#00000001B            ;Display Clear
        ACALL           CommandLCD
        acall   delay4m
mov     a,#080h
        acall   commandlcd
        mov     dptr,#comman3
        acall   writestring

        mov     a,#0c0h
        acall   commandlcd
        mov     dptr,#commanZ
        acall   writestring


        setb p0.4
        mov     a,#3                                    ;code data 3
        clr     c
        acall   sd_8888
        acall   delay500ms
        clr p0.4
        ljmp scanLg

lihat_4:
        cjne r0,#4,lihat_5
        Mov     a,#00000001B            ;Display Clear
        ACALL           CommandLCD
        acall   delay4m
```

```
        mov   a,#080h
        acall commandlcd
        mov   dptr,#comman4
        acall writestring

        mov   a,#0c0h
        acall commandlcd
        mov   dptr,#commanZ
        acall writestring
        setb p0.4
        mov   a,#4                              ;code data 4
        clr   c
        acall sd_8888
        acall delay500ms
        clr p0.4
        ljmp scanLg

lihat_5:
        cjne r0,#5,lihat_6
        Mov   a,#00000001B          ;Display Clear
        ACALL       CommandLCD
        acall delay4m
        mov   a,#080h
        acall commandlcd
        mov   dptr,#comman5
        acall writestring

        mov   a,#0c0h
        acall commandlcd
        mov   dptr,#commanZ
        acall writestring

        setb p0.4
        mov   a,#5                              ;code data 5
        clr   c
        acall sd_8888
        acall delay500ms
        clr p0.4
        ljmp scanLg

lihat_6:
        cjne r0,#6,lihat_MEN
        Mov   a,#00000001B          ;Display Clear
        ACALL       CommandLCD
        acall delay4m
              mov   a,#080h
```

```
            acall   commandlcd
            mov     dptr,#comman6
            acall   writestring

            mov     a,#0c0h
            acall   commandlcd
            mov     dptr,#commanZ
            acall   writestring


        setb p0.4
        mov     a,#6                                ;code data 6
        clr     c
        acall   sd_8888
        acall   delay500ms
        clr p0.4
        ljmp scanLg

lihat_MEN:
        cjne r0,#12,lihat_7     ;code data 12

secara:
        Mov     a,#89H
        ACALL       CommandLCD

        ;Mov    a,#'A'
        ;ACALL      WriteLCD
        mov     a,#080h
        acall   commandlcd

        mov     dptr,#commanA
        acall   writestring
        mov     a,#0c0h
        acall   commandlcd
        mov     dptr,#commanB
        acall   writestring
        ;clr    p1
        ljmp kirim
puter:
        ajmp    puter

commanA:    db      'Insert number',0
commanB:    db      'option:',0


lihat_7:
```

```
        cjne r0,#7,lihat_8
        Mov   a,#00000001B          ;Display Clear
        ACALLCommandLCD
        acall   delay4m
        mov   a,#080h
        acall   commandlcd
        mov   dptr,#comman7
        acall   writestring

        mov   a,#0c0h
        acall   commandlcd
        mov   dptr,#commanZ
        acall   writestring


        setb p0.4
        mov   a,#7                                  ;code data 7
        clr     c
        acall   sd_8888
        acall   delay500ms
        clr p0.4
        ljmp scanLg

lihat_8:
        cjne r0,#8,lihat_9
        Mov   a,#00000001B          ;Display Clear
        ACALL       CommandLCD
        acall   delay4m
        mov   a,#080h
        acall   commandlcd
        mov   dptr,#comman8
        acall   writestring

        mov   a,#0c0h
        acall   commandlcd
        mov   dptr,#commanZ
        acall   writestring

        setb p0.4
        mov   a,#8                                  ;code data 8
        clr     c
        acall   sd_8888
        acall   delay500ms
        clr p0.4
        ljmp scanLg
```

```
lihat_9:
        cjne r0,#9,lihat_CAN
        Mov   a,#00000001B          ;Display Clear
        ACALL       CommandLCD
        acall   delay4m
                mov   a,#080h
                acall   commandlcd
                mov   dptr,#comman9
                acall   writestring

                mov   a,#0c0h
                acall   commandlcd
                mov   dptr,#commanZ
                acall   writestring

        setb p0.4
        mov   a,#9                                  ;code data 9
        clr     c
        acall   sd_8888
        acall   delay500ms
        clr p0.4
        ljmp scanLg

lihat_CAN:
        cjne r0,#14,lihat_0
        Mov   a,#89H
        ACALL       CommandLCD

        ;Mov   a,#'A'
        ;ACALL       WriteLCD
        mov   a,#080h
        acall   commandlcd

        mov   dptr,#commanHi
        acall   writestring
        mov   a,#0c0h
        acall   commandlcd
        mov   dptr,#commanLo
        acall   writestring
        setb p0.4
        mov   a,#14                                 ;code data 14
        clr     c
        acall   sd_8888
        acall   delay500ms
        clr p0.4
        ljmp scanLg
```

```
ljmp scanLg

lihat_0:
        cjne r0,#0,lihat_ENT
        Mov   a,#00000001B          ;Display Clear
        ACALL       CommandLCD
        acall   delay4m
                mov   a,#080h
                acall   commandlcd
                mov   dptr,#comman10
                acall   writestring

                mov   a,#0c0h
                acall   commandlcd
                mov   dptr,#commanZ
                acall   writestring

        setb p0.4
        mov   a,#0                                  ;code data 0
        clr     c
        acall   sd_8888
        acall   delay500ms
        clr p0.4
        ljmp scanLg
lihat_ENT:
                cjne r0,#15,lainlain
                Mov   a,#00000001B          ;Display Clear
                ACALL       CommandLCD
                acall   delay4m
                mov   a,#080h
                acall   commandlcd
                mov   dptr,#commanE
                acall   writestring

                mov   a,#0c0h
                acall   commandlcd
                mov   dptr,#commanW
                acall   writestring

        setb p0.4
        mov   a,#15                                 ;code data 15
        clr     c
        acall   sd_8888
        acall   delay500ms
        clr p0.4
        acall   delay500ms
```

```
        acall   delay500ms
        acall   delay500ms
        acall   delay500ms
        ajmp secara

lainlain:
 ljmp   kirim

 commanX:   db      'Number 1',0
 commanY:   db      'Number 2',0
 comman3:   db      'Number 3',0
 comman4:   db      'Number 4',0
 comman5:   db      'Number 5',0
 comman6:   db      'Number 6',0
 comman7:   db      'Number 7',0
 comman8:   db      'Number 8',0
 comman9:   db      'Number 9',0
 comman10:  db      'Combination',0
 commanZ:   db      'Execute?(Y/N)',0
 commanE:   db      'Executing',0
 commanW:   db      'Please wait',0
 commanHi:  db      'Insert Number ',0
 commanLo:  db      'Option:',0


 end
```

Lampiran 2

***Listing* Program Penerima**

```
$mod51

api1  equ     p0.5
api2   equ    p0.6
api3  equ     p0.7
api4   equ    p2.0
api5  equ     p2.1
api6   equ    p2.7
api7  equ     p3.0
api8  equ     p3.1
api9  equ     p3.2
api10  equ    p3.3

led1   equ    p0.0
led2   equ    p0.1
led3   equ    p0.2
led4   equ    p0.3
led5   equ    p0.4
led6   equ    p2.2
led7   equ    p2.3
led8   equ    p2.4
led9   equ    p2.5
led10  equ    p2.6

org    200h
mov    r0,#00h
mov    p0,#00h
mov    p2,#00h
mov    p1,#00h



call   clr_led
call   clr_pemantik

start:
mov    a,p1
anl    a,#0fh

cjne   a,#01h,cek1
```

```
mov     r0,a
call    clr_led
clr     led1
jmp     cek12
cek1:
cjne    a,#02h,cek2
mov     r0,a
call    clr_led
clr     led2
jmp     cek12
cek2:
cjne    a,#03h,cek3
mov     r0,a
call    clr_led
clr     led3
jmp     cek12
cek3:
cjne    a,#04h,cek4
mov     r0,a
call    clr_led
clr     led4
jmp     cek12
cek4:
cjne    a,#05h,cek5
mov     r0,a
call    clr_led
clr     led5
jmp     cek12
cek5:
cjne    a,#06h,cek6
mov     r0,a
call    clr_led
clr     led6
jmp     cek12
cek6:
cjne    a,#07h,cek7
mov     r0,a
call    clr_led
clr     led7
jmp     cek12
cek7:
cjne    a,#08h,cek8
mov     r0,a
call    clr_led
clr     led8
jmp     cek12
```

```
cek8:
cjne    a,#09h,cek9
mov     r0,a
call    clr_led
clr     led9
jmp     cek12
cek9:
cjne    a,#00h,cek10 ;0
mov     r0,a
call    clr_led
call    variasi_led
jmp     cek12
cek10:
cjne    a,#0eh,cek11
mov     r0,a
call    clr_led
jmp     cek12
cek11:
cjne    a,#0fh,gak_ada
JMP     NYALAIN
gak_ada:
jmp     start
cek12:

MOV  50,A
CEKULANG:
call    delay10
MOV  A,P1
ANL  A,#0FH

CJNE  A,50,EXIT
JMP   CEKULANG
EXIT:
jmp     start

nyalain:
cjne    r0,#01h,nyalain1
setb    api1
call    delay
clr     api1
call    CLR_led
JMP   keluar
nyalain1:
cjne    r0,#02h,nyalain2
setb    api2
call    delay
```

```
clr     api2
call    CLR_led
ljmp    keluar
nyalain2:
cjne    r0,#03h,nyalain3
setb    api3
call    delay
clr     api3
call    CLR_led
ljmp    keluar
nyalain3:
cjne    r0,#04h,nyalain4
setb    api4
call    delay
clr     api4
call    CLR_led
ljmp    keluar
nyalain4:
cjne    r0,#05h,nyalain5
setb    api5
call    delay
clr     api5
call    CLR_led
ljmp    keluar
nyalain5:
cjne    r0,#06h,nyalain6
setb    api6
call    delay
clr     api6
call    CLR_led
ljmp    keluar
nyalain6:
cjne    r0,#07h,nyalain7
setb    api7
call    delay
clr     api7
call    CLR_led
ljmp    keluar
nyalain7:
cjne    r0,#08h,nyalain8
setb    api8
call    delay
clr     api8
call    CLR_led
ljmp    keluar
nyalain8:
```

```
cjne    r0,#09h,nyalain9
setb    api9
call    delay
clr     api9
call    CLR_led
ljmp    keluar
nyalain9:
cjne    r0,#00h,gak_ada2  ;0
call    variasi_pemantik
jmp     keluar
gak_ada2:
jmp     start

keluar:
call    delay10
MOV  A,P1
ANL  A,#0FH

CJNE  A,#0fh,exit2
JMP   keluar
EXIT2:
jmp     start

variasi_led:
call    delay10
clr     led1
call    delay10
clr     led2
call    delay10
clr     led3
call    delay10
clr     led4
call    delay10
clr     led5
call    delay10
clr     led6
call    delay10
clr     led7
call    delay10
clr     led8
call    delay10
clr     led9
call    delay10
clr     led10
call    delay10
ret
```

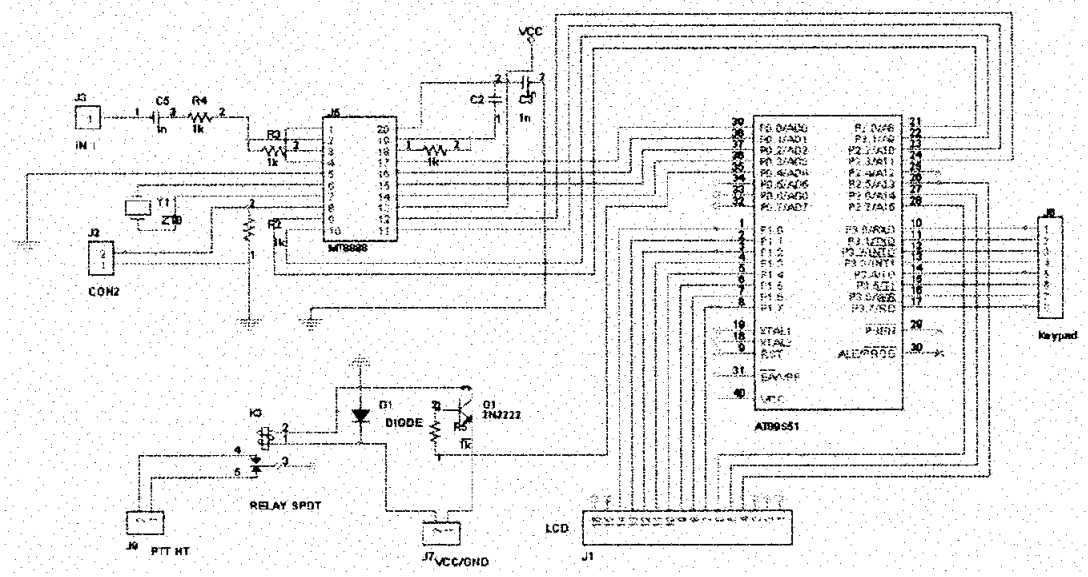
```
variasi_pemantik:
setb    api1
call    delay
clr     api1
setb    led1
setb    api2
call    delay
clr     api2
setb    led2
setb    api3
call    delay
clr     api3
setb    led3
setb    api4
call    delay
clr     api4
setb    led4
setb    api5
call    delay
clr     api5
setb    led5
setb    api6
call    delay
clr     api6
setb    led6
setb    api7
call    delay
clr     api7
setb    led7
setb    api8
call    delay
clr     api8
setb    led8
setb    api9
call    delay
clr     api9
setb    led9
setb    api10
call    delay
clr     api10
setb    led10
ret
CLR_pemantik:
clr     api1
clr     api2
```

```
clr     api3
clr     api4
clr     api5
clr     api6
clr     api7
clr     api8
clr     api9
clr     api10
ret

clr_led:
setb    led1
setb    led2
setb    led3
setb    led4
setb    led5
setb    led6
setb    led7
setb    led8
setb    led9
setb    led10
RET
delay:
mov     r3,#25
 delay1 : mov  r2,#255
 delay2 : mov  r1,#225
djnz    r1,$
djnz    r2,delay2
djnz    r3,delay1
ret

delay10:
          mov   r4,#4
delay11 :
mov     r5,#255
delay12   :             mov     r7,#225
djnz    r7,$
djnz    r5,delay12
djnz    r4,delay11
ret
end
```

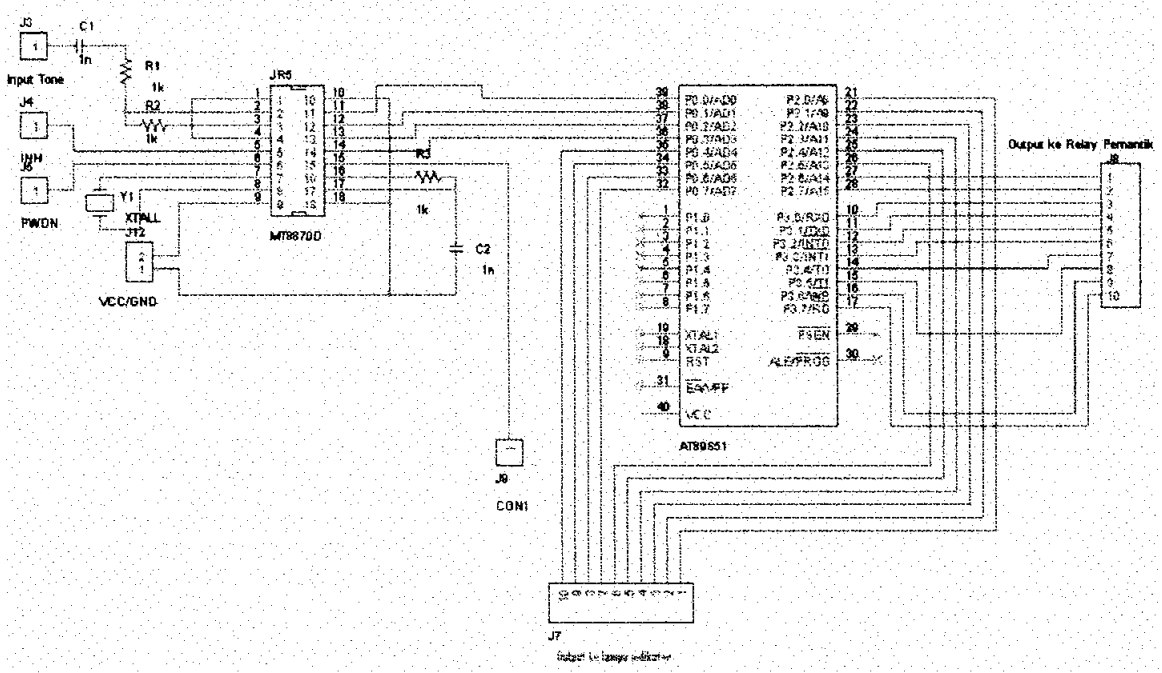
Lampiran 3

Skema Rangkaian Utama

Skema Rangkaian Utama Pemancar



Skema Rangkaian Utama Penerima



MT8888C

Integrated DTMF Transceiver with Intel Micro Interface

ISSUE 6 March 1997

Features

- Central office quality DTMF transmitter/receiver
- Low power consumption
- High speed Intel micro interface
- Adjustable guard time
- Automatic tone burst mode
- Call progress tone detection to -30dBm

Applications

- Credit card systems
- Paging systems
- Repeater systems/mobile radio
- Interconnect dialers
- Personal computers

Ordering Information

MT8888CE	20 Pin Plastic DIP
MT8888CS	20 Pin SOIC
MT8888CN	24 Pin SSOP

-40°C to +85°C

Description

The MT8888C is a monolithic DTMF transceiver with call progress filter. It is fabricated in CMOS technology offering low power consumption and high reliability.

The receiver section is based upon the industry standard MT8870 DTMF receiver while the transmitter utilizes a switched capacitor D/A converter for low distortion, high accuracy DTMF signalling. Internal counters provide a burst mode such that tone bursts can be transmitted with precise timing. A call progress filter can be selected allowing a microprocessor to analyze call progress tones.

The MT8888C utilizes an Intel micro interface, which allows the device to be connected to a number of popular microcontrollers with minimal external logic.

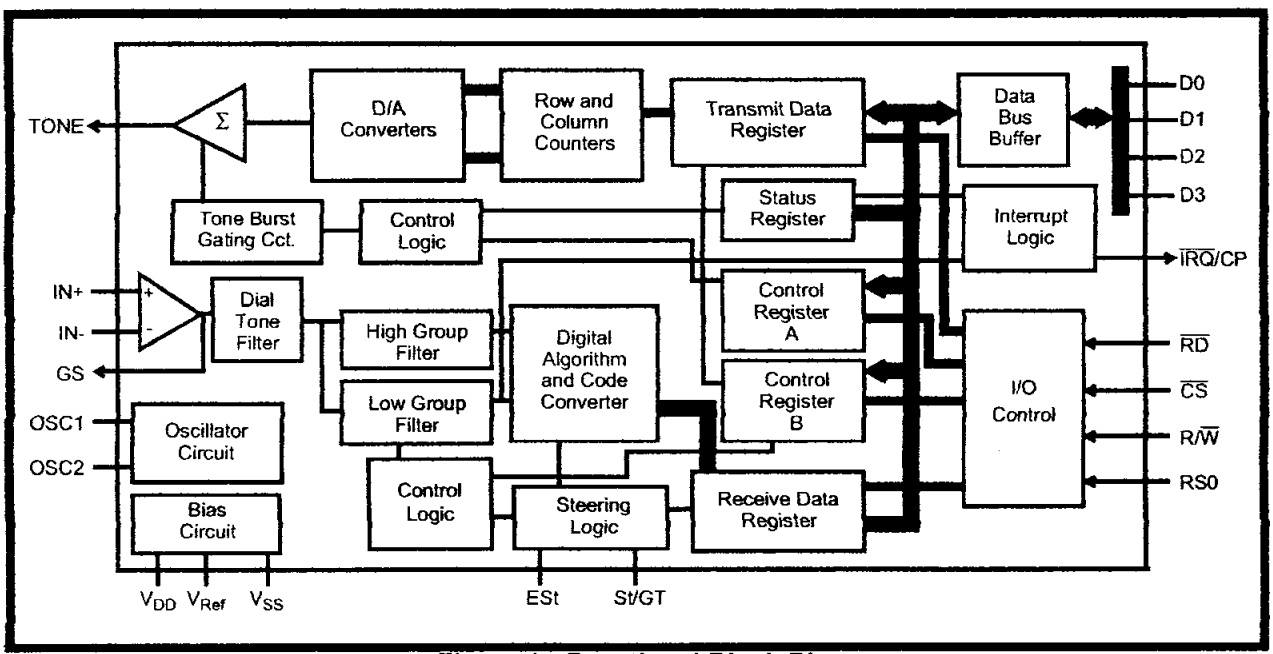


Figure 1 - Functional Block Diagram

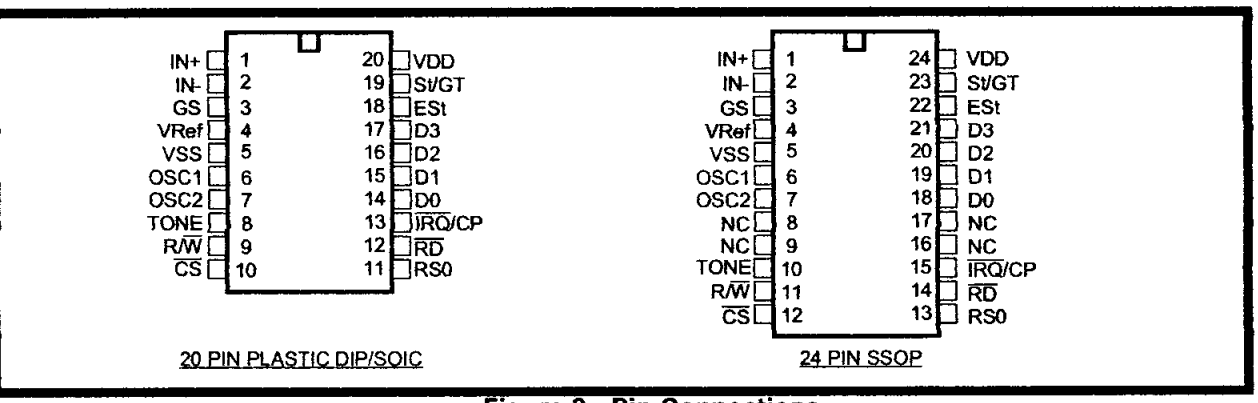


Figure 2 - Pin Connections

Pin Description

Pin #		Name	Description
20	24		
1	1	IN+	**Non-inverting** op-amp input.
2	2	IN-	**Inverting** op-amp input.
3	3	GS	**Gain Select**. Gives access to output of front end differential amplifier for connection of feedback resistor.
4	4	V_{Ref}	**Reference Voltage** output ($V_{DD}/2$).
5	5	V_{SS}	Ground (0V).
6	6	OSC1	**Oscillator** input. This pin can also be driven directly by an external clock.
7	7	OSC2	**Oscillator** output. A 3.579545 MHz crystal connected between OSC1 and OSC2 completes the internal oscillator circuit. Leave open circuit when OSC1 is driven externally.
8	10	TONE	Output from internal DTMF transmitter.
9	11	$\overline{WR}$	**Write** microprocessor input. TTL compatible.
10	12	$\overline{CS}$	**Chip Select** input. Active Low. This signal must be qualified externally by address latch enable (ALE) signal, see Figure 12.
11	13	RS0	**Register Select** input. Refer to Table 3 for bit interpretation. TTL compatible.
12	14	$\overline{RD}$	**Read** microprocessor input. TTL compatible.
13	15	$\overline{IRQ}$/ CP	**Interrupt Request/Call Progress** (open drain) output. In interrupt mode, this output goes low when a valid DTMF tone burst has been transmitted or received. In call progress mode, this pin will output a rectangular signal representative of the input signal applied at the input op-amp. The input signal must be within the bandwidth limits of the call progress filter, see Figure 8.
14-17	18-21	D0-D3	Microprocessor Data Bus. High impedance when $\overline{CS}$ = 1 or $\overline{RD}$ = 1. TTL compatible.
18	22	ESt	***Early Steering** output. Presents a logic high once the digital algorithm has detected a valid* tone pair (signal condition). Any momentary loss of signal condition will cause ESt to return to a logic low.
19	23	St/GT	**Steering Input/Guard Time** output (bidirectional). A voltage greater than V_{TSt} detected at St causes the device to register the detected tone pair and update the output latch. A voltage less than V_{TSt} frees the device to accept a new tone pair. The GT output acts to reset the external steering time-constant; its state is a function of ESt and the voltage on St.
20	24	V_{DD}	Positive power supply (5V typ.).
	8,9 16,17	NC	No Connection.

Functional Description

The MT8888C Integrated DTMF Transceiver consists of a high performance DTMF receiver with an internal gain setting amplifier and a DTMF generator which employs a burst counter to synthesize precise tone bursts and pauses. A call progress mode can be selected so that frequencies within the specified passband can be detected. The Intel micro interface allows microcontrollers, such as the 8080, 80C31/51 and 8085, to access the MT8888C internal registers.

Input Configuration

The input arrangement of the MT8888C provides a differential-input operational amplifier as well as a bias source (V_{Ref}), which is used to bias the inputs at $V_{DD}/2$. Provision is made for connection of a feedback resistor to the op-amp output (GS) for gain adjustment. In a single-ended configuration, the input pins are connected as shown in Figure 3.

Figure 4 shows the necessary connections for a differential input configuration.

Receiver Section

Separation of the low and high group tones is achieved by applying the DTMF signal to the inputs of two sixth-order switched capacitor bandpass filters, the bandwidths of which correspond to the low and high group frequencies (see Table 1). These filters incorporate notches at 350 Hz and 440 Hz for exceptional dial tone rejection. Each filter output is followed by a single order switched capacitor filter section, which smooths the signals prior to limiting. Limiting is performed by high-gain comparators which are provided with hysteresis to prevent detection of unwanted low-level signals. The outputs of the comparators provide full rail logic swings at the frequencies of the incoming DTMF signals.

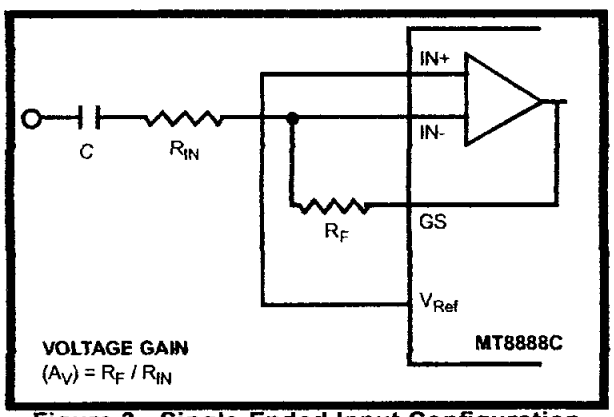


Figure 3 - Single-Ended Input Configuration

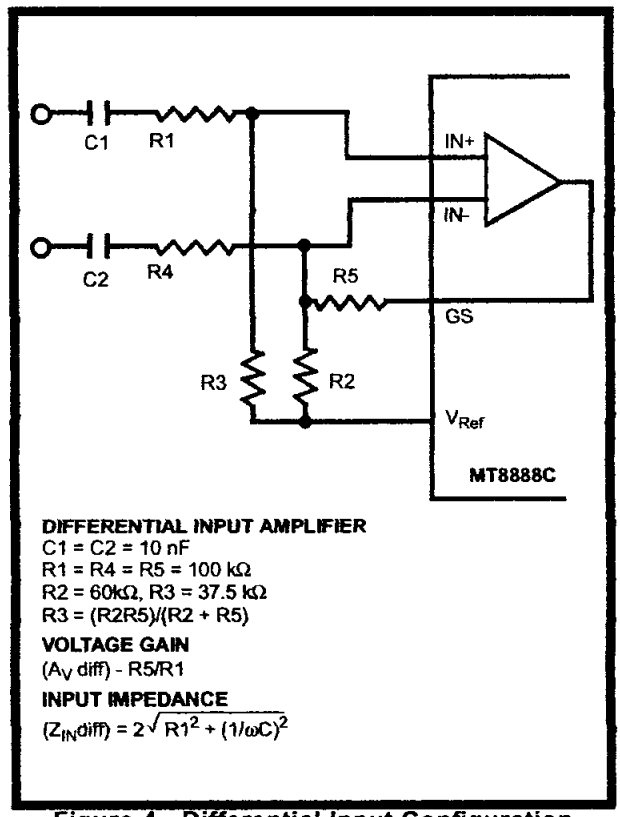


Figure 4 - Differential Input Configuration

F_{LOW}	F_{HIGH}	DIGIT	D_3	D_2	D_1	D_0
697	1209	1	0	0	0	1
697	1336	2	0	0	1	0
697	1477	3	0	0	1	1
770	1209	4	0	1	0	0
770	1336	5	0	1	0	1
770	1477	6	0	1	1	0
852	1209	7	0	1	1	1
852	1336	8	1	0	0	0
852	1477	9	1	0	0	1
941	1336	0	1	0	1	0
941	1209	*	1	0	1	1
941	1477	#	1	1	0	0
697	1633	A	1	1	0	1
770	1633	B	1	1	1	0
852	1633	C	1	1	1	1
941	1633	D	0	0	0	0

0= LOGIC LOW, 1= LOGIC HIGH

Table 1. Functional Encode/Decode Table

Following the filter section is a decoder employing digital counting techniques to determine the frequencies of the incoming tones and to verify that they correspond to standard DTMF frequencies. A complex averaging algorithm protects against tone simulation by extraneous signals such as voice while providing tolerance to small frequency deviations and variations. This averaging algorithm has been developed to ensure an optimum combination of immunity to talk-off and tolerance to the presence of interfering frequencies (third tones) and noise. When the detector recognizes the presence of two valid tones (this is referred to as the "signal condition" in some industry specifications) the "Early Steering" (ESt) output will go to an active state. Any subsequent loss of signal condition will cause ESt to assume an inactive state.

Steering Circuit

Before registration of a decoded tone pair, the receiver checks for a valid signal duration (referred to as character recognition condition). This check is performed by an external RC time constant driven by ESt. A logic high on ESt causes v_c (see Figure 5) to rise as the capacitor discharges. Provided that the signal condition is maintained (ESt remains high) for the validation period (t_{GTP}), v_c reaches the threshold (V_{TSt}) of the steering logic to register the tone pair, latching its corresponding 4-bit code (see Table 1) into the Receive Data Register. At this point the GT output is activated and drives v_c to V_{DD}. GT continues to drive high as long as ESt remains high. Finally, after a short delay to allow the output latch to settle, the delayed steering output flag goes high, signalling that a received tone pair has been registered. The status of the delayed steering flag can be monitored by checking the appropriate bit in the status register. If Interrupt mode has been selected, the $\overline{IRQ}$/CP pin will pull low when the delayed steering flag is active.

The contents of the output latch are updated on an active delayed steering transition. This data is presented to the four bit bidirectional data bus when the Receive Data Register is read. The steering circuit works in reverse to validate the interdigit pause between signals. Thus, as well as rejecting signals too short to be considered valid, the receiver will tolerate signal interruptions (drop out) too short to be considered a valid pause. This facility, together with the capability of selecting the steering time constants externally, allows the designer to tailor performance to meet a wide variety of system requirements.

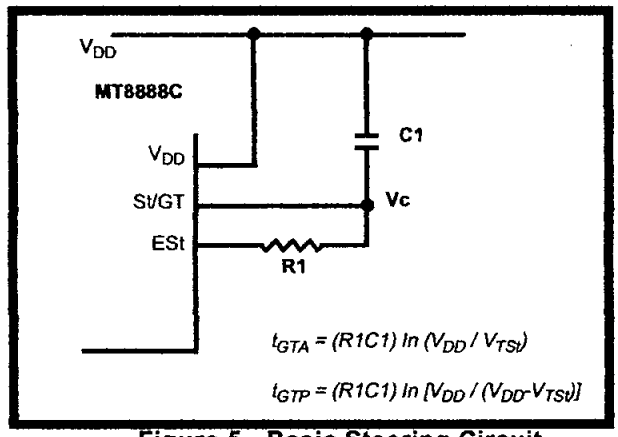


Figure 5 - Basic Steering Circuit

Guard Time Adjustment

The simple steering circuit shown in Figure 5 is adequate for most applications. Component values are chosen according to the following inequalities (see Figure 7):

$$t_{REC} \geq t_{DPmax} + t_{GTPmax} - t_{DAmin}$$
$$t_{\overline{REC}} \leq t_{DPmin} + t_{GTPmin} - t_{DAmax}$$
$$t_{ID} \geq t_{DAmax} + t_{GTAmax} - t_{DPmin}$$
$$t_{DO} \leq t_{DAmin} + t_{GTAmin} - t_{DPmax}$$

The value of t_{DP} is a device parameter (see AC Electrical Characteristics) and t_{REC} is the minimum signal duration to be recognized by the receiver. A value for C1 of 0.1 µF is recommended for most

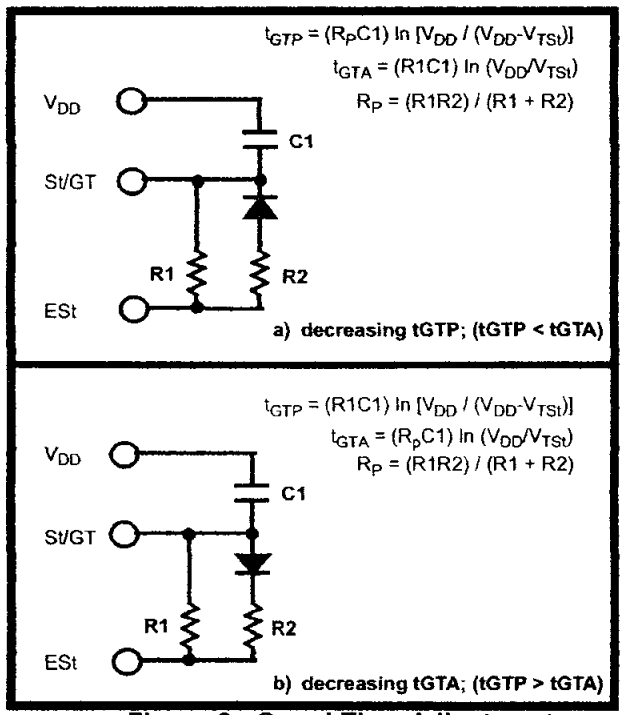


Figure 6 - Guard Time Adjustment

applications, leaving R1 to be selected by the designer. Different steering arrangements may be used to select independent tone present (t_{GTP}) and tone absent (t_{GTA}) guard times. This may be necessary to meet system specifications which place both accept and reject limits on tone duration and interdigital pause. Guard time adjustment also allows the designer to tailor system parameters such as talk off and noise immunity.

Increasing t_{REC} improves talk-off performance since it reduces the probability that tones simulated by speech will maintain a valid signal condition long enough to be registered. Alternatively, a relatively short t_{REC} with a long t_{DO} would be appropriate for extremely noisy environments where fast acquisition time and immunity to tone drop-outs are required. Design information for guard time adjustment is shown in Figure 6. The receiver timing is shown in Figure 7 with a description of the events in Figure 9.

Call Progress Filter

A call progress mode, using the MT8888C, can be selected allowing the detection of various tones, which identify the progress of a telephone call on the network. The call progress tone input and DTMF input are common, however, call progress tones can only be detected when CP mode has been selected. DTMF signals cannot be detected if CP mode has been selected (see Table 7). Figure 8 indicates the useful detect bandwidth of the call progress filter. Frequencies presented to the input, which are within the 'accept' bandwidth limits of the filter, are hard-limited by a high gain comparator with the $\overline{IRQ}$/CP pin serving as the output. The squarewave output obtained from the schmitt trigger can be analyzed by a microprocessor or counter arrangement to determine the nature of the call progress tone being detected. Frequencies which are in the 'reject' area will not be detected and consequently the $\overline{IRQ}$/CP pin will remain low.

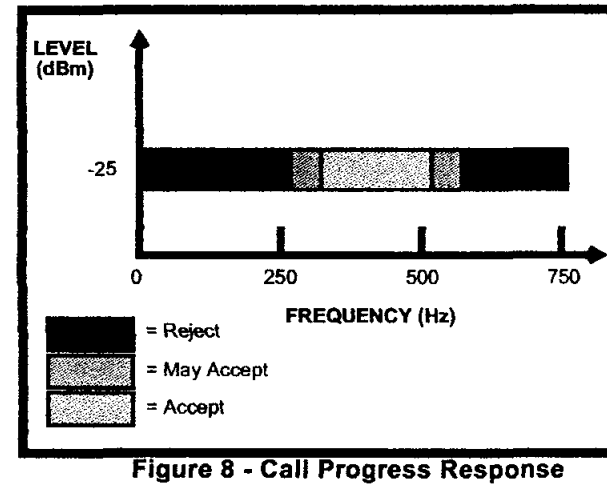


Figure 8 - Call Progress Response

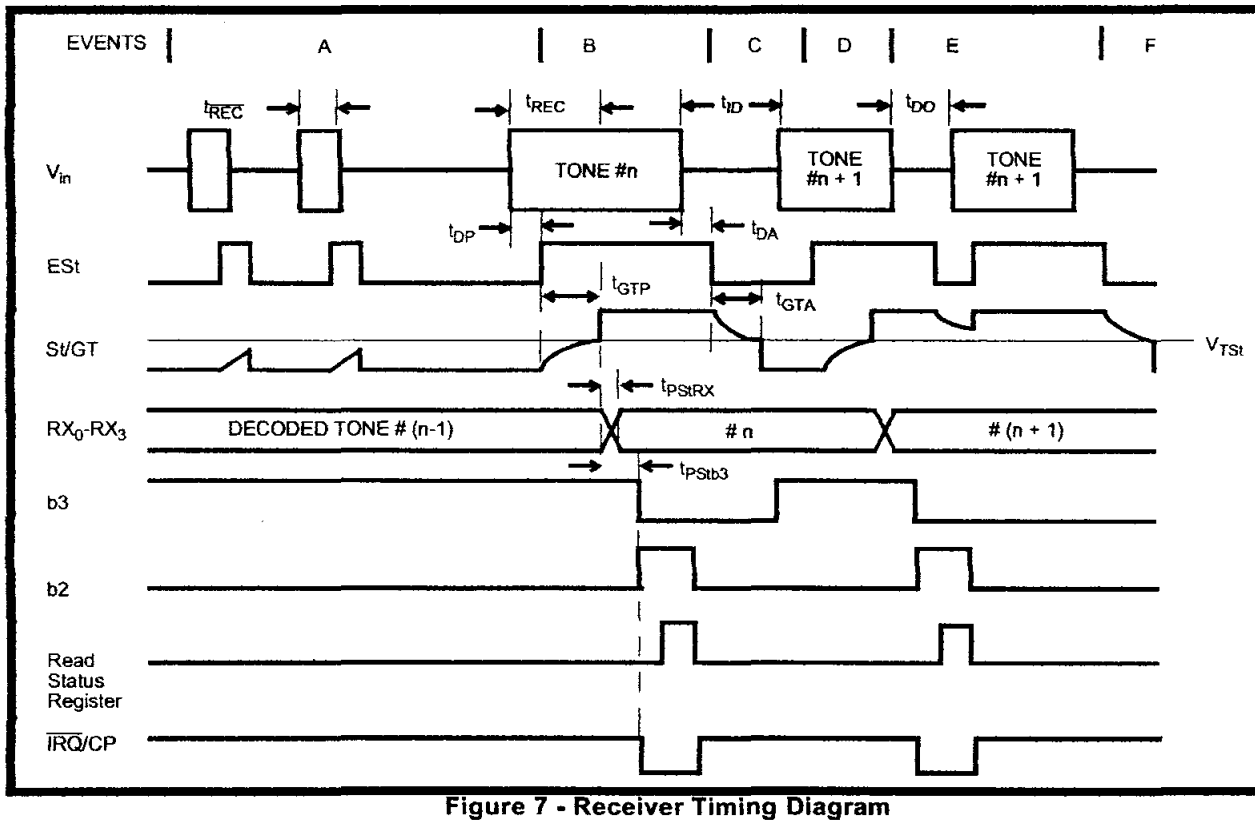


Figure 7 - Receiver Timing Diagram

EXPLANATION OF EVENTS

A) TONE BURSTS DETECTED, TONE DURATION INVALID, RX DATA REGISTER NOT UPDATED.
B) TONE #n DETECTED, TONE DURATION VALID, TONE DECODED AND LATCHED IN RX DATA REGISTER.
C) END OF TONE #n DETECTED, TONE ABSENT DURATION VALID, INFORMATION IN RX DATA REGISTER RETAINED UNTIL NEXT VALID TONE PAIR.
D) TONE #n+1 DETECTED, TONE DURATION VALID, TONE DECODED AND LATCHED IN RX DATA REGISTER.
E) ACCEPTABLE DROPOUT OF TONE #n+1, TONE ABSENT DURATION INVALID, DATA REMAINS UNCHANGED.
F) END OF TONE #n+1 DETECTED, TONE ABSENT DURATION VALID, INFORMATION IN RX DATA REGISTER RETAINED UNTIL NEXT VALID TONE PAIR.

EXPLANATION OF SYMBOLS

V_{in}	DTMF COMPOSITE INPUT SIGNAL.
ESt	EARLY STEERING OUTPUT. INDICATES DETECTION OF VALID TONE FREQUENCIES.
St/GT	STEERING INPUT/GUARD TIME OUTPUT. DRIVES EXTERNAL RC TIMING CIRCUIT.
RX_0-RX_3	4-BIT DECODED DATA IN RECEIVE DATA REGISTER
b3	DELAYED STEERING. INDICATES THAT VALID FREQUENCIES HAVE BEEN PRESENT/ABSENT FOR THE REQUIRED GUARD TIME THUS CONSTITUTING A VALID SIGNAL. ACTIVE LOW FOR THE DURATION OF A VALID DTMF SIGNAL.
b2	INDICATES THAT VALID DATA IS IN THE RECEIVE DATA REGISTER. THE BIT IS CLEARED AFTER THE STATUS REGISTER IS READ.
$\overline{IRQ}$/CP	INTERRUPT IS ACTIVE INDICATING THAT NEW DATA IS IN THE RX DATA REGISTER. THE INTERRUPT IS CLEARED AFTER THE STATUS REGISTER IS READ.
t_{REC}	MAXIMUM DTMF SIGNAL DURATION NOT DETECTED AS VALID.
$t_{\overline{REC}}$	MINIMUM DTMF SIGNAL DURATION REQUIRED FOR VALID RECOGNITION.
t_{ID}	MINIMUM TIME BETWEEN VALID SEQUENTIAL DTMF SIGNALS.
t_{DO}	MAXIMUM ALLOWABLE DROPOUT DURING VALID DTMF SIGNAL.
t_{DP}	TIME TO DETECT VALID FREQUENCIES PRESENT.
t_{DA}	TIME TO DETECT VALID FREQUENCIES ABSENT.
t_{GTP}	GUARD TIME, TONE PRESENT.
t_{GTA}	GUARD TIME, TONE ABSENT.

Figure 9 - Description of Timing Events

DTMF Generator

The DTMF transmitter employed in the MT8888C is capable of generating all sixteen standard DTMF tone pairs with low distortion and high accuracy. All frequencies are derived from an external 3.579545 MHz crystal. The sinusoidal waveforms for the individual tones are digitally synthesized using row and column programmable dividers and switched capacitor D/A converters. The row and column tones are mixed and filtered providing a DTMF signal with low total harmonic distortion and high accuracy. To specify a DTMF signal, data conforming to the encoding format shown in Table 1 must be written to the transmit Data Register. Note that this is the same as the receiver output code. The individual tones which are generated (f_{LOW} and f_{HIGH}) are referred to as Low Group and High Group tones. As seen from the table, the low group frequencies are 697, 770, 852 and 941 Hz. The high group frequencies are 1209, 1336, 1477 and 1633 Hz. Typically, the high group to low group amplitude ratio (twist) is 2 dB to com-pensate for high group attenuation on long loops.

The period of each tone consists of 32 equal time segments. The period of a tone is controlled by varying the length of these time segments. During write operations to the Transmit Data Register the 4 bit data on the bus is latched and converted to 2 of 8 coding for use by the programmable divider circuitry. This code is used to specify a time segment length, which will ultimately determine the frequency of the tone. When the divider reaches the appropriate count, as determined by the input code, a reset pulse is issued and the counter starts again. The number of time segments is fixed at 32, however, by varying the segment length as described above the frequency can also be varied. The divider output clocks another counter, which addresses the sinewave lookup ROM.

The lookup table contains codes which are used by the switched capacitor D/A converter to obtain discrete and highly accurate DC voltage levels. Two identical circuits are employed to produce row and column tones, which are then mixed using a low noise summing amplifier. The oscillator described needs no "start-up" time as in other DTMF generators since the crystal oscillator is running continuously thus providing a high degree of tone burst accuracy. A bandwidth limiting filter is incorporated and serves to attenuate distortion products above 8 kHz. It can be seen from Figure 8 that the distortion products are very low in amplitude.

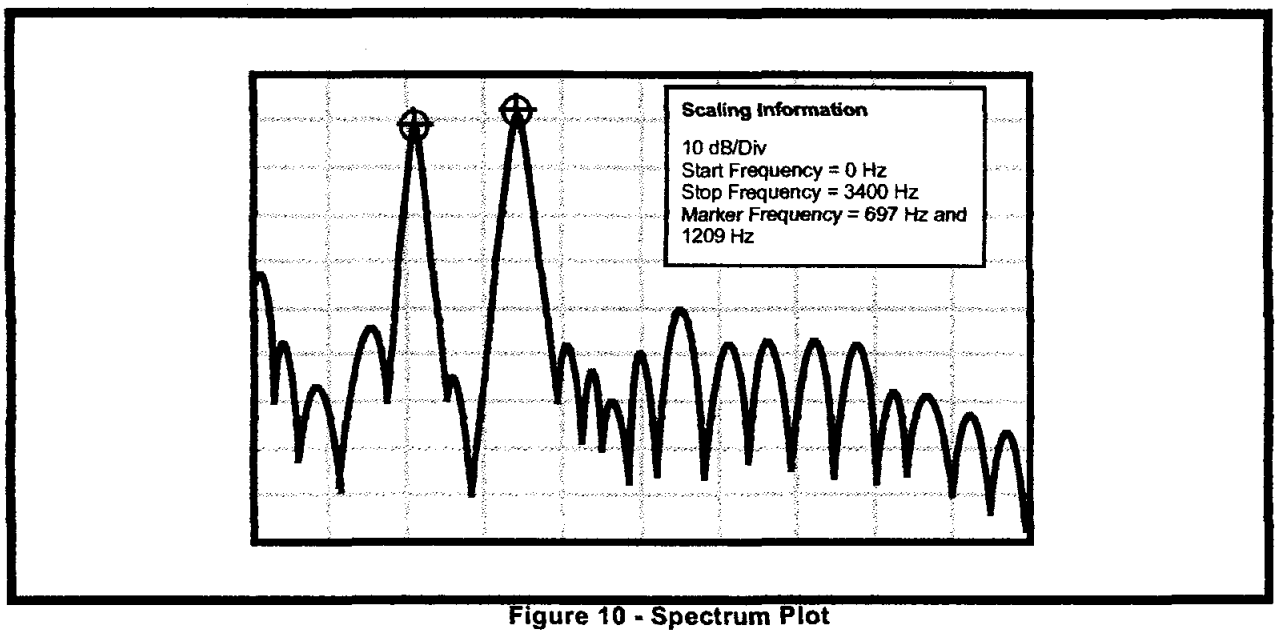


Figure 10 - Spectrum Plot

Burst Mode

In certain telephony applications it is required that DTMF signals being generated are of a specific duration determined either by the particular application or by any one of the exchange transmitter specifications currently existing. Standard DTMF signal timing can be accomplished by making use of the Burst Mode. The transmitter is capable of issuing symmetric bursts/pauses of predetermined duration. This burst/pause duration is 51 ms±1 ms, which is a standard interval for autodialer and central office applications. After the burst/pause has been issued, the appropriate bit is set in the Status Register indicating that the transmitter is ready for more data. The timing described above is available when DTMF mode has been selected. However, when CP mode (Call Progress mode) is selected, the burst/pause duration is doubled to 102 ms ±2 ms. Note that when CP mode and Burst mode have been selected, DTMF tones may be transmitted only and *not* received. In applications where a non-standard burst/pause time is desirable, a software timing loop or external timer can be used to provide the timing pulses when the burst mode is disabled by enabling and disabling the transmitter.

Single Tone Generation

A single tone mode is available whereby individual tones from the low group or high group can be generated. This mode can be used for DTMF test equipment applications, acknowledgment tone generation and distortion measurements. Refer to Control Register B description for details.

ACTIVE INPUT	OUTPUT FREQUENCY (Hz)		%ERROR
	SPECIFIED	ACTUAL	
L1	697	699.1	+0.30
L2	770	766.2	-0.49
L3	852	847.4	-0.54
L4	941	948.0	+0.74
H1	1209	1215.9	+0.57
H2	1336	1331.7	-0.32
H3	1477	1471.9	-0.35
H4	1633	1645.0	+0.73

Table 2. Actual Frequencies Versus Standard Requirements

Distortion Calculations

The MT8888C is capable of producing precise tone bursts with minimal error in frequency (see Table 2). The internal summing amplifier is followed by a first-order lowpass switched capacitor filter to minimize harmonic components and intermodulation products. The total harmonic distortion for a *single tone* can be calculated using Equation 1, which is the ratio of the total power of all the extraneous frequencies to the power of the fundamental frequency expressed as a percentage.

$$THD\ (\%) = 100 \frac{\left(\sqrt{V^2_{2f} + V^2_{3f} + V^2_{4f} + ... V^2_{nf}}\right)}{V_{fundamental}}$$

Equation 1. THD (%) For a Single Tone

The Fourier components of the tone output correspond to V_{2f}.... V_{nf} as measured on the output waveform. The total harmonic distortion for a *dual tone* can be calculated using Equation 2. V_L and V_H correspond to the low group amplitude and high group amplitude, respectively and V^2_{IMD} is the sum of all the intermodulation components. The internal switched-capacitor filter following the D/A converter keeps distortion products down to a very low level as shown in Figure 10.

$$THD\ (\%) = 100 \frac{\sqrt{V^2_{2L} + V^2_{3L} + ... V^2_{nL} + V^2_{2H} + V^2_{3H} + .. V^2_{nH} + V^2_{IMD}}}{\sqrt{V^2_L + V^2_H}}$$

Equation 2. THD (%) For a Dual Tone

DTMF Clock Circuit

The internal clock circuit is completed with the addition of a standard television colour burst crystal. The crystal specification is as follows:

Frequency:	3.579545 MHz
Frequency Tolerance:	±0.1%
Resonance Mode:	Parallel
Load Capacitance:	18pF
Maximum Series Resistance:	150 ohms
Maximum Drive Level:	2mW

e.g. CTS Knights MP036S
Toyocom TQC-203-A-9S

A number of MT8888C devices can be connected as shown in Figure 11 such that only one crystal is required. Alternatively, the OSC1 inputs on all devices can be driven from a TTL buffer with the OSC2 outputs left unconnected.

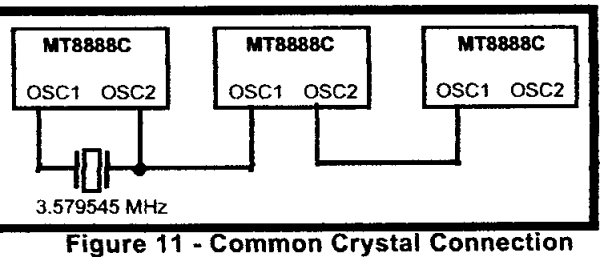


Figure 11 - Common Crystal Connection

Microprocessor Interface

The MT8888C incorporates an Intel microprocessor interface which is compatible with fast versions (16 MHz) of the 80C51. No wait cycles need to be inserted.

Figures 17 and 18 are the timing diagrams for the Intel 8031, 8051 and 8085 (5 MHz) microcontrollers. By NANDing the address latch enable (ALE) output with the high-byte address (P2) decode output, $\overline{CS}$ is generated. Figure 12 summarizes the connection of these Intel processors to the MT8888C transceiver.

The microprocessor interface provides access to five internal registers. The read-only Receive Data Register contains the decoded output of the last valid DTMF digit received. Data entered into the write-only Transmit Data Register will determine which tone pair is to be generated (see Table 1 for coding details). Transceiver control is accomplished with two control registers (see Tables 6 and 7), CRA and CRB, which have the same address. A write operation to CRB is executed by first setting the most significant bit (b3) in CRA. The following write operation to the same address will then be directed to CRB, and subsequent write cycles will be directed back to CRA. The read-only status register indicates the current transceiver state (see Table 8).

A software reset must be included at the beginning of all programs to initialize the control registers upon power-up or power reset (see Figure 17). Refer to Tables 4-7 for bit descriptions of the two control registers.

The multiplexed $\overline{IRQ}$/CP pin can be programmed to generate an interrupt upon validation of DTMF signals or when the transmitter is ready for more data (burst mode only). Alternatively, this pin can be configured to provide a squarewave output of the call progress signal. The $\overline{IRQ}$/CP pin is an open drain output and requires an external pull-up resistor (see Figure 13).

RS0	$\overline{WR}$	$\overline{RD}$	FUNCTION
0	0	1	Write to Transmit Data Register
0	1	0	Read from Receive Data Register
1	0	1	Write to Control Register
1	1	0	Read from Status Register

Table 3. Internal Register Functions

b3	b2	b1	b0
RSEL	IRQ	CP/DTMF	TOUT

Table 4. CRA Bit Positions

b3	b2	b1	b0
C/R	S/D	TEST	BURST $\overline{ENABLE}$

Table 5. CRB Bit Positions

BIT	NAME	DESCRIPTION
b0	TOUT	Tone Output Control. A logic high enables the tone output; a logic low turns the tone output off. This bit controls all transmit tone functions.
b1	CP/$\overline{\text{DTMF}}$	Call Progress or DTMF Mode Select. A logic high enables the receive call progress mode; a logic low enables DTMF mode. In DTMF mode the device is capable of receiving and transmitting DTMF signals. In CP mode a rectangular wave representation of the received tone signal will be present on the $\overline{\text{IRQ}}$/CP output pin if IRQ has been enabled (control register A, b2=1). In order to be detected, CP signals must be within the bandwidth specified in the AC Electrical Characteristics for Call Progress. Note: DTMF signals cannot be detected when CP mode is selected.
b2	IRQ	Interrupt Enable. A logic high enables the interrupt function; a logic low de-activates the interrupt function. When IRQ is enabled and DTMF mode is selected (control register A, b1=0), the $\overline{\text{IRQ}}$/CP output pin will go low when either 1) a valid DTMF signal has been received for a valid guard time duration, or 2) the transmitter is ready for more data (burst mode only).
b3	RSEL	Register Select. A logic high selects control register B for the next write cycle to the control register address. After writing to control register B, the following control register write cycle will be directed to control register A.

Table 6. Control Register A Description

BIT	NAME	DESCRIPTION
b0	$\overline{\text{BURST}}$	Burst Mode Select. A logic high de-activates burst mode; a logic low enables burst mode. When activated, the digital code representing a DTMF signal (see Table 1) can be written to the transmit register, which will result in a transmit DTMF tone burst and pause of equal durations (typically 51 msec.). Following the pause, the status register will be updated (b1 - Transmit Data Register Empty), and an interrupt will occur if the interrupt mode has been enabled. When CP mode (control register A, b1) is enabled the normal tone burst and pause durations are extended from a typical duration of 51 msec to 102 msec. When $\overline{\text{BURST}}$ is high (de-activated) the transmit tone burst duration is determined by the TOUT bit (control register A, b0).
b1	TEST	Test Mode Control. A logic high enables the test mode; a logic low de-activates the test mode. When TEST is enabled and DTMF mode is selected (control register A, b1=0), the signal present on the $\overline{\text{IRQ}}$/CP pin will be analogous to the state of the DELAYED STEERING bit of the status register (see Figure 7, signal b3).
b2	S/$\overline{\text{D}}$	Single or Dual Tone Generation. A logic high selects the single tone output; a logic low selects the dual tone (DTMF) output. The single tone generation function requires further selection of either the row or column tones (low or high group) through the C/$\overline{\text{R}}$ bit (control register B, b3).
b3	C/$\overline{\text{R}}$	Column or Row Tone Select. A logic high selects a column tone output; a logic low selects a row tone output. This function is used in conjunction with the S/$\overline{\text{D}}$ bit (control register B, b2).

Table 7. Control Register B Description

BIT	NAME	STATUS FLAG SET	STATUS FLAG CLEARED
b0	IRQ	Interrupt has occurred. Bit one (b1) or bit two (b2) is set.	Interrupt is inactive. Cleared after Status Register is read.
b1	TRANSMIT DATA REGISTER EMPTY (BURST MODE ONLY)	Pause duration has terminated and transmitter is ready for new data.	Cleared after Status Register is read or when in non-burst mode.
b2	RECEIVE DATA REGISTER FULL	Valid data is in the Receive Data Register.	Cleared after Status Register is read.
b3	$\overline{\text{DELAYED STEERING}}$	Set upon the valid detection of the absence of a DTMF signal.	Cleared upon the detection of a valid DTMF signal.

Table 8. Status Register Description

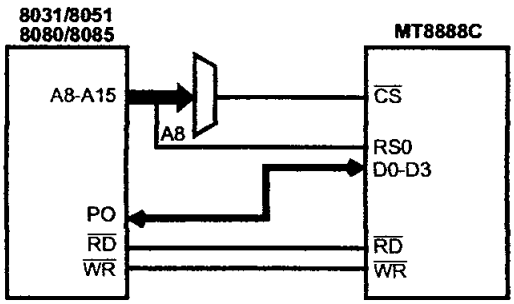
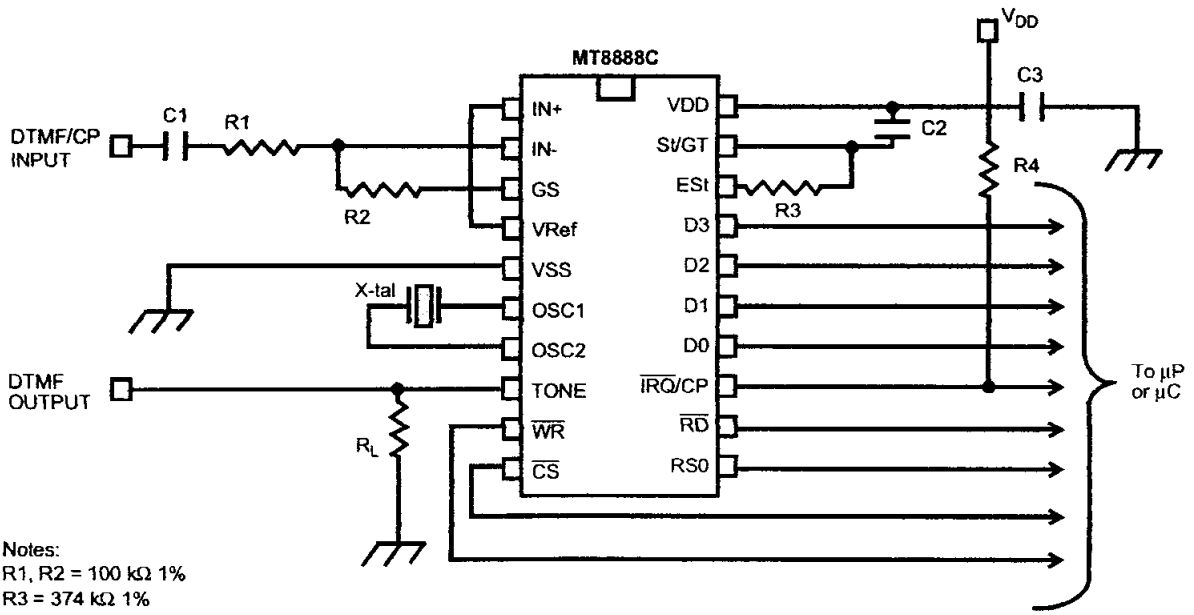


Figure 12 - MT8888C Interface Connections for Various Intel Micros



Notes:
R1, R2 = 100 kΩ 1%
R3 = 374 kΩ 1%
R4 = 3.3 kΩ 10%
R_L = 10 k Ω (min.)
C1 = 100 nF 5%
C2 = 100 nF 5%
C3 = 100 nF 10%*
X-tal = 3.579545 MHz

* Microprocessor based systems can inject undesirable noise into the supply rails. The performance of the MT8888C can be optimized by keeping noise on the supply rails to a minimum. The decoupling capacitor (C3) should be connected close to the device and ground loops should be avoided.

Figure 13 - Application Circuit (Single-Ended Input)

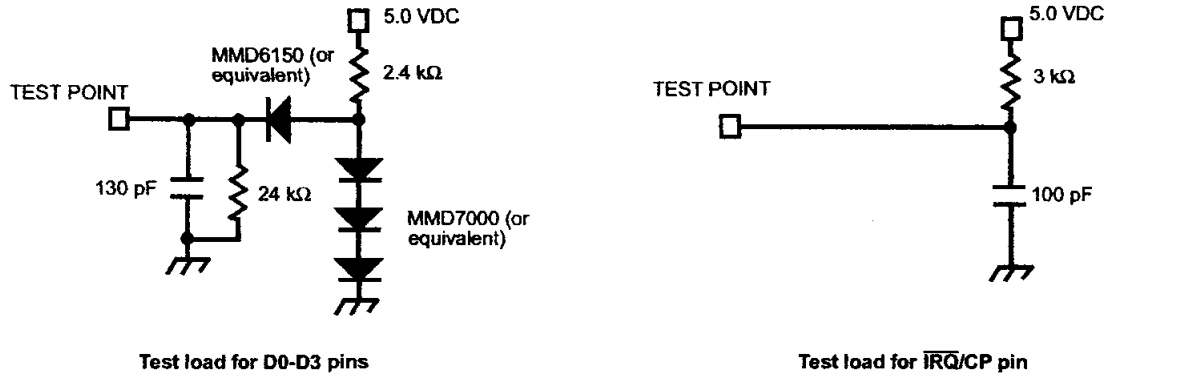


Figure 14 - Test Circuits

INITIALIZATION PROCEDURE

A software reset must be included at the beginning of all programs to initialize the control registers after power up.The initialization procedure should be implemented 100ms after power up.

Description:	Control			Data			
	RS0	**$\overline{WR}$**	**$\overline{RD}$**	**b3**	**b2**	**b1**	**b0**
1) Read Status Register	1	1	0	X	X	X	X
2) Write to Control Register	1	0	1	0	0	0	0
3) Write to Control Register	1	0	1	0	0	0	0
4) Write to Control Register	1	0	1	1	0	0	0
5) Write to Control Register	1	0	1	0	0	0	0
6) Read Status Register	1	1	0	X	X	X	X

TYPICAL CONTROL SEQUENCE FOR BURST MODE APPLICATIONS

Transmit DTMF tones of 50 ms burst/50 ms pause and Receive DTMF Tones.

Sequence:

	RS0	**$\overline{WR}$**	**$\overline{RD}$**	**b3**	**b2**	**b1**	**b0**
1) Write to Control Register A (tone out, DTMF, $\overline{IRQ}$, Select Control Register B)	1	0	1	1	1	0	1
2) Write to Control Register B (burst mode)	1	0	1	0	0	0	0
3) Write to Transmit Data Register (send a digit 7)	0	0	1	0	1	1	1
4) Wait for an interrupt or poll Status Register							
5) Read the Status Register	1	1	0	X	X	X	X
-if bit 1 is set, the Tx is ready for the next tone, in which case...							
Write to Transmit Register (send a digit 5)	0	0	1	0	1	0	1
-if bit 2 is set, a DTMF tone has been received, in which case....							
Read the Receive Data Register	0	1	0	X	X	X	X
-if both bits are set...							
Read the Receive Data Register	0	1	0	X	X	X	X
Write to Transmit Data Register	0	0	1	0	1	0	1

NOTE: IN THE TX BURST MODE, STATUS REGISTER BIT 1 WILL NOT BE SET UNTIL 100 ms (±2 ms) AFTER THE DATA IS WRITTEN TO THE TX DATA REGISTER. IN EXTENDED BURST MODE THIS TIME WILL BE DOUBLED TO 200 ms (± 4 ms).

Figure 15 - Application Notes

Absolute Maximum Ratings*

	Parameter	Symbol	Min	Max	Units
1	Power supply voltage V_{DD}-V_{SS}	V_{DD}		6	V
2	Voltage on any pin	V_I	V_{SS}-0.3	V_{DD}+0.3	V
3	Current at any pin (Except V_{DD} and V_{SS})			10	mA
4	Storage temperature	T_{ST}	-65	+150	°C
5	Package power dissipation	P_D		1000	mW

Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Parameter	Sym	Min	Typ‡	Max	Units	Test Conditions
1	Positive power supply	V_{DD}	4.75	5.00	5.25	V	
2	Operating temperature	T_O	-40		+85	°C	
3	Crystal clock frequency	f_{CLK}	3.575965	3.579545	3.583124	MHz	

Typical figures are at 25 °C and for design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics† - V_{SS}=0 V.

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	SUP	Operating supply voltage	V_{DD}	4.75	5.0	5.25	V	
2		Operating supply current	I_{DD}		7.0	11	mA	
3		Power consumption	P_C			57.8	mW	
4	INPUTS	High level input voltage (OSC1)	V_{IHO}	3.5			V	Note 9*
5		Low level input voltage (OSC1)	V_{ILO}			1.5	V	Note 9*
6		Steering threshold voltage	V_{TSt}	2.2	2.3	2.5	V	V_{DD}=5V
7	OUTPUTS	Low level output voltage (OSC2)	V_{OLO}			0.1	V	No load Note 9*
8		High level output voltage (OSC2)	V_{OHO}	4.9			V	No load Note 9*
9		Output leakage current (IRQ)	I_{OZ}		1	10	µA	V_{OH}=2.4 V
10		V_{Ref} output voltage	V_{Ref}	2.4	2.5	2.6	V	No load, V_{DD}=5V
11		V_{Ref} output resistance	R_{OR}		1.3		kΩ	
12	Digital	Low level input voltage	V_{IL}			0.8	V	
13		High level input voltage	V_{IH}	2.0			V	
14		Input leakage current	I_{IZ}			10	µA	V_{IN}=V_{SS} to V_{DD}
15	Data Bus	Source current	I_{OH}	-1.4	-6.6		mA	V_{OH}=2.4V
16		Sink current	I_{OL}	2.0	4.0		mA	V_{OL}=0.4V
17	ESt and StGt	Source current	I_{OH}	-0.5	-3.0		mA	V_{OH}=4.6V
18		Sink current	I_{OL}	2	4		mA	V_{OL}=0.4V
19	$\overline{IRQ}$/CP	Sink current	I_{OL}	4	16		mA	V_{OL}=0.4V

Characteristics are over recommended operating conditions unless otherwise stated.
Typical figures are at 25 °C, V_{DD} =5V and for design aid only: not guaranteed and not subject to production testing.
See "Notes" following AC Electrical Characteristics Tables.

Electrical Characteristics

Gain Setting Amplifier - Voltages are with respect to ground (V_{SS}) unless otherwise stated, V_{SS}= 0V.

	Characteristics	Sym	Min	Typ	Max	Units	Test Conditions
1	Input leakage current	I_{IN}			100	nA	$V_{SS} \le V_{IN} \le V_{DD}$
2	Input resistance	R_{IN}	10			MΩ	
3	Input offset voltage	V_{OS}			25	mV	
4	Power supply rejection	PSRR	50			dB	1 kHz
5	Common mode rejection	CMRR	40			dB	
6	DC open loop voltage gain	A_{VOL}	40			dB	C_L = 20p
7	Unity gain bandwidth	BW	1.0			MHz	C_L = 20p
8	Output voltage swing	V_O	0.5		V_{DD}-0.5	V	$R_L \ge 100$ kΩ to V_{SS}
9	Allowable capacitive load (GS)	C_L			100	pF	PM>40°
10	Allowable resistive load (GS)	R_L	50			kΩ	V_O = 4Vpp
11	Common mode range	V_{CM}	1.0		V_{DD}-1.0	V	R_L = 50kΩ

Figures are for design aid only: not guaranteed and not subject to production testing.
Characteristics are over recommended operating conditions unless otherwise stated.

MT8888C AC Electrical Characteristics† - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

		Characteristics	Sym	Min	Typ‡	Max	Units	Notes*
1	R X	Valid input signal levels (each tone of composite signal)		-29		+1	dBm	1,2,3,5,6
				27.5		869	mV_{RMS}	1,2,3,5,6

† Characteristics are over recommended operating conditions (unless otherwise stated) using the test circuit shown in Figure 13.

AC Electrical Characteristics† - Voltages are with respect to ground (V_{SS}) unless otherwise stated. f_C=3.579545 MHz

		Characteristics	Sym	Min	Typ‡	Max	Units	Notes*
1	R X	Positive twist accept				8	dB	2,3,6,9
2		Negative twist accept				8	dB	2,3,6,9
3		Freq. deviation accept		±1.5%± 2Hz				2,3,5
4		Freq. deviation reject		±3.5%				2,3,5
5		Third tone tolerance			-16		dB	2,3,4,5,9,10
6		Noise tolerance			-12		dB	2,3,4,5,7,9,10
7		Dial tone tolerance			22		dB	2,3,4,5,8,9

† Characteristics are over recommended operating conditions unless otherwise stated.
‡ Typical figures are at 25°C, V_{DD} = 5V, and for design aid only: not guaranteed and not subject to production testing.
* *See "Notes" following AC Electrical Characteristics Tables.

ectrical Characteristics† - Call Progress - Voltages are with respect to ground (V_{SS}), unless otherwise stated.

Characteristics	Sym	Min	Typ‡	Max	Units	Conditions
ccept Bandwidth	f_A	310		500	Hz	@ -25 dBm, Note 9
ower freq. (REJECT)	f_{LR}		290		Hz	@ -25 dBm
pper freq. (REJECT)	f_{HR}		540		Hz	@ -25 dBm
all progress tone detect level (total ower)		-30			dBm	

teristics are over recommended operating conditions unless otherwise stated
figures are at 25°C, V_{DD}=5V, and for design aid only: not guaranteed and not subject to production testing

ectrical Characteristics† - DTMF Reception - Typical DTMF tone accept and reject requirements. Actual e user selectable as per Figures 5, 6 and 7.

Characteristics	Sym	Min	Typ‡	Max	Units	Conditions
Minimum tone accept duration	t_{REC}		40		ms	
Maximum tone reject duration	$t_{\overline{REC}}$		20		ms	
Minimum interdigit pause duration	t_{ID}		40		ms	
Maximum tone drop-out duration	t_{OD}		20		ms	

teristics are over recommended operating conditions unless otherwise stated
figures are at 25°C, V_{DD}=5V, and for design aid only: not guaranteed and not subject to production testing

ectrical Characteristics† - Voltages are with respect to ground (V_{SS}), unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Conditions
T O N E I N	Tone present detect time	t_{DP}	3	11	14	ms	Note 11
	Tone absent detect time	t_{DA}	0.5	4	8.5	ms	Note 11
	Delay St to b3	t_{PStb3}		13		µs	See Figure 7
	Delay St to RX_0-RX_3	t_{PStRX}		8		µs	See Figure 7
T O N E O U T	Tone burst duration	t_{BST}	50		52	ms	DTMF mode
	Tone pause duration	t_{PS}	50		52	ms	DTMF mode
	Tone burst duration (extended)	t_{BSTE}	100		104	ms	Call Progress mode
	Tone pause duration (extended)	t_{PSE}	100		104	ms	Call Progress mode
	High group output level	V_{HOUT}	-6.1		-2.1	dBm	R_L=10kΩ
	Low group output level	V_{LOUT}	-8.1		-4.1	dBm	R_L=10kΩ
	Pre-emphasis	dB_P	0	2	3	dB	R_L=10kΩ
	Output distortion (Single Tone)	THD		-35		dB	25 kHz Bandwidth R_L=10kΩ
	Frequency deviation	f_D		±0.7	±1.5	%	f_C=3.579545 MHz
	Output load resistance	R_{LT}	10		50	kΩ	
X T A L	Crystal/clock frequency	f_C	3.5759	3.5795	3.5831	MHz	
	Clock input rise and fall time	t_{CLRF}			110	ns	Ext. clock
	Clock input duty cycle	DC_{CL}	40	50	60	%	Ext. clock
	Capacitive load (OSC2)	C_{LO}			30	pF	

is over recommended temperature & power supply voltages.
figures are at 25°C and for design aid only: not guaranteed and not subject to production testing.

AC Electrical Characteristics† - MPU Interface - Voltages are with respect to ground (V_{SS}), unless otherwise stated.

	Characteristics	Sym	Min	Typ‡	Max	Units	Conditions
1	$\overline{RD}/\overline{WR}$ clock frequency	f_{CYC}		4.0		MHz	Figure 16
2	$\overline{RD}/\overline{WR}$ cycle period	t_{CYC}		250		ns	Figure 16
3	$\overline{RD}/\overline{WR}$ rise and fall time	t_R, t_F			20	ns	Figure 16
4	Address setup time	t_{AS}	23			ns	Figures 17 & 18
5	Address hold time	t_{AH}	26			ns	Figures 17 & 18
6	Data hold time (read)	t_{DHR}	22			ns	Figures 17 & 18
7	$\overline{RD}$ to valid data delay (read)	t_{DDR}			100	ns	Figures 17 & 18
8	$\overline{RD}$, $\overline{WR}$ pulse width low	t_{PWL}	150			ns	Figures 16, 17 & 18
9	$\overline{RD}$, $\overline{WR}$ pulse width high	t_{PWH}		100		ns	Figures 16, 17 & 18
10	Data setup time (write)	t_{DSW}	45			ns	Figures 17 & 18
11	Data hold time (write)	t_{DHW}	10			ns	Figures 17 & 18
12	Input Capacitance (data bus)	C_{IN}		5		pF	
13	Output Capacitance ($\overline{IRQ}$/CP)	C_{OUT}		5		pF	

Characteristics are over recommended operating conditions unless otherwise stated
Typical figures are at 25°C, V_{DD}=5V, and for design aid only: not guaranteed and not subject to production testing

NOTES:
1) dBm=decibels above or below a reference power of 1 mW into a 600 ohm load.
2) Digit sequence consists of all 16 DTMF tones.
3) *Tone duration=40 ms. Tone pause=40 ms.*
4) Nominal DTMF frequencies are used.
5) Both tones in the composite signal have an equal amplitude.
6) The tone pair is deviated by ± 1.5%±2 Hz.
7) Bandwidth limited (3 kHz) Gaussian noise.
8) The precise dial tone frequencies are 350 and 440 Hz (±2%).
9) Guaranteed by design and characterization. Not subject to production testing.
10) Referenced to the lowest amplitude tone in the DTMF signal.
11) For guard time calculation purposes.

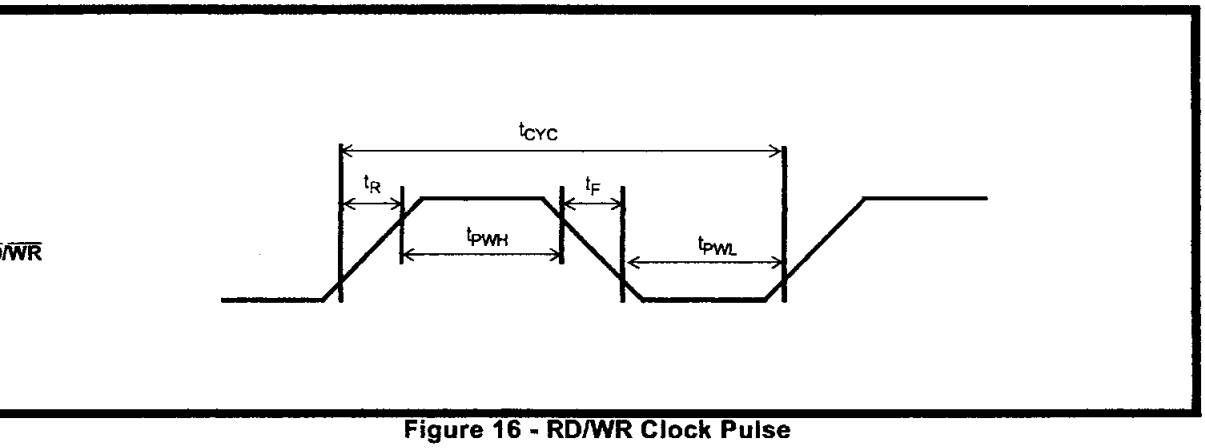


Figure 16 - RD/WR Clock Pulse

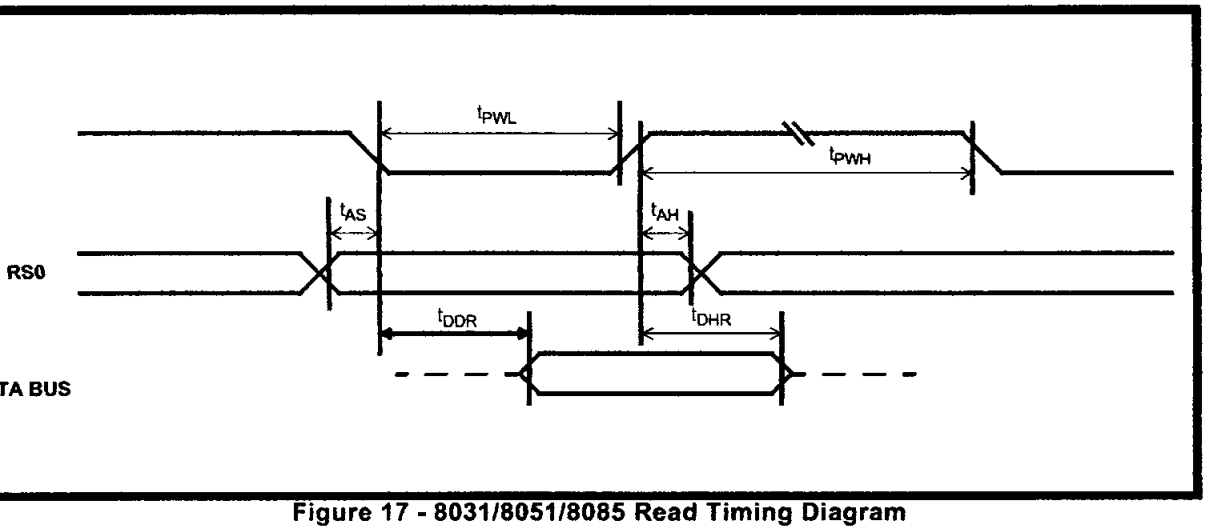


Figure 17 - 8031/8051/8085 Read Timing Diagram

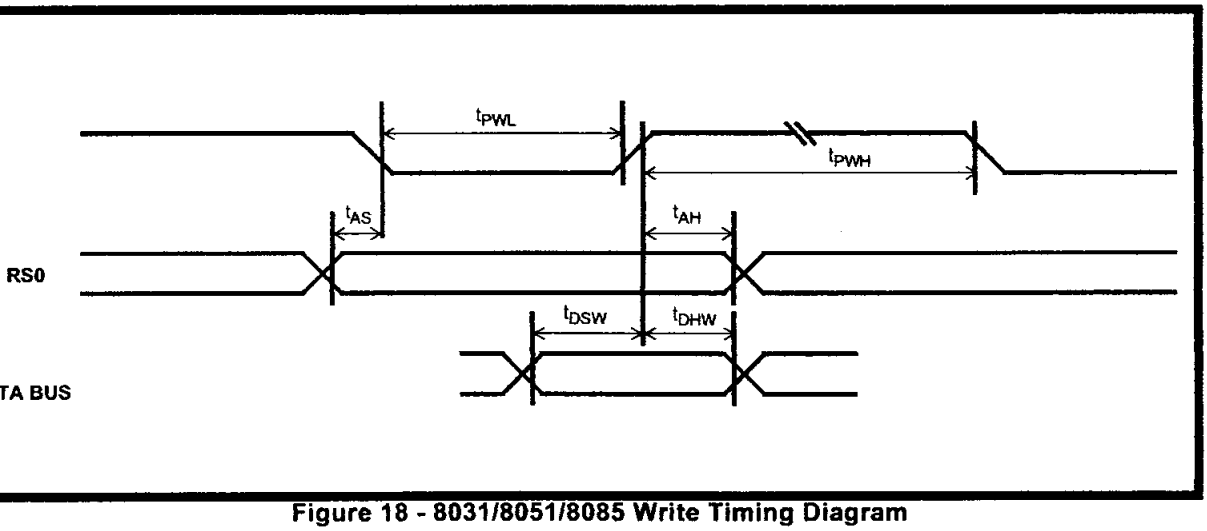


Figure 18 - 8031/8051/8085 Write Timing Diagram

ISO²-CMOS MT8870D/MT8870D-1
Integrated DTMF Receiver

ISSUE 5 March 1997

Features
- Complete DTMF Receiver
- Low power consumption
- Internal gain setting amplifier
- Adjustable guard time
- Central office quality
- Power-down mode
- Inhibit mode
- Backward compatible with MT8870C/MT8870C-1

Applications
- Receiver system for British Telecom (BT) or CEPT Spec (MT8870D-1)
- Paging systems
- Repeater systems/mobile radio
- Credit card systems
- Remote control
- Personal computers
- Telephone answering machine

Ordering Information

MT8870DE/DE-1	18 Pin Plastic DIP
MT8870DS/DS-1	18 Pin SOIC
MT8870DN/DN-1	20 Pin SSOP

-40 °C to +85 °C

Description

The MT8870D/MT8870D-1 is a complete DTMF receiver integrating both the bandsplit filter and digital decoder functions. The filter section uses switched capacitor techniques for high and low group filters; the decoder uses digital counting techniques to detect and decode all 16 DTMF tone-pairs into a 4-bit code. External component count is minimized by on chip provision of a differential input amplifier, clock oscillator and latched three-state bus interface.

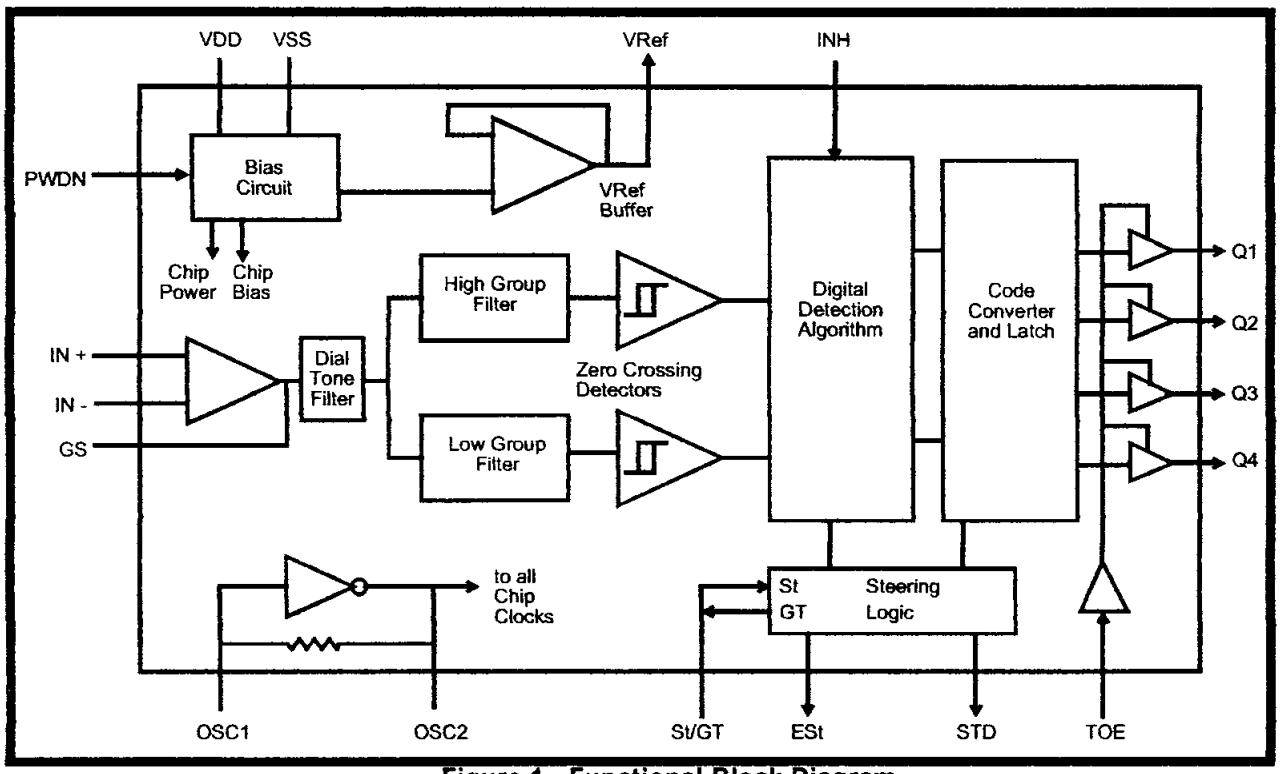


Figure 1 - Functional Block Diagram

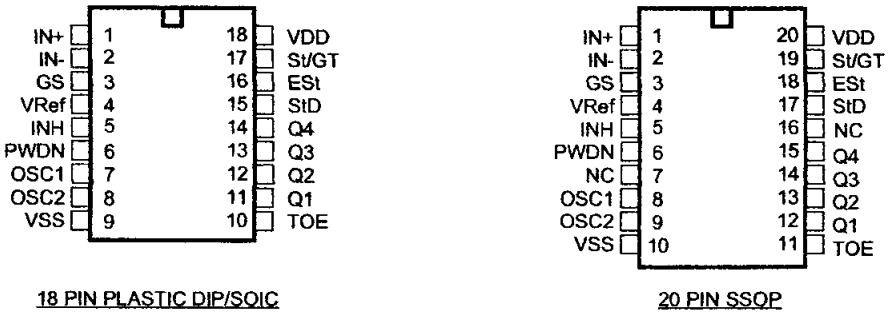


Figure 2 - Pin Connections

scription

Name	Description
IN+	**Non-Inverting Op-Amp (Input).**
IN-	**Inverting Op-Amp (Input).**
GS	**Gain Select.** Gives access to output of front end differential amplifier for connection of feedback resistor.
V_{Ref}	**Reference Voltage (Output).** Nominally $V_{DD}/2$ is used to bias inputs at mid-rail (see Fig. 6 and Fig. 10).
INH	***Inhibit (Input).*** *Logic high inhibits the detection of tones representing characters A, B, C* and D. This pin input is internally pulled down.
PWDN	**Power Down (Input).** Active high. Powers down the device and inhibits the oscillator. This pin input is internally pulled down.
OSC1	**Clock (Input).**
OSC2	**Clock (Output).** A 3.579545 MHz crystal connected between pins OSC1 and OSC2 completes the internal oscillator circuit.
V_{SS}	**Ground (Input).** 0V typical.
TOE	**Three State Output Enable (Input).** Logic high enables the outputs Q1-Q4. This pin is pulled up internally.
Q1-Q4	**Three State Data (Output).** When enabled by TOE, provide the code corresponding to the last valid tone-pair received (see Table 1). When TOE is logic low, the data outputs are high impedance.
StD	**Delayed Steering (Output).**Presents a logic high when a received tone-pair has been registered and the output latch updated; returns to logic low when the voltage on St/GT falls below V_{TSt}.
ESt	**Early Steering (Output).** Presents a logic high once the digital algorithm has detected a valid tone pair (signal condition). Any momentary loss of signal condition will cause ESt to return to a logic low.
St/GT	**Steering Input/Guard time (Output) Bidirectional.** A voltage greater than V_{TSt} detected at St causes the device to register the detected tone pair and update the output latch. A voltage less than V_{TSt} frees the device to accept a new tone pair. The GT output acts to reset the external steering time-constant; its state is a function of ESt and the voltage on St.
V_{DD}	**Positive power supply (Input).** +5V typical.
NC	No Connection.

Functional Description

The MT8870D/MT8870D-1 monolithic DTMF receiver offers small size, low power consumption and high performance. Its architecture consists of a bandsplit filter section, which separates the high and low group tones, followed by a digital counting section which verifies the frequency and duration of the received tones before passing the corresponding code to the output bus.

Filter Section

Separation of the low-group and high group tones is achieved by applying the DTMF signal to the inputs of two sixth-order switched capacitor bandpass filters, the bandwidths of which correspond to the low and high group frequencies. The filter section also incorporates notches at 350 and 440 Hz for exceptional dial tone rejection (see Figure 3). Each filter output is followed by a single order switched capacitor filter section which smooths the signals prior to limiting. Limiting is performed by high-gain comparators which are provided with hysteresis to prevent detection of unwanted low-level signals. The outputs of the comparators provide full rail logic swings at the frequencies of the incoming DTMF signals.

Decoder Section

Following the filter section is a decoder employing digital counting techniques to determine the frequencies of the incoming tones and to verify that they correspond to standard DTMF frequencies. A complex averaging algorithm protects against tone simulation by extraneous signals such as voice while

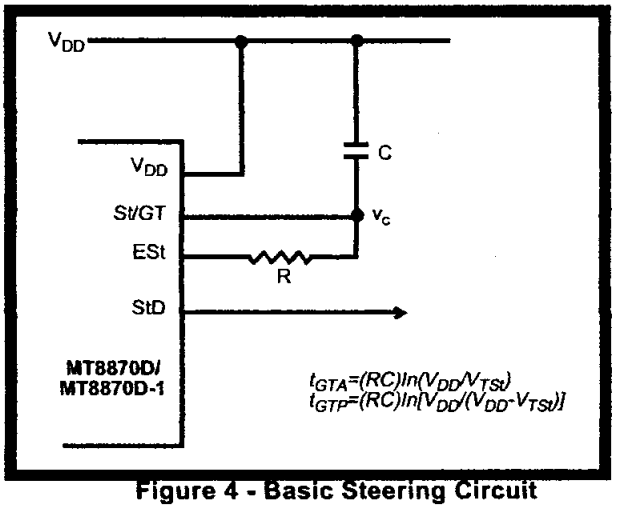


Figure 4 - Basic Steering Circuit

providing tolerance to small frequency deviations and variations. This averaging algorithm has been developed to ensure an optimum combination of immunity to talk-off and tolerance to the presence of interfering frequencies (third tones) and noise. When the detector recognizes the presence of two valid tones (this is referred to as the "signal condition" in some industry specifications) the "Early Steering" (ESt) output will go to an active state. Any subsequent loss of signal condition will cause ESt to assume an inactive state (see "Steering Circuit").

Steering Circuit

Before registration of a decoded tone pair, the receiver checks for a valid signal duration (referred to as character recognition condition). This check is performed by an external RC time constant driven by ESt. A logic high on ESt causes v_c (see Figure 4) to rise as the capacitor discharges. Provided signal

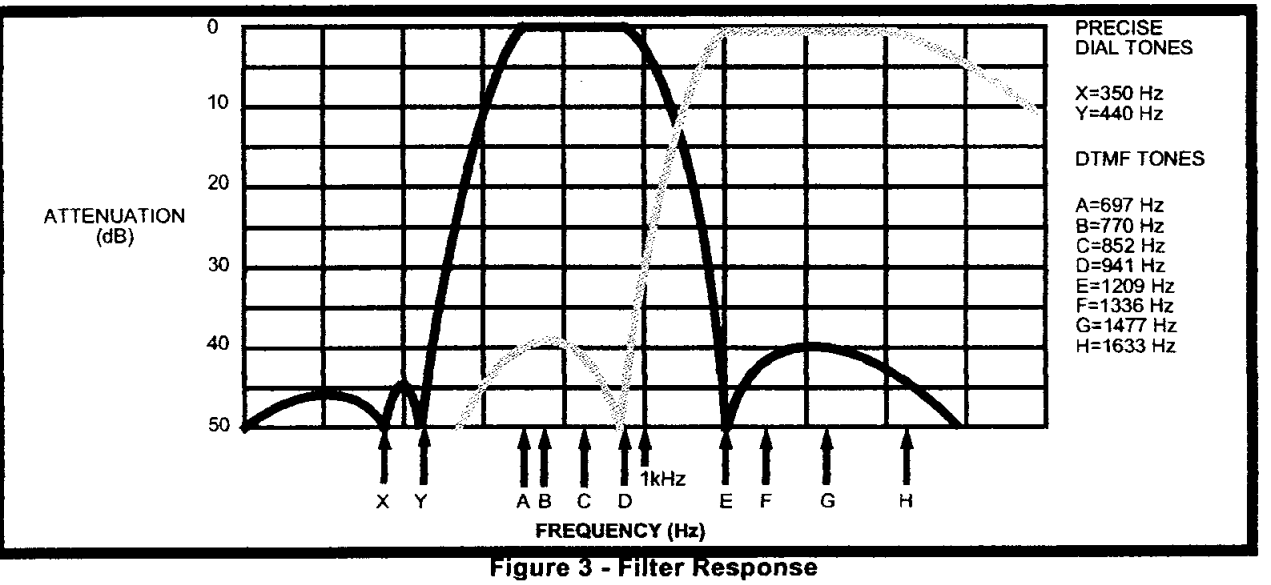


Figure 3 - Filter Response

n is maintained (ESt remains high) for the
n period (t_{GTP}), v_c reaches the threshold
f the steering logic to register the tone pair,
its corresponding 4-bit code (see Table 1)
output latch. At this point the GT output is
d and drives v_c to V_{DD}. GT continues to drive
long as ESt remains high. Finally, after a
elay to allow the output latch to settle, the
steering output flag (StD) goes high,
g that a received tone pair has been
ed. The contents of the output latch are
vailable on the 4-bit output bus by raising the
ate control input (TOE) to a logic high. The
circuit works in reverse to validate the
t pause between signals. Thus, as well as
signals too short to be considered valid, the
will tolerate signal interruptions (dropout)
t to be considered a valid pause. This facility,
with the capability of selecting the steering
nstants externally, allows the designer to
erformance to meet a wide variety of system
nents.

Time Adjustment

y situations not requiring selection of tone
and interdigital pause, the simple steering
hown in Figure 4 is applicable. Component
re chosen according to the formula:

$$t_{REC}=t_{DP}+t_{GTP}$$
$$t_{ID}=t_{DA}+t_{GTA}$$

ue of t_{DP} is a device parameter (see Figure
t_{REC} is the minimum signal duration to be
zed by the receiver. A value for C of 0.1 µF is

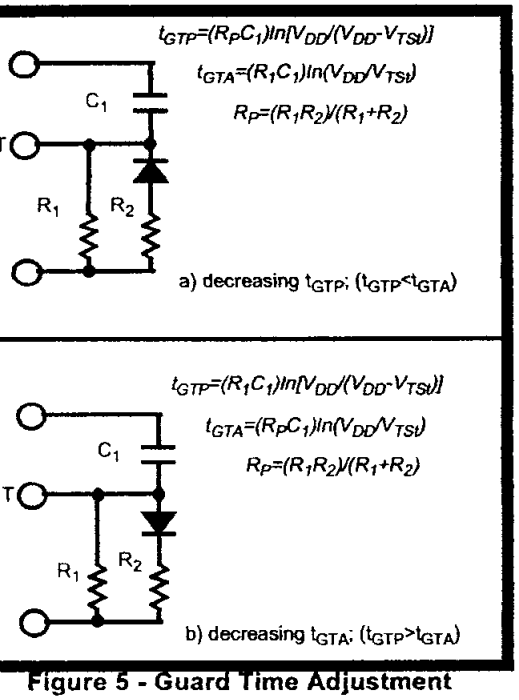


Figure 5 - Guard Time Adjustment

Digit	TOE	INH	ESt	Q_4	Q_3	Q_2	Q_1
ANY	L	X	H	Z	Z	Z	Z
1	H	X	H	0	0	0	1
2	H	X	H	0	0	1	0
3	H	X	H	0	0	1	1
4	H	X	H	0	1	0	0
5	H	X	H	0	1	0	1
6	H	X	H	0	1	1	0
7	H	X	H	0	1	1	1
8	H	X	H	1	0	0	0
9	H	X	H	1	0	0	1
0	H	X	H	1	0	1	0
*	H	X	H	1	0	1	1
#	H	X	H	1	1	0	0
A	H	L	H	1	1	0	1
B	H	L	H	1	1	1	0
C	H	L	H	1	1	1	1
D	H	L	H	0	0	0	0
A	H	H	L	undetected, the output code will remain the same as the previous detected code			
B	H	H	L				
C	H	H	L				
D	H	H	L				

Table 1. Functional Decode Table

L=LOGIC LOW, H=LOGIC HIGH, Z=HIGH IMPEDANCE
X = DON'T CARE

recommended for most applications, leaving R to be selected by the designer.

Different steering arrangements may be used to select independently the guard times for tone present (t_{GTP}) and tone absent (t_{GTA}). This may be necessary to meet system specifications which place both accept and reject limits on both tone duration and interdigital pause. Guard time adjustment also allows the designer to tailor system parameters such as talk off and noise immunity. Increasing t_{REC} improves talk-off performance since it reduces the probability that tones simulated by speech will maintain signal condition long enough to be registered. Alternatively, a relatively short t_{REC} with a long t_{DO} would be appropriate for extremely noisy environments where fast acquisition time and immunity to tone drop-outs are required. Design information for guard time adjustment is shown in Figure 5.

Power-down and Inhibit Mode

A logic high applied to pin 6 (PWDN) will power down the device to minimize the power consumption in a standby mode. It stops the oscillator and the functions of the filters.

Inhibit mode is enabled by a logic high input to the pin 5 (INH). It inhibits the detection of tones representing characters A, B, C, and D. The output code will remain the same as the previous detected code (see Table 1).

Differential Input Configuration

The input arrangement of the MT8870D/MT8870D-1 provides a differential-input operational amplifier as well as a bias source (V_{Ref}) which is used to bias the inputs at mid-rail. Provision is made for connection of a feedback resistor to the op-amp output (GS) for adjustment of gain. In a single-ended configuration, the input pins are connected as shown in Figure 10 with the op-amp connected for unity gain and V_{Ref} biasing the input at $^1/_2V_{DD}$. Figure 6 shows the differential configuration, which permits the adjustment of gain with the feedback resistor R_5.

Crystal Oscillator

The internal clock circuit is completed with the addition of an external 3.579545 MHz crystal and is normally connected as shown in Figure 10 (Single-Ended Input Configuration). However, it is possible to configure several MT8870D/MT8870D-1 devices employing only a single oscillator crystal. The oscillator output of the first device in the chain is coupled through a 30 pF capacitor to the oscillator input (OSC1) of the next device. Subsequent devices are connected in a similar fashion. Refer to Figure 7 for details. The problems associated with unbalanced loading are not a concern with the arrangement shown, i.e., precision balancing capacitors are not required.

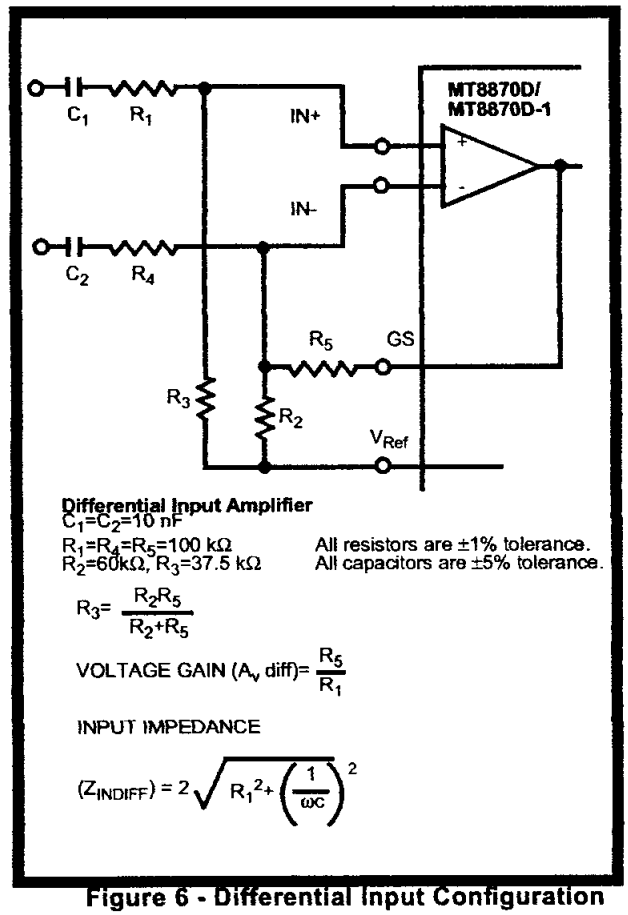


Figure 6 - Differential Input Configuration

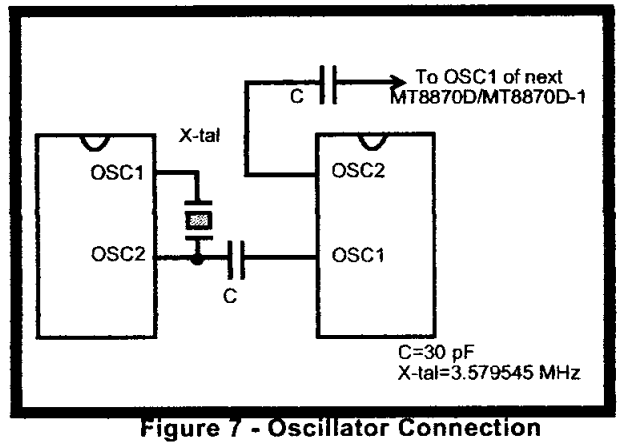


Figure 7 - Oscillator Connection

Parameter	Unit	Resonator
R1	Ohms	10.752
L1	mH	.432
C1	pF	4.984
C0	pF	37.915
Qm	-	896.37
Δf	%	±0.2%

Table 2. Recommended Resonator Specifications

Note: Qm=quality factor of RLC model, i.e., $1/2\Pi fR1C1$.

cations

VER SYSTEM FOR BRITISH TELECOM POR 1151

rcuit shown in Fig. 9 illustrates the use of 0D-1 device in a typical receiver system. BT efines the input signals less than -34 dBm as -operate level. This condition can be attained osing a suitable values of R_1 and R_2 to 3 dB attenuation, such that -34 dBm input will correspond to -37 dBm at the gain setting of MT8870D-1. As shown in the diagram, the nent values of R_3 and C_2 are the guard time ments when the total component tolerance is or better performance, it is recommended to non-symmetric guard time circuit in Fig. 8.

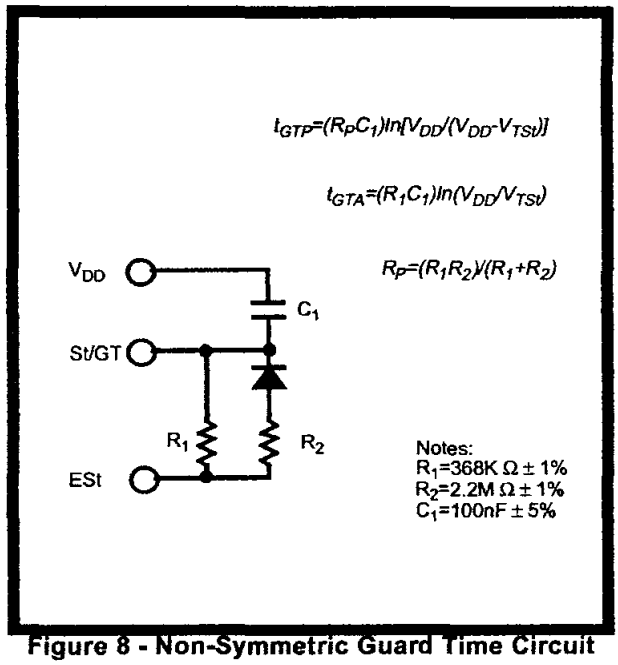
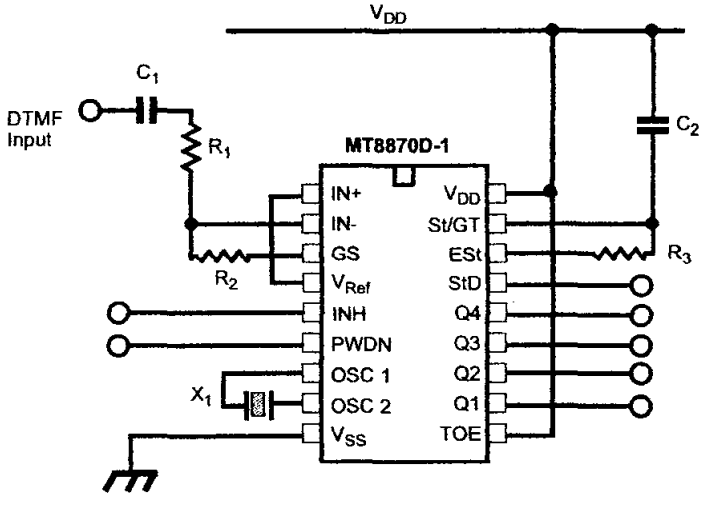


Figure 8 - Non-Symmetric Guard Time Circuit



NOTES:
R_1 = 102KΩ ± 1%
R_2 = 71.5KΩ ± 1%
R_3 = 390KΩ ±1 %
C_1,C_2 = 100 nF ± 5%
X_1 = 3.579545 MHz ± 0.1%
V_{DD} = 5.0V ± 5%

Figure 9 - Single-Ended Input Configuration for BT or CEPT Spec

Absolute Maximum Ratings†

	Parameter	Symbol	Min	Max	Units
1	DC Power Supply Voltage	V_{DD}		7	V
2	Voltage on any pin	V_I	V_{SS}-0.3	V_{DD}+0.3	V
3	Current at any pin (other than supply)	I_I		10	mA
4	Storage temperature	T_{STG}	-65	+150	°C
5	Package power dissipation	P_D		500	mW

Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.
erate above 75 °C at 16 mW / °C. All leads soldered to board.

Recommended Operating Conditions - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Parameter	Sym	Min	Typ‡	Max	Units	Test Conditions
1	DC Power Supply Voltage	V_{DD}	4.75	5.0	5.25	V	
2	Operating Temperature	T_O	-40		+85	°C	
3	Crystal/Clock Frequency	fc		3.579545		MHz	
4	Crystal/Clock Freq.Tolerance	Δfc		±0.1		%	

Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics - V_{DD}=5.0V± 5%, V_{SS}=0V, -40°C ≤ T_O ≤ +85°C, unless otherwise stated.

		Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
1	SUPPLY	Standby supply current	I_{DDQ}		10	25	µA	PWDN=V_{DD}
2		Operating supply current	I_{DD}		3.0	9.0	mA	
3		Power consumption	P_O		15		mW	fc=3.579545 MHz
4	INPUTS	High level input	V_{IH}	3.5			V	V_{DD}=5.0V
5		Low level input voltage	V_{IL}			1.5	V	V_{DD}=5.0V
6		Input leakage current	I_{IH}/I_{IL}		0.1		µA	V_{IN}=V_{SS} or V_{DD}
7		Pull up (source) current	I_{SO}		7.5	20	µA	TOE (pin 10)=0, V_{DD}=5.0V
8		Pull down (sink) current	I_{SI}		15	45	µA	INH=5.0V, PWDN=5.0V, V_{DD}=5.0V
9		Input impedance (IN+, IN-)	R_{IN}		10		MΩ	@ 1 kHz
10		Steering threshold voltage	V_{TSt}	2.2	2.4	2.5	V	V_{DD} = 5.0V
11	OUTPUTS	Low level output voltage	V_{OL}			V_{SS}+0.03	V	No load
12		High level output voltage	V_{OH}	V_{DD}-0.03			V	No load
13		Output low (sink) current	I_{OL}	1.0	2.5		mA	V_{OUT}=0.4 V
14		Output high (source) current	I_{OH}	0.4	0.8		mA	V_{OUT}=4.6 V
15		V_{Ref} output voltage	V_{Ref}	2.3	2.5	2.7	V	No load, V_{DD} = 5.0V
16		V_{Ref} output resistance	R_{OR}		1		kΩ	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

ıg Characteristics - V_{DD}=5.0V±5%, V_{SS}=0V, -40°C ≤ T_O ≤ +85°C ,unless otherwise stated.

ing Amplifier

Characteristics	Sym	Min	Typ‡	Max	Units	Test Conditions
ıt leakage current	I_{IN}			100	nA	$V_{SS} \le V_{IN} \le V_{DD}$
ıt resistance	R_{IN}	10			MΩ	
ıt offset voltage	V_{OS}			25	mV	
ver supply rejection	PSRR	50			dB	1 kHz
nmon mode rejection	CMRR	40			dB	0.75 V ≤ V_{IN} ≤ 4.25 V biased at V_{Ref} =2.5 V
open loop voltage gain	A_{VOL}	32			dB	
ty gain bandwidth	f_C	0.30			MHz	
tput voltage swing	V_O	4.0			V_{pp}	Load ≥ 100 kΩ to V_{SS} @ GS
ximum capacitive load (GS)	C_L			100	pF	
sistive load (GS)	R_L			50	kΩ	
mmon mode range	V_{CM}	2.5			V_{pp}	No Load

D AC Electrical Characteristics - V_{DD}=5.0V ±5%, V_{SS}=0V, -40°C ≤ T_O ≤ +85°C , using Test Circuit shown in Figure 10.

Characteristics	Sym	Min	Typ‡	Max	Units	Notes*
d input signal levels (each e of composite signal)		-29		+1	dBm	1,2,3,5,6,9
		27.5		869	mV_{RMS}	1,2,3,5,6,9
ıative twist accept				8	dB	2,3,6,9,12
itive twist accept				8	dB	2,3,6,9,12
quency deviation accept		±1.5% ± 2 Hz				2,3,5,9
quency deviation reject		±3.5%				2,3,5,9
d tone tolerance			-16		dB	2,3,4,5,9,10
se tolerance			-12		dB	2,3,4,5,7,9,10
tone tolerance			+22		dB	2,3,4,5,8,9,11

ures are at 25 °C and are for design aid only: not guaranteed and not subject to production testing.

ecibels above or below a reference power of 1 mW into a 600 ohm load.
quence consists of all DTMF tones.
ration= 40 ms, tone pause= 40 ms.
ondition consists of nominal DTMF frequencies.
es in composite signal have an equal amplitude.
ir is deviated by ±1.5 %± 2 Hz.
ith limited (3 kHz) Gaussian noise.
cise dial tone frequencies are (350 Hz and 440 Hz) ± 2 %.
rror rate of better than 1 in 10,000.
ced to lowest level frequency component in DTMF signal.
ced to the minimum valid accept level.
teed by design and characterization.

MT8870D-1 AC Electrical Characteristics - V_{DD}=5.0V±5%, V_{SS}=0V, -40°C ≤ T_O ≤ +85°C , using Test Circuit shown in Figure 10.

	Characteristics	Sym	Min	Typ‡	Max	Units	Notes*
1	Valid input signal levels (each tone of composite signal)		-31		+1	dBm	Tested at V_{DD}=5.0V 1,2,3,5,6,9
			21.8		869	mV_{RMS}	
2	Input Signal Level Reject		-37			dBm	Tested at V_{DD}=5.0V 1,2,3,5,6,9
			10.9			mV_{RMS}	
3	Negative twist accept				8	dB	2,3,6,9,13
4	Positive twist accept				8	dB	2,3,6,9,13
5	Frequency deviation accept		±1.5%± 2 Hz				2,3,5,9
6	Frequency deviation reject		±3.5%				2,3,5,9
7	Third zone tolerance			-18.5		dB	2,3,4,5,9,12
8	Noise tolerance			-12		dB	2,3,4,5,7,9,10
9	Dial tone tolerance			+22		dB	2,3,4,5,8,9,11

‡ Typical figures are at 25 °C and are for design aid only: not guaranteed and not subject to production testing.

*NOTES
1. dBm= decibels above or below a reference power of 1 mW into a 600 ohm load.
2. Digit sequence consists of all DTMF tones.
3. Tone duration= 40 ms, tone pause= 40 ms.
4. Signal condition consists of nominal DTMF frequencies.
5. Both tones in composite signal have an equal amplitude.
6. Tone pair is deviated by ±1.5 %± 2 Hz.
7. Bandwidth limited (3 kHz) Gaussian noise.
8. The precise dial tone frequencies are (350 Hz and 440 Hz) ± 2 %.
9. For an error rate of better than 1 in 10,000.
10. Referenced to lowest level frequency component in DTMF signal.
11. Referenced to the minimum valid accept level.
12. Referenced to Fig. 10 input DTMF tone level at -25dBm (-28dBm at GS Pin) interference frequency range between 480-3400Hz.
13. Guaranteed by design and characterization.

ectrical Characteristics - V_{DD}=5.0V±5%, V_{SS}=0V, -40°C ≤ To ≤ +85°C , using Test Circuit shown in Figure 10.

	Characteristics	Sym	Min	Typ‡	Max	Units	Conditions
TIMING	Tone present detect time	t_{DP}	5	11	14	ms	Note 1
	Tone absent detect time	t_{DA}	0.5	4	8.5	ms	Note 1
	Tone duration accept	t_{REC}			40	ms	Note 2
	Tone duration reject	$t_{\overline{REC}}$	20			ms	Note 2
	Interdigit pause accept	t_{ID}			40	ms	Note 2
	Interdigit pause reject	t_{DO}	20			ms	Note 2
OUTPUTS	Propagation delay (St to Q)	t_{PQ}		8	11	µs	TOE=V_{DD}
	Propagation delay (St to StD)	t_{PStD}		12	16	µs	TOE=V_{DD}
	Output data set up (Q to StD)	t_{QStD}		3.4		µs	TOE=V_{DD}
	Propagation delay (TOE to Q ENABLE)	t_{PTE}		50		ns	load of 10 kΩ, 50 pF
	Propagation delay (TOE to Q DISABLE)	t_{PTD}		300		ns	load of 10 kΩ, 50 pF
PDWN	Power-up time	t_{PU}		30		ms	Note 3
	Power-down time	t_{PD}		20		ms	
CLOCK	Crystal/clock frequency	f_C	3.5759	3.5795	3.5831	MHz	
	Clock input rise time	t_{LHCL}			110	ns	Ext. clock
	Clock input fall time	t_{HLCL}			110	ns	Ext. clock
	Clock input duty cycle	DC_{CL}	40	50	60	%	Ext. clock
	Capacitive load (OSC2)	C_{LO}			30	pF	

al figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

s:
Used for guard-time calculation purposes only.
These, user adjustable parameters, are not device specifications. The adjustable settings of these minimums and maximums are recommendations based upon network requirements.
With valid tone present at input, t_{PU} equals time from PDWN going low until ESt going high.

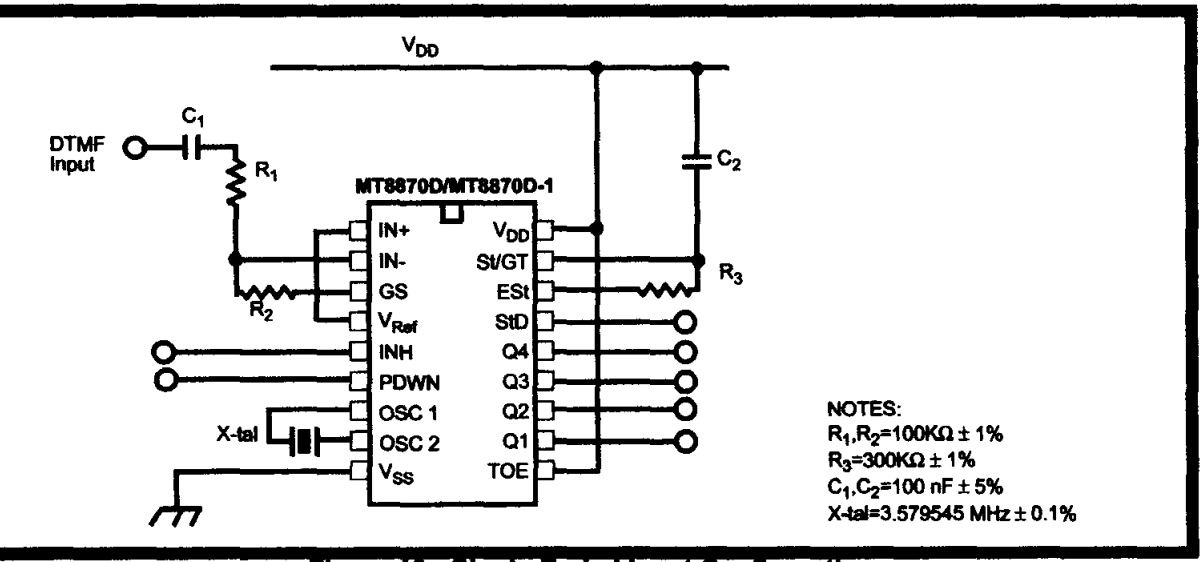
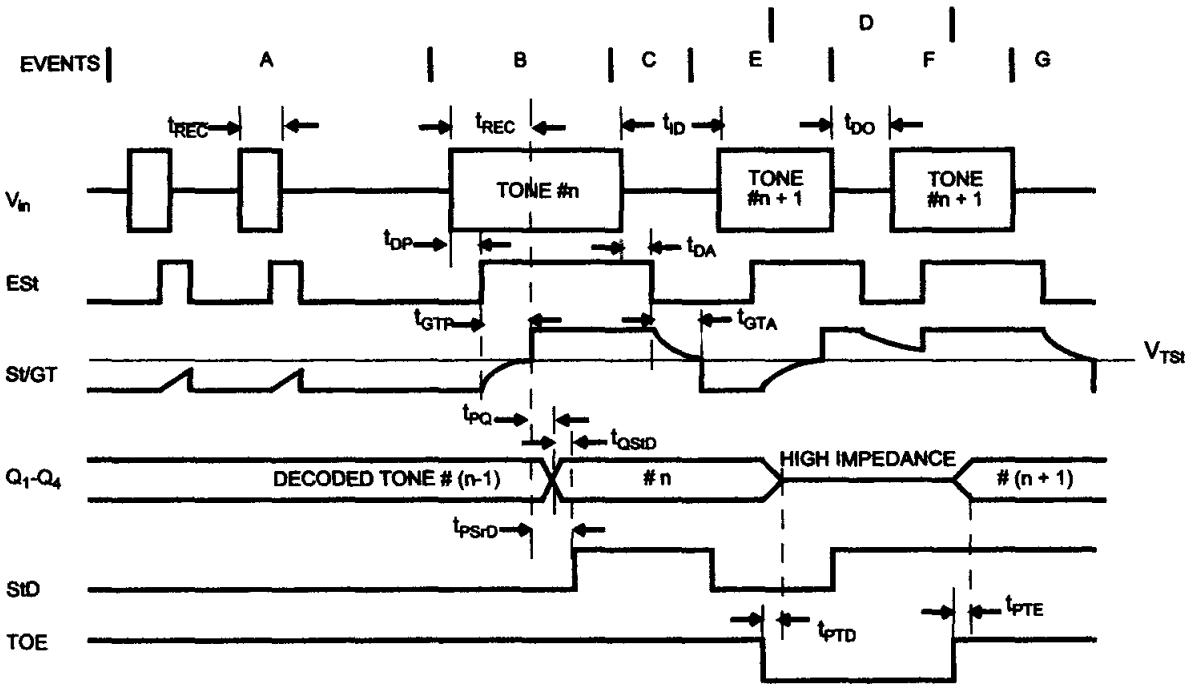


Figure 10 - Single-Ended Input Configuration



EXPLANATION OF EVENTS

A) TONE BURSTS DETECTED, TONE DURATION INVALID, OUTPUTS NOT UPDATED.

B) TONE #n DETECTED, TONE DURATION VALID, TONE DECODED AND LATCHED IN OUTPUTS

C) END OF TONE #n DETECTED, TONE ABSENT DURATION VALID, OUTPUTS REMIAN LATCHED UNTIL NEXT VALID TONE.

D) OUTPUTS SWITCHED TO HIGH IMPEDANCE STATE.

E) TONE #n + 1 DETECTED, TONE DURATION VALID, TONE DECODED AND LATCHED IN OUTPUTS (CURRENTLY HIGH IMPEDANCE).

F) ACCEPTABLE DROPOUT OF TONE #n + 1, TONE ABSENT DURATION INVALID, OUTPUTS REMAIN LATCHED.

G) END OF TONE #n + 1 DETECTED, TONE ABSENT DURATION VALID, OUTPUTS REMAIN LATCHED UNTIL NEXT VALID TONE.

EXPLANATION OF SYMBOLS

V_{in} DTMF COMPOSITE INPUT SIGNAL.

ESt EARLY STEERING OUTPUT. INDICATES DETECTION OF VALID TONE FREQUENCIES.

St/GT STEERING INPUT/GUARD TIME OUTPUT. DRIVES EXTERNAL RC TIMING CIRCUIT.

Q_1-Q_4 4-BIT DECODED TONE OUTPUT.

StD DELAYED STEERING OUTPUT. INDICATES THAT VALID FREQUENCIES HAVE BEEN PRESENT/ABSENT FOR THE REQUIRED GUARD TIME THUS CONSTITUTING A VALID SIGNAL.

TOE TONE OUTPUT ENABLE (INPUT). A LOW LEVEL SHIFTS Q_1-Q_4 TO ITS HIGH IMPEDANCE STATE.

t_{REC} MAXIMUM DTMF SIGNAL DURATION NOT DETECED AS VALID

t_{REC} MINIMUM DTMF SIGNAL DURATION REQUIRED FOR VALID RECOGNITION

t_{ID} MAXIMUM TIME BETWEEN VALID DTMF SIGNALS.

t_{DO} MAXIMUM ALLOWABLE DROP OUT DURING VALID DTMF SIGNAL.

t_{DP} TIME TO DETECT THE PRESENCE OF VALID DTMF SIGNALS.

t_{DA} TIME TO DETECT THE ABSENCE OF VALID DTMF SIGNALS.

t_{GTP} GUARD TIME, TONE PRESENT.

t_{GTA} GUARD TIME, TONE ABSENT.

Figure 11 - Timing Diagram

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