LAMPIRAN

GAMBAR RANGKAIAN LENGKAP

IC buffer 2 (A1)
IC buffer 2 (A2)
IC buffer 2 (A3)
IC buffer 2 (A4)
IC buffer 2 (A5)
IC buffer 2 (A6)
IC buffer 2 (A7)

Relay pH meter

pH meter

ICL7126CPL

MEDWIN S
5103001024

IC buffer 1 (A1)
IC buffer 1 (A2)
IC buffer 1 (A3)
IC buffer 1 (A4)
IC buffer 1 (A5)
IC buffer 1 (A6)
IC buffer 1 (A7)

relay pH meter

relay solenoid 1
relay solenoid2
relay pompa air

IC buffer 3

IC buffer 3 (Y4)

Solenoid 1

IC buffer 3 (Y5)

Solenoid 2

SOURCE VOLTAGE

IC buffer 3 (Y6)

V+ pH meter

pompa
air

LISTING PROGRAM

```
mov    p0,#0ffh    ;inisialisasi PORT 0 dengan 00h sebagai output
mov    p1,#0ffh    ;inisialisasi PORT 1 dengan FFh sebagai input digit pertama ;pH
                    meter
mov    p2,#0ffh    ;inisialisasi PORT 2 dengan FFh
mov    p3,#0ffh    ;inisialisasi PORT 3dengan FFh sebagai input digit kedua pH ;meter

isi_air:
       setb    p0.0           ;mematikan LED hijau
       setb    p0.1           ;mematikan LED merah
       setb    p0.2           ;mematikan LED kuning
       clr     p0.3           ;menyalakan solenoid valve 1 (pengisian air)
       setb    p0.4           ;mematikan solenoid valve 2
       clr     p0.5           ;menyalakan pompa air
       clr     p0.6           ;mematikan pH meter
       ljmp    timer10s        ;menunggu 10s

cek_pH:
       setb    p0.3           ;mematikan solenoid valve 1
       setb    p0.5           ;mematikan pompa air
       setb    p0.6           ;menyalakan pH meter
       ljmp    timer15s

nol:
mov    a,p3      ;data pada PORT 1 dipindahkan ke ACCUMULATOR (a)
orl    a,#80h    ;data pada A di OR dengan 80h
cjne   a,#0c0h,satu    ;pengecekan data A (PORT 1) sama atau tidak dengan c0h
jmp    error

satu:
cjne   a,#0f9h,dua    ;pengecekan data A (PORT 1) sama atau tidak dengan f9h
jmp    error

dua:
cjne   a,#0a4h,tiga    ;pengecekan data A (PORT 1) sama atau tidak dengan a4h
jmp    error

tiga:
cjne   a,#0b0h,empat ;pengecekan data A (PORT 1) sama atau tidak dengan b0h
jmp    error

empat:
cjne   a,#99h,lima    ;pengecekan data A (PORT 1)sama atau tidak dengan 99h
jmp    error

lima:
cjne   a,#92h,enam    ;pengecekan data A (PORT 1) sama atau tidak dengan 92h
```

```
jmp     error

enam:
cjne    a,#82h,tujuh    ;pengecekan data A (PORT 1) sama atau tidak dengan 82h
jmp     enam_nol

enam_nol:
mov     a,p1                    ;data pada PORT 3 dipindahkan ke A
orl     a,#80h                  ;data pada A di OR dengan 80h
cjne    a,#81h,enam_satu ;pengecekan data A (PORT 3) sama atau tidak dengan 81h
jmp     error

enam_satu:
cjne    a,#0cfh,enam_dua ;pengecekan data A (PORT 3) sama atau tidak dengan 0cfh
jmp     asam

enam_dua:
cjne    a,#92h,enam_tiga    ;pengecekan data A (PORT 3) sama atau tidak dengan 92h
jmp     asam

enam_tiga:
cjne    a,#86h,enam_empat ;pengecekan data A (PORT 3) sama atau tidak dengan 86h
jmp     asam

enam_empat:
cjne    a,#0cch,enam_lima ;pengecekan data A (PORT 3) sama atau tidak dengan 0cch
jmp     asam

enam_lima:
cjne    a,#0a4h,enam_enam  pengecekan data A (PORT 3) sama atau tidak dengan 0a4h
jmp     asam

enam_enam:
cjne    a,#0a0h,enam_tujuh ;pengecekan data A (PORT 3) sama atau tidak dengan 0a0h
jmp     normal

enam_tujuh:
cjne    a,#8fh,enam_delapan ;pengecekan data A (PORT 3) sama atau tidak dengan 8fh
jmp     normal

enam_delapan:
cjne    a,#80h,enam_sembilan ;pengecekan data A (PORT 3) sama atau tidak dengan 80h
jmp     normal
```

```
enam_sembilan:
cjne    a,#84h,enam_nol        ;pengecekan data A (PORT 3) sama atau tidak dengan 84h
jmp     normal


tujuh:
cjne    a,#0f8h,delapan        ;pengecekan data A (PORT 3) sama atau tidak dengan f8h
jmp     normal


delapan:
cjne    a,#80h,sembilan        ;pengecekan data A (PORT 1) sama atau tidak dengan 80h
jmp     delapan_nol


delapan_nol:
mov     a,p1           ;data pada PORT 3 dipindahkan ke A
orl     a,#80h         ;data pada A di OR dengan 80h
cjne    a,#81h,delapan_satu  ;pengecekan data A (PORT 3) sama atau tidak dengan 81h
jmp     normal


delapan_satu:
cjne    a,#0cfh,delapan_dua    ;pengecekan data A (PORT 3) sama atau tidak dengan 0cfh
jmp     normal


delapan_dua:
cjne    a,#92h,delapan_tiga    ;pengecekan data A (PORT 3) sama atau tidak dengan 92h
jmp     normal


delapan_tiga:
cjne    a,#86h,delapan_empat;pengecekan data A (PORT 3) sama atau tidak dengan 86h
jmp     normal


delapan_empat:
cjne    a,#0cch,delapan_lima ;pengecekan data A (PORT 3) sama atau tidak dengan 0cch
jmp     normal


delapan_lima:
cjne    a,#0a4h,delapan_enam ;pengecekan data A (PORT 3) sama atau tidak dengan 0a4h
jmp     basa


delapan_enam:
cjne    a,#0a0h,delapan_tujuh ;pengecekan data A (PORT 3) sama atau tidak dengan 0a0h
jmp     basa


delapan_tujuh:
cjne    a,#8fh,delapan_delapan ;pengecekan data A (PORT 3) sama atau tidak dengan 8fh
jmp     basa
```

```
delapan_delapan:
cjne    a,#80h,delapan_sembilan ;pengecekan data A (PORT 3) sama atau tidak dengan 80h
jmp     basa

delapan_sembilan:
cjne    a,#84h,delapan_nol    ;pengecekan data A (PORT 3) sama atau tidak dengan 84h
jmp     basa

sembilan:
cjne    a,#90h,cek_lagi    ;pengecekan data A (PORT 1) sama atau tidak dengan 84h
jmp     error

cek_lagi:
jmp     nol                ;pengecekkan ulang nilai pH

timer10s:
mov     r7,#204            ;10detik
acall   delay10s
jmp     cek_ph

timer15s:
mov     r6,#210            ;15detik
acall   delay15s
jmp     nol

timer30s:
mov     r5,#210            ; 15detik x 2
mov     r4,#210            ; = 30detik
acall   delay30s1
jmp     isi_air

delay10s:
mov     tmod,#01h
mov     tl0,#65h           ;membuat timer
mov     th0,#4fh ;         50ms
setb    tr0
jnb     tf0,$
clr     tr0
clr     tf0
djnz    r7,delay10s
ret
```

```
delay15s:
mov     tmod,#01h
mov     tl0,#0bfh       ;membuat timer
mov     th0,#01h        ;       72ms
setb    tr0
jnb     tf0,$
clr     tr0
clr     tf0
djnz    r6,delay15s
ret


delay30s1:
mov     tmod,#01h
mov     tl0,#0bfh       ;membuat timer
mov     th0,#01h        ;       72ms
setb    tr0
jnb     tf0,$
clr     tr0
clr     tf0
djnz    r5,delay30s1


delay30s2:
mov     tmod,#01h
mov     tl0,#0bfh       ;membuat timer
mov     th0,#01h        ;       72ms
setb    tr0
jnb     tf0,$
clr     tr0
clr     tf0
djnz    r4,delay30s2
ret


error:  ;menunjukkan 6 < pH dan pH > 8
clr     p0.6    ;mematikan pH meter
clr     p0.0    ;menyalakan LED hijau
clr     p0.1    ;menyalakan LED merah
clr     p0.2    ;menyalakan LED kuning
setb    p0.3    ;mematikan solenoid 1
setb    p0.4    ;mematikan solenoid 2
setb    p0.5            ;mematikan pompa air
acall   timer30s        ;menunggu selama 30s
```

```
normal:          ;menunjukkan 6.5 < pH < 8.5
clr     p0.6     ;mematikan pH meter
clr     p0.0     ;menyalakan LED hijau (normal)
setb    p0.1     ;mematikan LED merah (asam)
setb    p0.2     ;mematikan LED kuning (basa)
clr     p0.3     ;menyalakan solenoid valve 1 (normal)
setb    p0.4     ;mematikan solenoid valve 2 (tdk normal)
clr     p0.5     ;menyalakan pompa air
acall   timer30s        ;menunggu selama 30s

asam:   ;menunjukkan 6.1 <= pH <= 6.5
clr     p0.6     ;mematikan pH meter
setb    p0.0     ;mematikan LED hijau (normal)
clr     p0.1     ;menyalakan LED merah (asam)
setb    p0.2     ;mematikan LED kuning (basa)
setb    p0.3     ;mematikan solenoid valve 1 (normal)
clr     p0.4     ;menyalakan solenoid valve 2 (tdk normal)
clr     p0.5     ;menyalakan pompa air
acall   timer30s        ;menunggu selama 30s

basa:   ;menunjukkan 8.5 <= pH <= 8.9
clr     p0.6     ;mematikan pH meter
setb    p0.0     ;mematikan LED hijau (normal)
setb    p0.1     ;mematikan LED merah (asam)
clr     p0.2     ;menyalakan LED kuning (basa)
setb    p0.3     ;mematikan solenoid valve 1 (normal)
clr     p0.4     ;menyalakan solenoid valve 2 (tdk normal)
clr     p0.5             ;menyalakan pompa air
acall   timer30s        ;menunggu selama 30s

end
```

MANUAL pH METER HANNA INSTRUMENT HI 98107

pHep® is a rugged pH tester with replaceable electrode and removable reference junction. The instrument can be calibrated at two points by the user, simply acting on the offset and slope calibration trimmers.

pHep® is in compliance with the CE directives

SPECIFICATIONS

Range	0.0 to 14.0 pH
Resolution	0.1 pH
Accuracy (@20°C/68°F)	±0.1 pH
Typical EMC Deviation	±0.1 pH
Calibration	Manual, 2 point, through offset and slope trimmers
Environment	0 to 50°C (32 to 122°F); RH max 95%
Battery Type	4 x 1.5V alkaline
Battery Life	approx 700 hours of use
Dimensions	175 x 41 x 23 mm (6.9 x 1.6 x 0.9")
Weight	95 g (3.4 oz.)

ACCESSORIES

HI 73106	Spare electrode
HI 7004M	pH 4.01 solution, 230 mL bottle
HI 7007M	pH 7.01 solution, 230 mL bottle
HI 7010M	pH 10.01 solution, 230 mL
HI 70300M	Storage solution, 230 mL bottle
HI 7061M	Cleaning solution, 230 mL bottle
HI 731326	Calibration screwdriver (20 pcs)
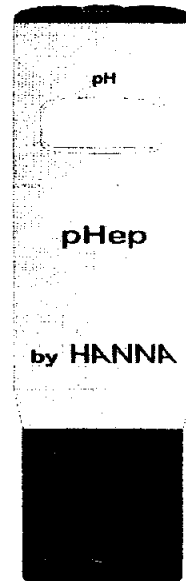
pHep® is a registered trademark of Hanna Instruments

HANNA instruments
www.hannainst.com

pHep®
HI 98107
Pocket-sized pH Meter

pH

pHep

by HANNA

CONDITIONING

- Remove the cap.
- To activate the electrode, immerse it in (HI70300) storage solution for 2 hours.

CALIBRATION

- Immerse the electrode in pH 7.01 (HI7007) buffer solution.
- Allow the reading to stabilize and with the supplied screwdriver, adjust the "pH7" calibration trimmer to read "7.0" pH.
- Rinse the electrode with tap water and immerse it into the second buffer.
- Use pH 4.01 (HI7004) if the solution to be measured is acidic (pH < 7), or pH 10.0 (HI7010) for alkaline samples (pH > 7).
- Allow the reading to stabilize and with the screwdriver adjust the "pH4/10" calibration trimmer to read "4.0" or "10.0" pH.

OPERATION

- Remove the protective cap, turn the pHep on, by sliding the ON/OFF switch on the top of the meter.
- Immerse it in the solution to be tested without exceeding the maximum immersion level.
- Stir gently and wait for the reading to stabilize.
- After use, switch the meter off, rinse the electrode with tap water and store it with a few drops of storage (HI70300) or pH7 (HI7007) solution in the protective cap. Always replace the protective cap after use.

NEVER USE DISTILLED OR DEIONIZED WATER FOR STORAGE PURPOSES.

- Large differences in pH readings (up to 1 pH) could be due to lack of calibration or dry electrode.

MAINTENANCE

The sensor should be kept moist at all times. For this purpose, always keep wet the tissue inside the protective cap. In case of erroneous readings even after an accurate conditioning and calibration, the reference junction might be contaminated or clogged.

Pull out 2 mm (1/8") of the cloth junction to renew the electrode reference (it is recommended to cut the cloth leaving always at least 2 mm - 1/8" over the reference compartment) and recalibrate the meter.

The cloth junction can be pulled out approximately 7 times. After this, the electrode should be replaced.

ELECTRODE REPLACEMENT

For replacing the electrode, contact your dealer or the nearest Hanna Service Center.

BATTERY REPLACEMENT

If calibration can not be performed or the display fades, batteries must be replaced. Slide off the battery compartment cover and replace all four 1.5V alkaline batteries while paying attention to the correct polarity.

Batteries should only be replaced in a non hazardous area and using the battery type specified in this instruction manual.

1

ΜΛXIΜ

Low Power, 3½ Digit A/D Converter

General Description

The Maxim ICL7126 is a monolithic analog to digital converter with very high input impedance. On-board active components include segment drivers, segment decoders, voltage reference and a clock circuit. The ICL7126 directly drives a non-multiplexed liquid crystal (LCD) display, requiring no external display drive circuitry. Significantly reduced power consumption makes the ICL7126 a superior device, especially for portable systems.

Versatility and accuracy are inherent features of this converter. The dual-slope conversion technique automatically rejects interference signals common in industrial environments. The true differential input and reference are particularly useful when making ratiometric measurements (ohms or bridge transducers), and the zero-integrator phase in Maxim's ICL7126 eliminates overrange hangover and hysteresis effects. The Zero Integrator phase also allows the use of larger auto zero capacitors reducing noise further. Finally, this device offers high accuracy by lowering rollover error to less than one count and zero reading drift to less than $1\mu V/°C$.

Applications

These devices can be used in a wide range of digital panel meter applications. Most applications, however, involve the measurement and display of analog data:

Pressure	Conductance
Voltage	Current
Resistance	Speed
Temperature	Material Thickness

## Pin Configuration

See ICL7106 for 44 Lead PLCC Pin Configuration
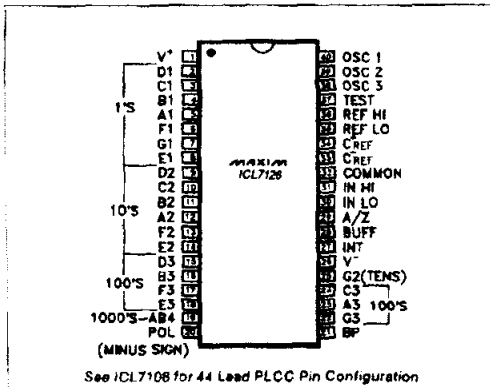
Features

♦ Improved 2nd Source! (See 3rd page for "Maxim Advantage™").

♦ Power dissipation guaranteed less than 1mW–9V battery life 3000 hours typical

♦ Guaranteed first reading recovery from overrange

♦ Zero Input Gives Zero Reading

♦ Drives LCD Displays Directly

♦ Low Noise (15µV p-p) without hysteresis or overrange hangover

♦ True Differential Reference and Input

♦ Monolithic, Low Power CMOS

Ordering Information

PART	TEMP. RANGE	PACKAGE
ICL7126CPL	0°C to +70°C	40 Lead Plastic DIP
ICL7126CJL	0°C to +70°C	40 Lead CERDIP
ICL7126CQH	0°C to +70°C	44 Lead Plastic Chip Carrier
ICL7126C/D	0°C to +70°C	Dice

Typical Operating Circuit

FULL SCALE INPUT	VREF
2.000 V	1.000 V
200.0 mV	100.0 mV

(Detailed Circuit Diagram—Figure 1 & 2)
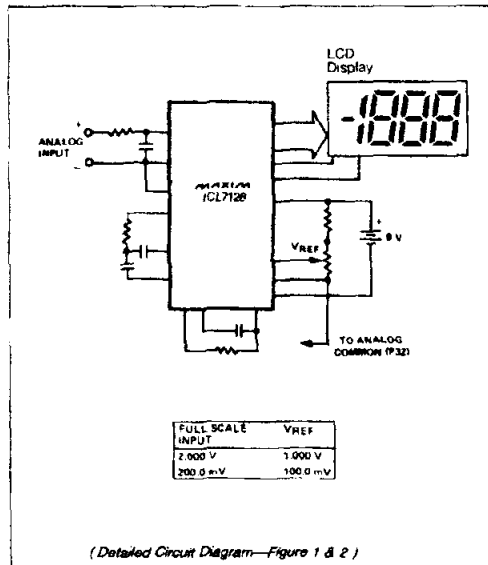
The "Maxim Advantage™" signifies an upgraded quality level. At no additional cost we offer a second-source device that is subject to the following: guaranteed performance over temperature along with tighter test specifications on many key parameters; and device enhancements, when needed, that result in improved performance without changing the functionality.

Low Power, 3½ Digit A/D Converter

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V⁺ to V⁻) 15V
Analog Input Voltage (either input)(Note 1) ....V⁺ to V⁻
Reference Input Voltage (either input) ....V⁺ to V⁻
Clock Input ....TEST to V⁺

Power Dissipation (Note 2)
   Cerdip Package 1000mW
   Plastic Package 800mW
Operating Temperature Range .... 0°C to +70°C
Storage Temperature Range .... -65°C to +160°C
Lead Temperature (Soldering, 60 sec.) .... +300°C

Note 1: Input voltages may exceed the supply voltages, provided the input current is limited to ±100μA.

Note 2: Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (Note 3, 7)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Zero Input Reading	$V_{IN} = 0.0V$ Full-Scale = 200.0mV	−000.0	±000.0	+000.0	Digital Reading
Ratiometric Reading	$V_{IN} = V_{REF}$, $V_{REF} = 100mV$	999	999/1000	1000	Digital Reading
Roll-Over Error (Difference in reading for equal positive and negative reading near full-scale)	$-V_{IN} = +V_{IN} = 200.0mV$	−1	±0.2	+1	Counts
Linearity (Max. deviation from best straight line fit)	Full-Scale = 200mV or Full-Scale = 2.000V	−1	±0.02	+1	Counts
Common-Mode Rejection Ratio (Note 4)	$V_{CM} = ±1V$, $V_{IN} = 0V$ Full-Scale = 200.0mV		50		μV/V
Noise (Pk-Pk value not exceeded 95% of time)	$V_{IN} = 0V$, Full-Scale = 200.0mV		15		μV
Leakage Current @ Input	$V_{IN} = 0V$		1	10	pA
Zero Reading Drift	$V_{IN} = 0V$, 0°C < T_A < +70°C		0.2	1	μV/°C
Scale Factor Temperature Coefficient	$V_{IN} = 199.0mV$, 0°C < T_A < +70°C (Ext. Ref. 0ppm/°C)		1	5	ppm/°C
Supply Current (Does not include COMMON current)	$V_{IN} = 0V$ (Note 6)		50	100	μA
Analog COMMON Voltage (With respect to positive supply)	250kΩ between Common and Positive Supply	2.4	2.8	3.2	V
Temp. Coeff. of Analog COMMON (With respect to positive supply)	250kΩ between Common and Positive Supply		80		ppm/°C
Pk-Pk Segment Drive Voltage (Note 5)	V⁺ to V⁻ = 9V	4	5	6	V
Pk-Pk Backplane Drive Voltage (Note 5)	V⁺ to V⁻ = 9V	4	5	6	V
Power Dissipation Capacitance	vs Clock Frequency		40		pF

Note 3: Unless otherwise noted, specifications apply at $T_A = 25°C$, $f_{CLOCK} = 16kHz$ and are tested in the circuit of Figure 1.

Note 4: Refer to "Differential Input" discussion.

Note 5: Backplane drive is in phase with segment drive for "off" segment, 180° out of phase for "on" segment. Frequency is 20 times conversion rate. Average DC component is less than 50mV.

Note 6: 48kHz oscillator, Figure 2, increases current by 20μA (typ).

Note 7: Extra capacitance of CERDIP package changes oscillator resistor value to 470kΩ or 150kΩ (1 reading/sec or 3 readings/sec).

The electrical characteristics above are a reproduction of a portion of Intersil's copyrighted (1983/1984) data book. This information does not constitute any representation by Maxim that Intersil's products will perform in accordance with these specifications. The "Electrical Characteristics Table" along with the descriptive excerpts from the original manufacturer's data sheet have been included in this data sheet solely for comparative purposes.

MAXIM

/VI/IXI/VI

Low Power, 3½ Digit A/D Converter

- ◆ Low Noise
- ◆ Key Parameters Guaranteed over Temperature
- ◆ Guaranteed Overload Recovery Time
- ◆ Significantly Improved ESD Protection (Note 9)

- ◆ Negligible Hysteresis
- ◆ Increased Maximum Rating for Input Current (Note 10)
- ◆ Maxim Quality and Reliability

ABSOLUTE MAXIMUM RATINGS: This device conforms to the Absolute Maximum Ratings on adjacent page.

ELECTRICAL CHARACTERISTICS: Specifications below satisfy or exceed all "tested" parameters on adjacent page.

(V⁺ 9V; T_A = 25°C; f_{CLOCK} = 16kHz; test circuit - Figure 1; unless noted)

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Zero Input Reading	V_{IN} = 0.0V, Full Scale = 200.0mV T_A = 25°C (Note 8) 0° ≤ T_A ≤ +70°C (Note 12)	000.0 −000.0	±000.0 ±000.0	+000.0 +000.0	Digital Reading
Ratiometric Reading	V_{IN} = V_{REF}, V_{REF} = 100mV T_A = 25°C (Note 8) 0° ≤ T_A ≤ +70°C (Note 12)	999 998	999/1000 999/1000	1000 1001	Digital Reading
Rollover Error (Difference in reading for equal positive and negative reading near Full Scale)	−V_{IN} = −V_{IN} 200.0mV T_A = 25°C (Note 8) 0° ≤ T_A ≤ +70°C (Note 12)	1	±.2 ±.2	+1	Counts
Linearity (Max. deviation from best straight line fit)	Full Scale = 200.0mV or full scale = 2.000V	−1	±.2	+1	Counts
Common Mode Rejection Ratio	V_{CM} = ±1V, V_{IN} = 0V Full Scale = 200.0mV		5		µV/V
Noise (Pk-Pk value not exceeded 95% of time)	V_{IN} = 0V Full Scale = 200.0mV		10		µV
Input Leakage Current	V_{IN} = 0 T_A = 25°C (Note 8) 0° ≤ T_A ≤ +70°C		1	10 200	pA
Zero Reading Drift	V_{IN} = 0 0° ≤ T_A ≤ +70°C (Note 8)		0.2	1	µV/°C
Scale Factor Temperature Coefficient	V_{IN} = 199.0mV 0° ≤ T_A ≤ +70°C (Ext. Ref. 0ppm/°C) (Note 8)		1	5	ppm/°C
V⁺ Supply Current	V_{IN} = 0 T_A = 25°C 0° ≤ T_A ≤ +70°C		60	100 120	µA
Analog Common Voltage (with respect to Pos. Supply)	250kΩ between Common & Pos. Supply	2.6	2.8	3.2	V
Temp. Coeff. of Analog Common (with respect to Pos. Supply)	250kΩ between Common & Pos. Supply		75		ppm/°C
Pk-Pk Segment Drive Voltage Pk-Pk Backplane Drive Voltage	V⁺ to V⁻ = 9V	4	5	6	V
Test Pin Voltage	With respect to V⁺	4	5	6	V
Overload Recovery Time (Note 11)	V_{IN} changing from ± 10V to 0V		0	1	Measurement Cycles

Note 8: Test condition is V_{IN} applied between pins IN-HI and IN-LO through a 1MΩ series resistor as shown in Figure 1.

Note 9: All pins are designed to withstand electrostatic discharge (ESD) levels in excess of 2000V. (Test circuit per Mil Std 883, Method 3015.1)

Note 10: Input voltages may exceed the supply voltage provided the input current is limited to +1mA (This revises Note 1 on adjacent page).

Note 11: Number of measurement cycles for display to give accurate reading.

Note 12: 1MΩ resistor is removed from circuits in Figure 1.
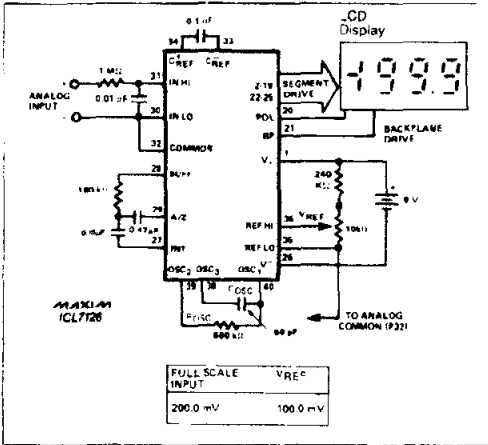
Low Power, 3½ Digit A/D Converter

Figure 1. Maxim ICL7126 Typical Operating Circuit
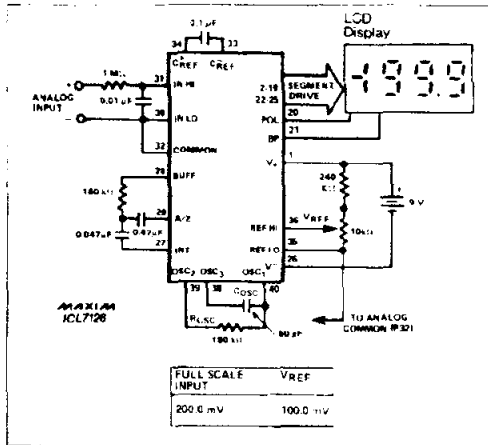Clock Frequency 16kHz (1 reading/sec)

FULL SCALE INPUT	V$_{REF}$
200.0 mV	100.0 mV

Figure 2. Maxim ICL7126 Typical Operating Circuit
Clock Frequency 48kHz (3 readings/sec)

FULL SCALE INPUT	V$_{REF}$
200.0 mV	100.0 mV

Analog Section

Figure 3 shows the Block Diagram of the Analog Section for the ICL7126. Each measurement cycle is divided into four phases:

1. Auto-Zero (A-Z)
2. Signal Integrate (INT)
3. Reference De-Integrate (DI)
4. Zero Integrator (ZI)

Auto-Zero Phase

Three events occur during auto-zero. The inputs, IN-HI and IN-LO, are disconnected from the pins and internally shorted to analog common. The reference capacitor is charged to the reference voltage. And lastly, a feedback loop is closed around the system to charge the auto-zero capacitor CAZ to compensate for offset voltages in the comparator, buffer amplifier and integrator. The inherent noise of the system determines the A-Z accuracy.

Signal Integrate Phase

The internal input high (IN-HI) and input low (IN-LO) are connected to the external pins, the internal short is removed and the auto-zero loop is opened. The converter then integrates the differential voltage between IN-HI and IN-LO for a fixed time. This differential voltage can be within a wide common-mode range (within one volt of either supply). If, however, the input signal has no return with respect to the converter power supply, IN-LO can be tied to analog common to establish the correct common-mode voltage. The polarity of the integrated signal is determined at the end of this phase.

Reference De-Integrate

IN-HI is connected across the previously charged reference capacitor and IN-LO is internally connected to analog common. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The input signal determines the time required for the output to return to zero. The digital reading displayed is:

$$1000 \times \frac{V_{IN}}{V_{REF}}$$

Zero Integrator Phase

Input low is shorted to analog COMMON and the reference capacitor is charged to the reference voltage. A feedback loop is closed around the system to input high, causing the integrator output to return to zero. This phase normally lasts between 11 and 140 clock pulses but is extended to 740 clock pulses after a "heavy" over range conversion.

Differential Reference

The reference voltage can be generated anywhere within the power supply voltage of the converter. The main source of common-mode error is a roll-over voltage. This is caused by the reference capacitor losing or gaining charge to stray capacitance on its nodes. The reference capacitor can gain charge (increase voltage) if there is a large common-mode voltage. This is the result of a positive signal de-integration. In contrast, the reference capacitor will lose charge (decrease voltage) when de-integrating a negative input signal. Rollover error is caused by this difference in reference for positive or negative input voltages. This error can be held to less than half a count for the worst-case condition by selecting a reference capacitor that is large enough in comparison to the stray capacitance. (See component value selection.)
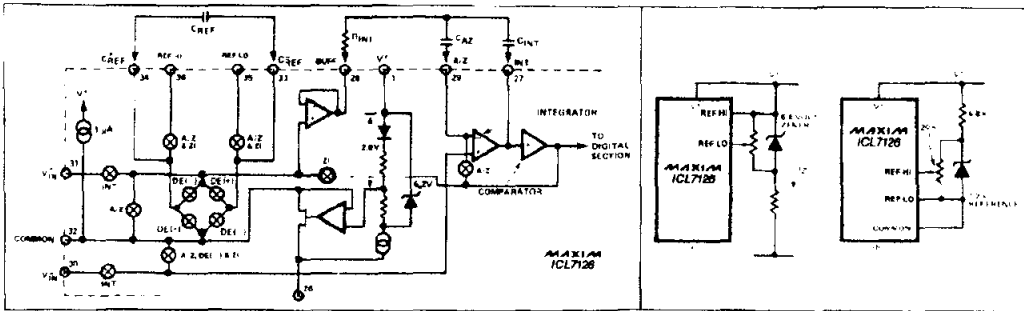
MAXIM

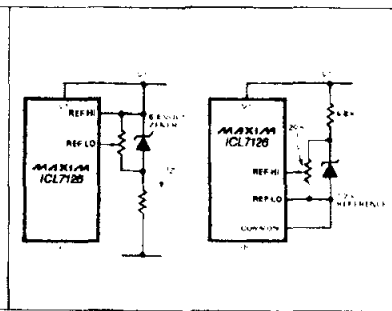# Low Power, 3½ Digit A/D Converter

Figure 3. Analog Section ICL7126

Figure 4. Using an External Reference

Differential Input

Differential voltages anywhere within the common-mode range of the input amplifier can be accepted by the input (specifically from 1V below the positive supply to 1.5V above the negative supply). The system has a CMRR of 86dB (typ) in this range. Care must be exercised, however, to ensure that the integrator output does not saturate, since the integrator follows the common-mode voltage. A large positive common-mode voltage with a near full-scale negative differential input voltage is a worst-case condition. When most of the integrator output swing has been used up by the positive common-mode voltage, the negative input signal drives the integrator more positive. The integrator swing can be reduced to less than the recommended 2V full-scale swing with no loss of accuracy in these critical applications. The integrator output can swing within 0.3V of either supply without loss of linearity.

Analog Common

The primary purpose of this pin is to set the common-mode voltage for battery operation. This is useful for any system where the input signals are floating with respect to the power supply. A voltage of approximately 2.8V less than the positive supply is set by this pin. The Analog Common has some of the attributes of a reference voltage. If the total supply voltage is large enough to cause the zener to regulate (>7V), the common voltage will have a low output impedance (approximately 15Ω), a temperature coefficient of typically 80 ppm/°C and a low voltage coefficient (.001%).

During auto-zero and reference integrate the internal input low is connected to Analog Common. If IN-LO is different from Analog-Common, a common-mode voltage exists in the system and is taken care of by the excellent CMRR of the converter. In some applications, however, IN-LO will be set at a fixed known voltage (e.g., power supply common). Whenever possible Analog Common should be tied to the same point, thus removing the common-mode voltage from the converter. The same holds true for the reference voltage. If convenient, the reference should be referenced to analog common as shown in Figure 4B. This will remove the common-mode voltage from the reference system.

Analog common is internally tied to an N-channel FET that can sink 500 µA or more of current. This will hold the analog common voltage 2.8V below the positive supply (when a source is trying to pull the common line positive). There is only 1 µA of source current, however, so common may easily be tied to a more negative voltage, thus over-riding the internal reference.

Test

Two functions are performed by the test pin. The first is using this pin as the negative supply on the 7126. This is useful for externally generated segment drivers or any other annunciators the user may want to include on the LCD. This pin is coupled to the internally generated digital supply through a 500Ω resistor. This application is illustrated in Figures 5 & 6.

A lamp test is the second function. All segments will be turned on and the display should read −1888, when TEST is pulled high (V+).

Caution: In the lamp test mode, the segments have a constant dc voltage (no square wave). This can burn the LCD (display) if left in this mode for several minutes.
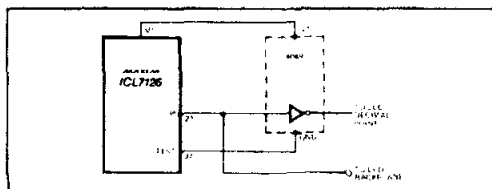

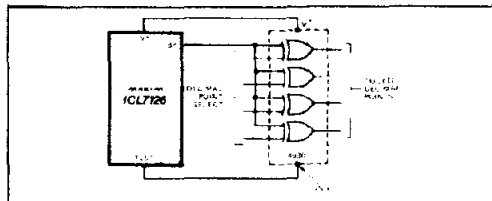Figure 5. Simple Inverter for Fixed Decimal Point

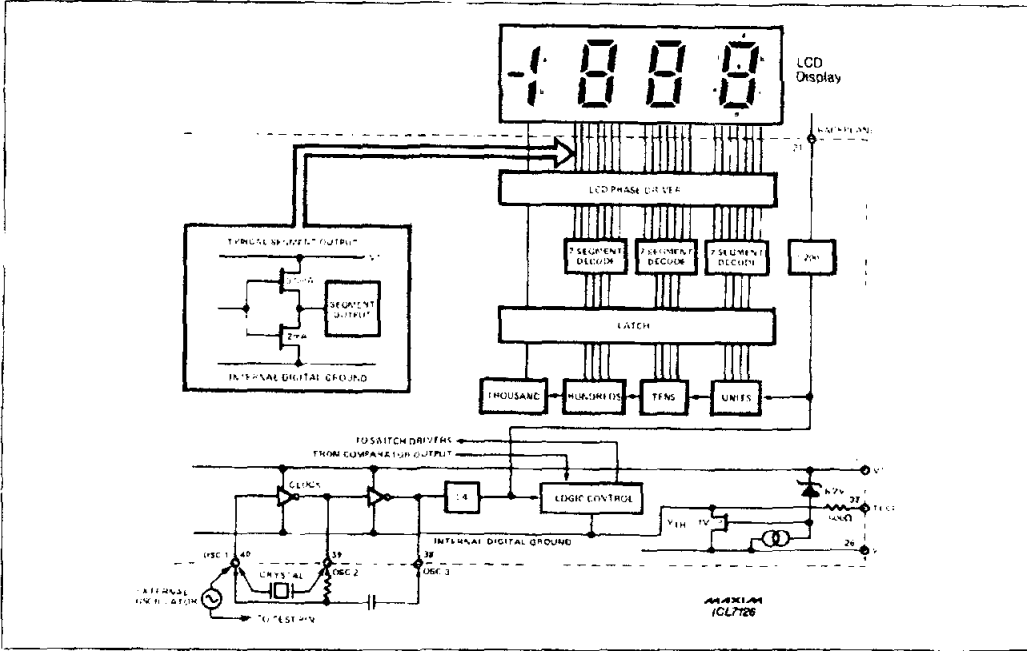Figure 6. Exclusive "OR" Gate for Decimal Point Drive

MAXIM

Figure 7. ICL7126 Digital Section

Digital Section

The digital section for the ICL7126 is illustrated in Figure 7. In Figure 7, an internal digital ground is generated from a 6V zener diode and a large P channel source follower. This supply is made stiff in effort to absorb the large capacitive currents when the back plane (BP) voltage is switched. The BP frequency is calculated by dividing the clock frequency by 800. For example, with a clock frequency of 48kHz (3 readings per second), the backplane will be a 60Hz square wave with a nominal amplitude of 5V. The segments are driven at the same frequency and amplitude. Note that these are out-of-phase when the BP is On and in-phase when OFF. Negligible dc voltage exists across the segments in either case.

The polarity indication is "on" for negative analog inputs, for the ICL7126. If desired IN-HI and IN-LO can be reversed giving a "on" for positive analog inputs.

System Timing

The clocking circuitry for the ICL7126 is illustrated in Figure 7. Three approaches can be used:

1. A crystal between pins 39 and 40.

2. An external oscillator connected to pin 40.

3. An RC oscillator using all three pins.

The decade counters are driven by the clock frequency which is divided by four. This frequency is then further divided to form the four convert-cycle phases, namely: signal integrate (1000 counts), reference de-integrate (0 to 2000 counts), auto-zero (260 to 2989 counts) and zero integrator (11 to 740).

The signal integration should be a multiple of 60Hz to achieve a maximum rejection of 60Hz pickup. Oscillator frequencies of 33⅓kHz, 40kHz, 48kHz, 60kHz, 80kHz, 120kHz, 240kHz, etc., should be selected. Similarly, for 50Hz rejection, oscillator frequencies of 200kHz, 100kHz, 66⅔kHz, 50kHz, 40kHz, etc., are appropriate. Note that 40kHz (2.5 readings/second) will reject both 50 and 60Hz (also 400 and 440Hz).

Auto-zero receives the unused portion of reference deintegrate for signals less than full-scale. A complete measurement cycle is 4,000 counts (16,000) clock pulses), independent of input voltage. As an example, an oscillator frequency of 16kHz would be used to obtain one reading per second.

MAXIM

Low Power, 3½ Digit A/D Converter

Component Value Selection

Auto-Zero Capacitor

The noise of the system is influenced by the auto-zero capacitor. For a 2V scale, a $0.1\mu F$ capacitor is adequate. While the Maxim ICL7126 will operate with a $0.33\mu F$ capacitor, a $0.47\mu F$ capacitor is recommended for the 200mV full scale where noise rejection is very important. Due to the ZI phase, noise can be reduced by using a larger auto-zero capacitor without causing hysteresis or overrange hangover problems.

Reference Capacitor

For most applications, a $0.1\mu F$ capacitor is acceptable. However, a large value is needed to prevent roll over error where a large common-mode voltage exists (i.e., the REF-LO pin is not at analog common) and a 200mV scale is used. Generally, the roll over error will be held to half a count by using a $1.0\mu F$ capacitor.

Integrating Capacitor

To ensure that the integrator will not saturate (approximately 0.3V from either supply), an appropriate integrating capacitor must be selected. A nominal ±2V full-scale integrator swing is acceptable when the analog common is used as a reference. The nominal value for CINT is $0.15\mu F$ at one reading per second. (16kHz clock). This value should be changed in inverse proportion to maintain the same output swing if a different oscillator frequency is used.

The integrating capacitor must have low dielectric absorption to minimize linearity errors. Polypropylene capacitors are recommended for this application.

Integrating Resistor

The integrator and the buffer amplifier both have a class A output stage with $6\mu A$ of quiescent current and can supply $1\mu A$ of drive current with negligible non-linearity. The integrating resistor should be large enough to keep the amplifiers in the linear region over the entire input voltage range. The resistor value, however, should be low enough that undue leakage requirements are not placed on the PC boards. For a 200mV scale, a $180k\Omega$ resistor is recommended; (2V scale/1.8MEGΩ).

Reference Voltage

An analog input voltage of V_{IN} equal to 2 (V_{REF}) is required to generate full scale output of 2000 counts. Thus, for 2V and 200mV scales, V_{REF} should equal 1V and 100mV respectively. However, there will exist a scale factor other than the unity between the input voltage and the digital reading in many applications where the A/D is connected to a transducer.

As an example, the designer may like to have a full scale reading in a weighing system when the voltage from the transducer is 0.682V. The designer should use the input voltage directly and select V_{REF} at 0.341V instead of dividing the input down to 1V. A suitable value of the integrating resistor would be $330k\Omega$. This provides for a slightly quieter system and avoids a divider network on the input. Another advantage of this system occurs when the digital reading of zero is desired for $V_{IN} \neq$ zero. Examples are temperature and weighing systems with variable tare. By connecting the voltage transducer between V_{IN} positive and common, and the variable (or fixed) offset voltage between common and V_{IN} negative, the offset rating can be conveniently generated.

Oscillator Components

A 50pF capacitor is recommended for all ranges of frequency and the resistor is selected from the equation $f \approx 0.45/RC$. For 48kHz clock (3 readings/second), $R = 180k\Omega$, for 16kHz, $R = 560k\Omega$.
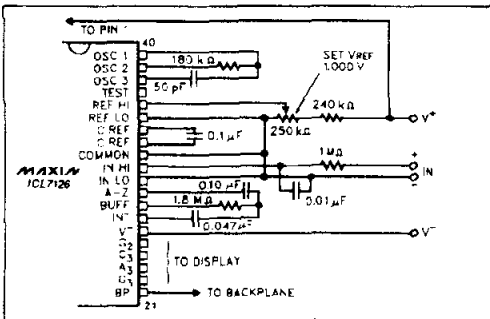
Typical Applications

Figure 8. Recommended Component Values for 2.000V Full-Scale, 3 Readings/Sec. For 1 reading/sec, change CINT, ROSC to values of Figure 1.
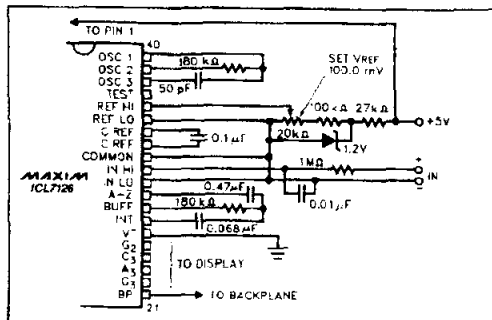

Figure 9. 7126 Operated from Single +5V Supply. An external reference must be used in this application, since the voltage between V⁺ and V⁻ is insufficient for correct operation of the internal reference.
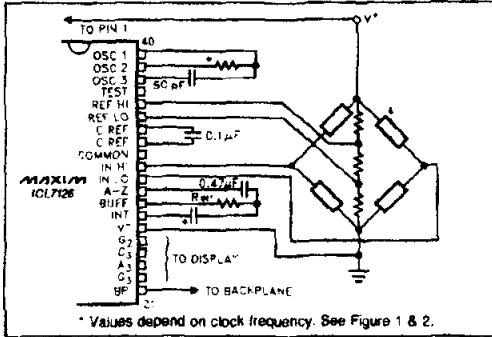
Low Power, 3½ Digit A/D Converter

ICL7126

* Values depend on clock frequency. See Figure 1 & 2.

Figure 10. 7126 Measuring Ratiometric Values of Quad Load Cell. The resistor values within the bridge are determined by the desired sensitivity.
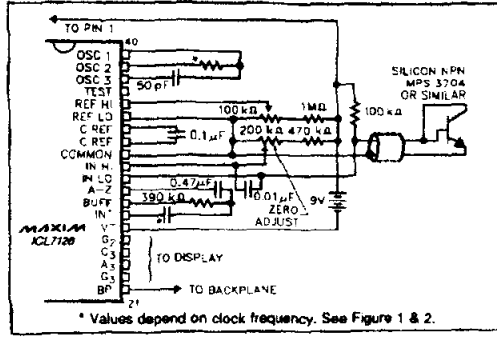

* Values depend on clock frequency. See Figure 1 & 2.

Figure 11. 7126 used as a Digital Centigrade Thermometer. A silicon diode-connected transistor has a temperature coefficient of about -2mV/° C/. Calibration is achieved by placing the sensing transistor in ice water and adjusting the zeroing potentiometer for a 000.0 reading. The sensor should then be placed in boiling water and the scale-factor potentiometer adjusted for a 100.0 reading.

Chip Topography
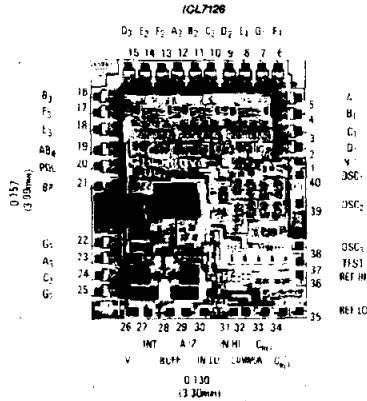
ICL7126

MAXIM

MOTOROLA

OCTAL BUS TRANSCEIVER

The SN54/74LS245 is an Octal Bus Transmitter/Receiver designed for 8-line asynchronous 2-way data communication between data buses. Direction Input (DR) controls transmission of Data from bus A to bus B or bus B to bus A depending upon its logic level. The Enable input (E) can be used to isolate the buses.

- Hysteresis Inputs to Improve Noise Immunity
- 2-Way Asynchronous Data Bus Communication
- Input Diodes Limit High-Speed Termination Effects
- ESD > 3500 Volts

LOGIC AND CONNECTION DIAGRAMS DIP (TOP VIEW)
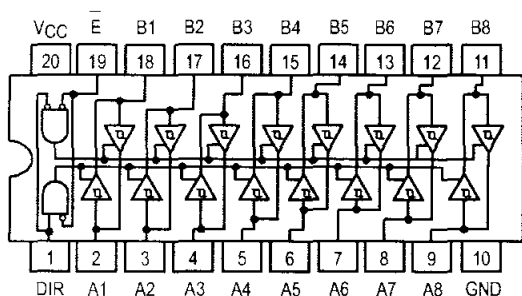
TRUTH TABLE

INPUTS		OUTPUT
E	DIR	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	Isolation

H = HIGH Voltage Level
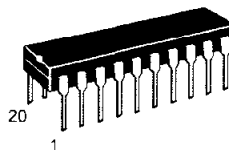L = LOW Voltage Level
X = Immaterial
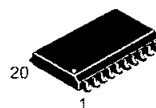

SN54/74LS245

OCTAL BUS TRANSCEIVER

LOW POWER SCHOTTKY
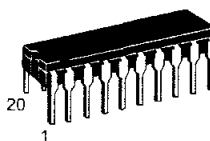
J SUFFIX
CERAMIC
CASE 732-03

N SUFFIX
PLASTIC
CASE 738-03

DW SUFFIX
SOIC
CASE 751D-03

ORDERING INFORMATION

SN54LSXXXJ   Ceramic
SN74LSXXXN   Plastic
SN74LSXXXDW SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54	4.5	5.0	5.5	V
		74	4.75	5.0	5.25	
T_A	Operating Ambient Temperature Range	54	−55	25	125	°C
		74	0	25	70	
I_{OH}	Output Current — High	54, 74			−3.0	mA
		54			−12	mA
		74			−15	
I_{OL}	Output Current — Low	54			12	mA
		74			24	

SN54/74LS245

CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

Symbol	Parameter		Min	Typ	Max	Unit	Test Conditions	
IH	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
IL	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
$V_{T+}-V_{T-}$	Hysteresis		0.2	0.4		V	V_{CC} = MIN	
IK	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
OH	Output HIGH Voltage	54, 74	2.4	3.4		V	V_{CC} = MIN, I_{OH} = −3.0 mA	
		54, 74	2.0			V	V_{CC} = MIN, I_{OH} = MAX	
OL	Output LOW Voltage	54, 74		0.25	0.4	V	I_{OL} = 12 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 24 mA	
OZH	Output Off Current HIGH				20	μA	V_{CC} = MAX, V_{OUT} = 2.7 V	
OZL	Output Off Current LOW				−200	μA	V_{CC} = MAX, V_{OUT} = 0.4 V	
H	Input HIGH Current	A or B, DR or E			20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
		DR or E			0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
		A or B			0.1	mA	V_{CC} = MAX, V_{IN} = 5.5 V	
L	Input LOW Current				−0.2	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
OS	Output Short Circuit Current (Note 1)		−40		−225	mA	V_{CC} = MAX	
CC	Power Supply Current Total, Output HIGH				70	mA	V_{CC} = MAX	
	Total, Output LOW				90			
	Total at HIGH Z				95			

Note 1: Not more than one output should be shorted at a time, nor for more than 1 second.

**CHARACTERISTICS** (T_A = 25°C, V_{CC} = 5.0 V, T_{RISE}/T_{FALL} ≤ 6.0 ns)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
LH HL	Propagation Delay, Data to Output		8.0 8.0	12 12	ns	C_L = 45 pF, R_L = 667 Ω
ZH	Output Enable Time to HIGH Level		25	40	ns	
ZL	Output Enable Time to LOW Level		27	40	ns	
LZ	Output Disable Time from LOW Level		15	25	ns	C_L = 5.0 pF, R_L = 667 Ω
HZ	Output Disable Time from HIGH Level		15	25	ns	

National *Semiconductor*

June 1989

54LS14/DM74LS14 Hex Inverters with Schmitt Trigger Inputs

General Description

This device contains six independent gates each of which performs the logic INVERT function. Each input has hysteresis which increases the noise immunity and transforms a slowly changing input signal to a fast changing, jitter free output.

Connection Diagram

Dual-In-Line Package
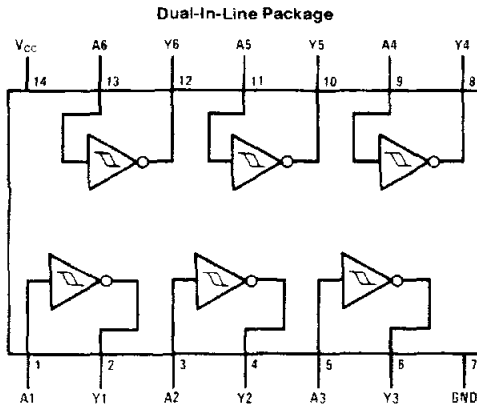
TL/F/6953-1

Order Number 54LS14DMQB, 54LS14FMQB,
54LS14LMQB, DM74LS14M or DM74LS14N
See NS Package Number E20A, J14A, M14A, N14A or W14B

Function Table

$Y = \overline{A}$

Input	Output
A	Y
L	H
H	L

H = High Logic Level
L = Low Logic Level

Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage	7V
Input Voltage	7V
Operating Free Air Temperature Range	
54LS	$-55°C$ to $+125°C$
DM74LS	$0°C$ to $+70°C$
Storage Temperature Range	$-65°C$ to $+150°C$

Note: *The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.*

Recommended Operating Conditions

Symbol	Parameter	54LS14			DM74LS14			Units
		Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{T+}	Positive-Going Input Threshold Voltage (Note 1)	1.5	1.6	2.0	1.4	1.6	1.9	V
V_{T-}	Negative-Going Input Threshold Voltage (Note 1)	0.6	0.8	1.1	0.5	0.8	1	V
HYS	Input Hysteresis (Note 1)	0.4	0.8		0.4	0.8		V
I_{OH}	High Level Output Current			-0.4			0.4	mA
I_{OL}	Low Level Output Current			4			8	mA
T_A	Free Air Operating Temperature	-55		125	0		70	°C

Electrical Characteristics over recommended operating free air temperature range (unless otherwise noted)

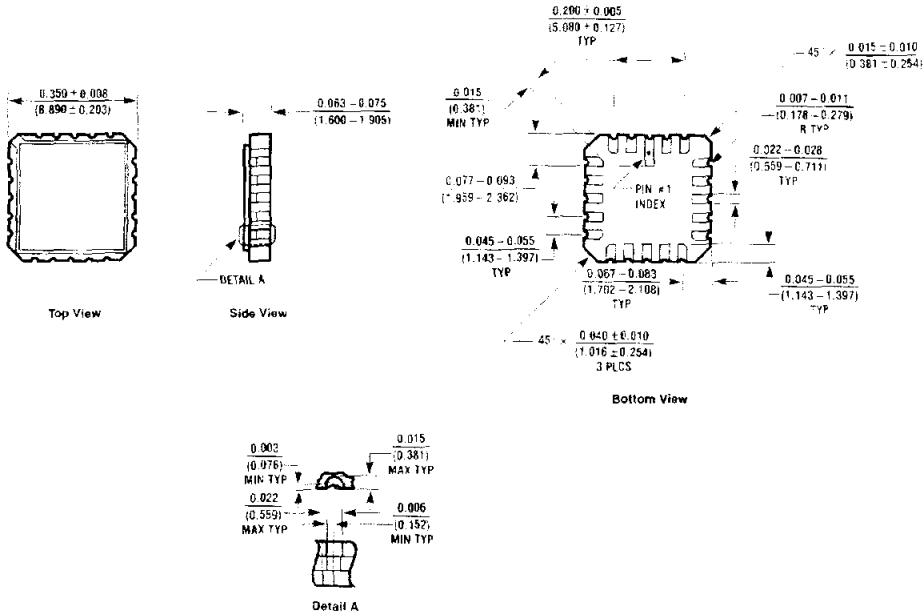| Symbol	Parameter	Conditions		Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = -18 mA				-1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max	54LS	2.5	3.4		V
			DM74	2.7	3.4		
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min	54LS		0.25	0.4	V
			DM74		0.35	0.5	
		V_{CC} = Min, I_{OL} = 4 mA	DM74		0.25	0.4	
I_{T+}	Input Current at Positive-Going Threshold	V_{CC} = 5V, V_I = V_{T-}	DM74		-0.14		mA
I_T	Input Current at Negative-Going Threshold	V_{CC} = 5V, V_I = V_{T-}	DM74		-0.18		mA
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V	DM74			0.1	mA
		V_{CC} = Max, V_I = 10.0V	54LS				
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.7V				20	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				-0.4	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	54LS	-20		-100	mA
			DM74	-20		-100	
I_{CCH}	Supply Current with Outputs High	V_{CC} = Max			8.6	16	mA
I_{CCL}	Supply Current with Outputs Low	V_{CC} = Max			12	21	mA

Note 1: V_{CC} = 5V.

Note 2: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 3: Not more than one output should be shorted at a time, and the duration should not exceed one second.

Switching Characteristics at V_{CC} = 5V and T_A = 25°C (See Section 1 for Test Waveforms and Output Load)

Symbol	Parameter	R_L = 2 kΩ				Units
		C_L = 15 pF		C_L = 50 pF		
		Min	Max	Min	Max	
t_{PLH}	Propagation Delay Time Low to High Level Output	5	22	8	25	ns
t_{PHL}	Propagation Delay Time High to Low Level Output	5	22	10	33	ns

Physical Dimensions inches (millimeters)

Top View

Side View

DETAIL A

Bottom View

0.200 + 0.005
(5.080 + 0.127)
TYP

0.015
(0.381)
MIN TYP

0.077 − 0.093
(1.959 − 2.362)

0.045 − 0.055
(1.143 − 1.397)
TYP

0.067 − 0.083
(1.702 − 2.108)
TYP

45° × 0.040 ± 0.010
(1.016 ± 0.254)
3 PLCS

PIN #1
INDEX

45° × 0.015 ± 0.010
(0.381 ± 0.254)

0.007 − 0.011
(0.178 − 0.279)
R TYP

0.022 − 0.028
(0.559 − 0.711)
TYP

0.045 − 0.055
(1.143 − 1.397)
TYP

0.350 + 0.008
(8.890 ± 0.203)

0.063 − 0.075
(1.600 − 1.905)

Detail A

0.003
(0.076)
MIN TYP

0.022
(0.559)
MAX TYP

0.015
(0.381)
MAX TYP

0.006
(0.152)
MIN TYP

Ceramic Leadless Chip Carrier (E)
Order Number 54LS14LMQB
NS Package Number E20A

Physical Dimensions inches (millimeters) (Continued)
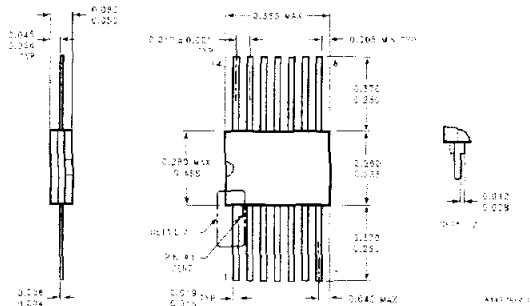
14-Lead Ceramic Flat Package (W)
Order Number 54LS14FMQB
NS Package Number W14B

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

FAIRCHILD
SEMICONDUCTOR ™

BD135/137/139

Medium Power Linear and Switching Applications
• Complement to BD136, BD138 and BD140 respectively

1   TO-126

1. Emitter   2.Collector   3.Base

NPN Epitaxial Silicon Transistor

Absolute Maximum Ratings T_C=25°C unless otherwise noted

Symbol	Parameter		Value	Units
V_{CBO}	Collector-Base Voltage	: BD135	45	V
		: BD137	60	V
		: BD139	80	V
V_{CEO}	Collector-Emitter Voltage	: BD135	45	V
		: BD137	60	V
		: BD139	80	V
V_{EBO}	Emitter-Base Voltage		5	V
I_C	Collector Current (DC)		1.5	A
I_{CP}	Collector Current (Pulse)		3.0	A
I_B	Base Current		0.5	A
P_C	Collector Dissipation (T_C=25°C)		12.5	W
P_C	Collector Dissipation (T_a=25°C)		1.25	W
T_J	Junction Temperature		150	°C
T_{STG}	Storage Temperature		- 55 ~ 150	°C

Electrical Characteristics T_C=25°C unless otherwise noted

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V_{CEO}(sus)	Collector-Emitter Sustaining Voltage					
	: BD135	I_C = 30mA, I_B = 0	45			V
	: BD137		60			V
	: BD139		80			V
I_{CBO}	Collector Cut-off Current	V_{CB} = 30V, I_E = 0			0.1	μA
I_{EBO}	Emitter Cut-off Current	V_{EB} = 5V, I_C = 0			10	μA
h_{FE1}	DC Current Gain : ALL DEVICE	V_{CE} = 2V, I_C = 5mA	25			
h_{FE2}	: ALL DEVICE	V_{CE} = 2V, I_C = 0.5A	25			
h_{FE3}	: BD135	V_{CE} = 2V, I_C = 150mA	40		250	
	: BD137, BD139		40		160	
V_{CE}(sat)	Collector-Emitter Saturation Voltage	I_C = 500mA, I_B = 50mA			0.5	V
V_{BE}(on)	Base-Emitter ON Voltage	V_{CE} = 2V, I_C = 0.5A			1	V

h_{FE} Classification

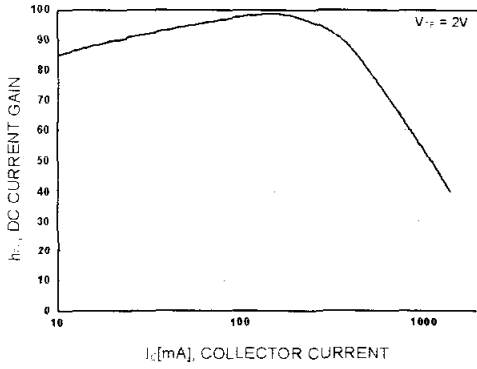| Classification	6	10	16
h_{FE3}	40 ~ 100	63 ~ 160	100 ~ 250

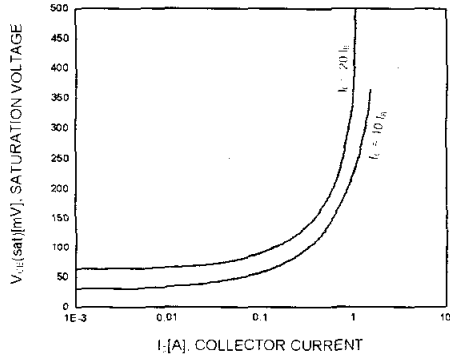# Typical Characteristics

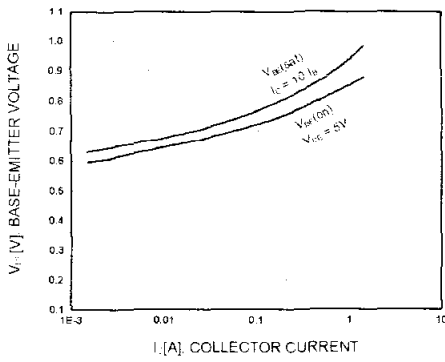Figure 1. DC current Gain

Figure 2. Collector-Emitter Saturation Voltage

Figure 3. Base-Emitter Voltage
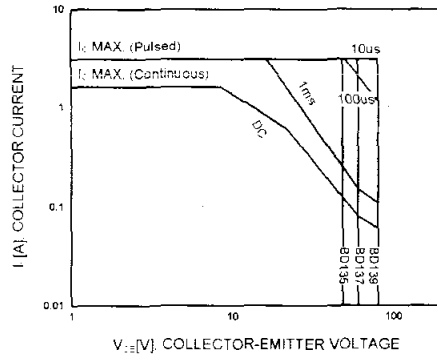
Figure 4. Safe Operating Area
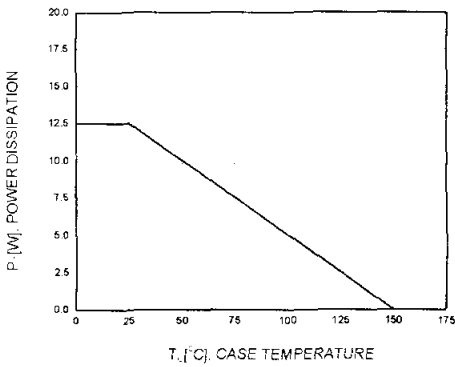
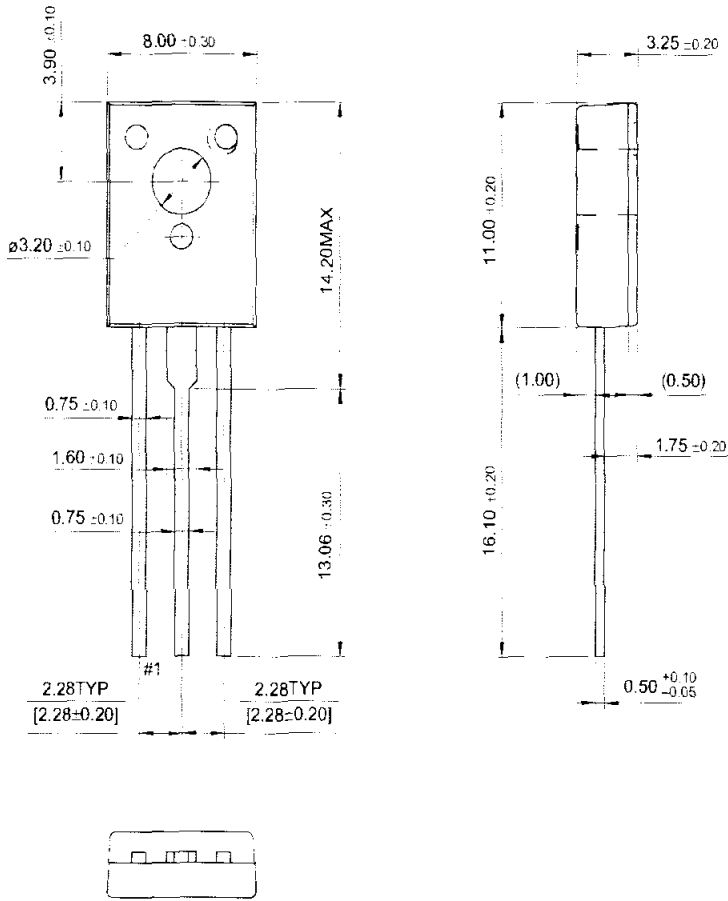Figure 5. Power Derating

Package Demensions

TO-126

3.90 ± 0.10

8.00 ± 0.30

3.25 ± 0.20

$\emptyset 3.20 \pm 0.10$

$14.20MAX$

11.00 ± 0.20

0.75 ± 0.10

1.60 ± 0.10

0.75 ± 0.10

13.06 ± 0.30

(1.00)

(0.50)

1.75 ± 0.20

16.10 ± 0.20

#1

$2.28TYP$
$[2.28 \pm 0.20]$

$2.28TYP$
$[2.28 \pm 0.20]$

$0.50 \,^{+0.10}_{-0.05}$

Dimensions in Millimeters

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FASTr™	SuperSOT™-3	
GTO™	SuperSOT™-6	

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