PETUNJUK PEMAKAIAN ALAT

- Galon diisi hingga batas petunjuk air yang ada disamping galon.
- Hidupkan Kompresor hingga kompresor mati sendiri.
- Hubungkan kabel dari catu daya pada sumber tegangan AC 220 Volt .
- Tekan tombol *Reset* pada rangkaian ***minimum system*** mikrokontroler.
- Letakkan botol diantara sensor infra merah pertama (S1) yang ada disamping kanan dan kiri konveyer.
- Jika petunjuk air yang ada disamping galon sudah menghalangi sensor air, maka akan terjadi pe-non aktif-an proses kerja mikrokontroler. Maka alat akan berhenti.
- Jika akan melakukan proses pengisian lagi, maka Lepaskan hubungan kabel catu daya dari sumbernya.
- Buang isi udara yang ada dalam galon lewat saluran pembuangan udara yang ada diatas galon, dan air yang ada dalam galon lewat kran pembuangan air yang ada dibawah galon.
- Lakukan proses mulai dari awal.

Catatan :

Jika terjadi kemacetan pengoperasian alat maka tekan tombol **RESET**

Kemudian lakukan petunjuk pemakaian mulai dari point ke-4.

SELAMAT MENCOBA

TERIMA KASIH

```
P2.0;       Sensor Awal
P2.1;       Sensor Pengisian
P2.2;       Sensor Akhir
P2.3;       Sensor Pendeteksi Air
P3.0;       Driver Motor DC
P3.1;       Driver Solenoid

$INCLUDE(REG51.INC)
            ORG 00H
            AJMP INISIAL
            ORG 50H
DELAY1:     MOV R7,#50
DD2:        MOV R6,#0FFH
DD1:        MOV R5,#0FFH
            DJNZ R5,$
            DJNZ R6,DD1
            DJNZ R7,DD2
            RET
DELAY2:     MOV R7,#10
DD4:        MOV R6,#0FFH
DD3:        MOV R5,#0FFH
            DJNZ R5,$
            DJNZ R6,DD3
            DJNZ R7,DD4
            RET
INISIAL:
            MOV SP,#60H
            MOV IE,#00H
            CLR P3.0
            SETB P3.1
            MOV P2,#0FFH
```

```
START:
        JNB P2.0,$
KONVEYER:
        SETB P3.0
CEK1:
        JNB P2.1,$
ISI:
        CLR P3.0
        CLR P3.1
ULANG:
        ACALL DELAY1
        JB P2.3,GAMEOVER
        SETB P3.1
JALAN:
        SETB P3.0
        JNB P2.2,$
BERHENTI:
        SETB P3.0
        AJMP START
GAMEOVER:
        AJMP $

END
```

eatures

- Compatible with MCS-51™ Products
- 4K Bytes of In-System Reprogrammable Flash Memory
  - Endurance: 1,000 Write/Erase Cycles
- Fully Static Operation: 0 Hz to 24 MHz
- Three-Level Program Memory Lock
- 128 x 8-Bit Internal RAM
- 32 Programmable I/O Lines
- Two 16-Bit Timer/Counters
- Six Interrupt Sources
- Programmable Serial Channel
- Low Power Idle and Power Down Modes

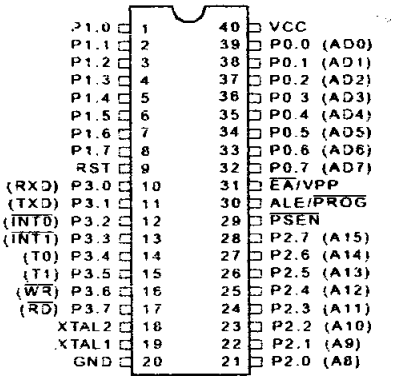
escription

he AT89C51 is a low-power, high-performance CMOS 8-bit microcomputer with 4K ytes of Flash Programmable and Erasable Read Only Memory (PEROM). The evice is manufactured using Atmel's high density nonvolatile memory technology nd is compatible with the industry standard MCS-51™ instruction set and pinout. The n-chip Flash allows the program memory to be reprogrammed in-system or by a conntional nonvolatile memory programmer. By combining a versatile 8-bit CPU with ash on a monolithic chip, the Atmel AT89C51 is a powerful microcomputer which ovides a highly flexible and cost effective solution to many embedded control applitions.

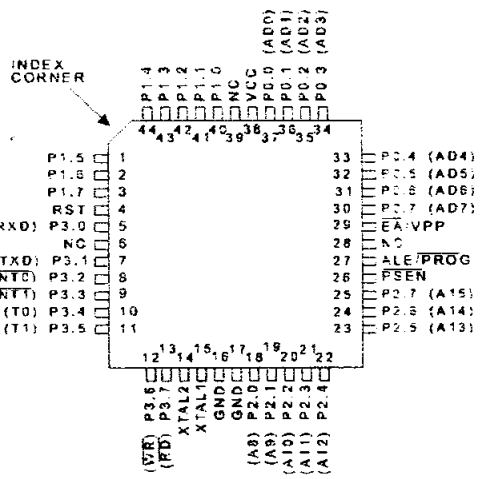
(continued)

in Configurations

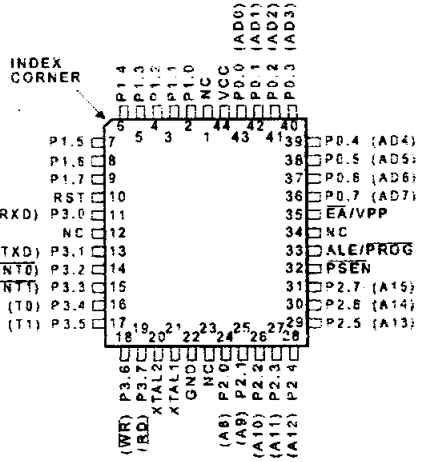
PDIP



PQFP/TQFP



PLCC

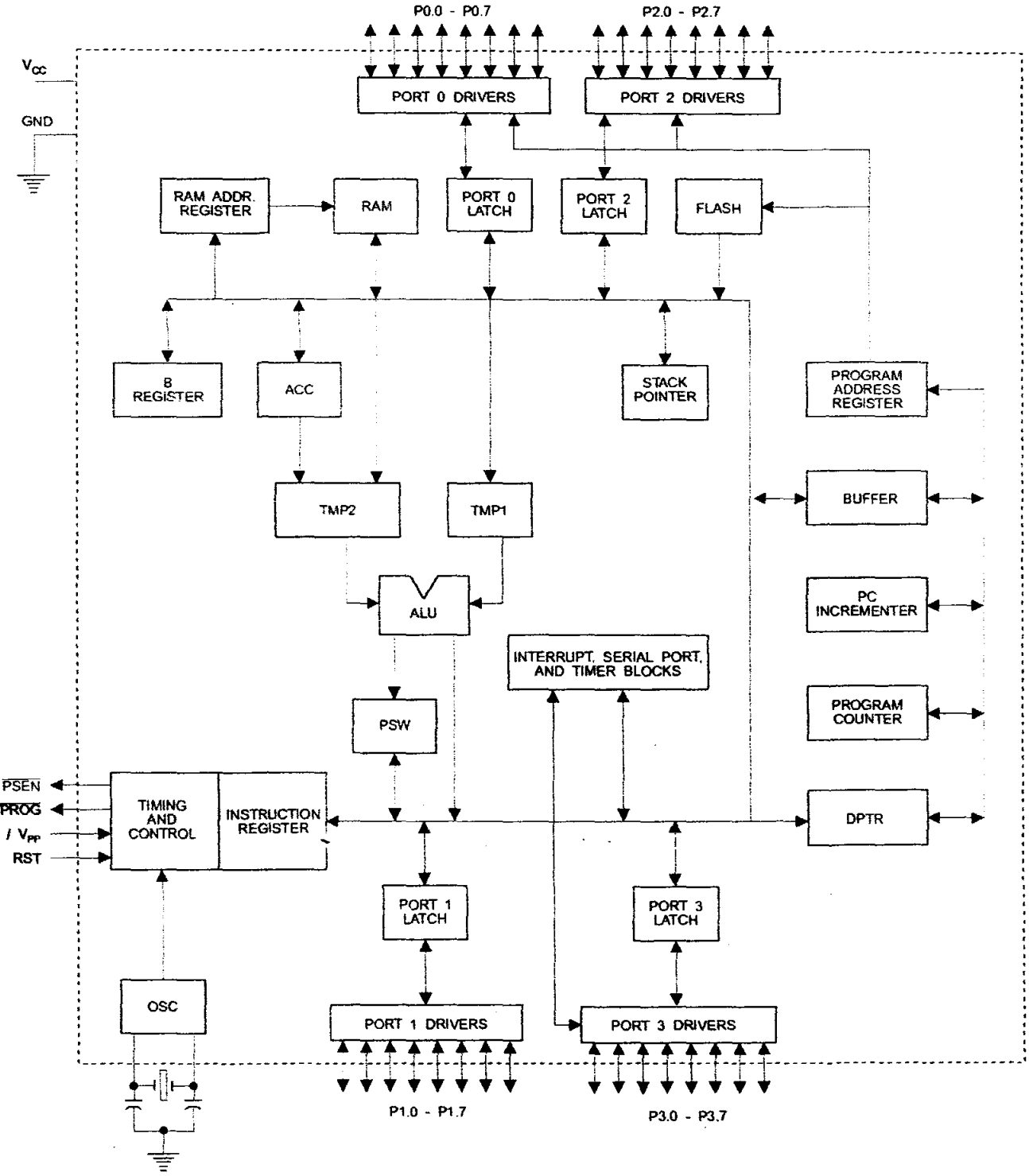


8-Bit Microcontroller with 4K Bytes Flash

AT89C51

0265F-A-12/97

: Diagram


P0.0 - P0.7
P2.0 - P2.7
V_{CC}
GND
PORT 0 DRIVERS
PORT 2 DRIVERS
RAM ADDR. REGISTER
RAM
PORT 0 LATCH
PORT 2 LATCH
FLASH
B REGISTER
ACC
STACK POINTER
PROGRAM ADDRESS REGISTER
TMP2
TMP1
BUFFER
ALU
PC INCREMENTER
INTERRUPT, SERIAL PORT, AND TIMER BLOCKS
PSW
PROGRAM COUNTER
PSEN
PROG
/ V_{PP}
RST
TIMING AND CONTROL
INSTRUCTION REGISTER
DPTR
PORT 1 LATCH
PORT 3 LATCH
OSC
PORT 1 DRIVERS
PORT 3 DRIVERS
P1.0 - P1.7
P3.0 - P3.7

AT89C51 provides the following standard features: 4K
s of Flash, 128 bytes of RAM, 32 I/O lines, two 16-bit
r/counters, a five vector two-level interrupt architecture,
ll duplex serial port, on-chip oscillator and clock cir-
y. In addition, the AT89C51 is designed with static logic
operation down to zero frequency and supports two
ware selectable power saving modes. The Idle Mode
s the CPU while allowing the RAM, timer/counters,
al port and interrupt system to continue functioning. The
ver Down Mode saves the RAM contents but freezes
oscillator disabling all other chip functions until the next
dware reset.

n Description

ply voltage.

D
und.

t 0
t 0 is an 8-bit open drain bidirectional I/O port. As an
out port each pin can sink eight TTL inputs. When 1s
written to port 0 pins, the pins can be used as high-
edance inputs.

t 0 may also be configured to be the multiplexed low-
er address/data bus during accesses to external pro-
m and data memory. In this mode P0 has internal pul-
s.

t 0 also receives the code bytes during Flash program-
g, and outputs the code bytes during program verifica-
. External pullups are required during program verifica-
.

t 1
t 1 is an 8-bit bidirectional I/O port with internal pullups.
Port 1 output buffers can sink/source four TTL inputs.
en 1s are written to Port 1 pins they are pulled high by
internal pullups and can be used as inputs. As inputs,
t 1 pins that are externally being pulled low will source
rent (I_{IL}) because of the internal pullups.

t 1 also receives the low-order address bytes during
sh programming and verification.

t 2
t 2 is an 8-bit bidirectional I/O port with internal pullups.
Port 2 output buffers can sink/source four TTL inputs.
en 1s are written to Port 2 pins they are pulled high by
internal pullups and can be used as inputs. As inputs,
t 2 pins that are externally being pulled low will source
rent (I_{IL}) because of the internal pullups.

t 2 emits the high-order address byte during fetches
m external program memory and during accesses to
ernal data memory that use 16-bit addresses (MOVX @
TR). In this application it uses strong internal pullups
when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

Port 3

Port 3 is an 8-bit bidirectional I/O port with internal pullups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}) because of the pullups.

Port 3 also serves the functions of various special features of the AT89C51 as listed below:

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

Port 3 also receives some control signals for Flash programming and verification.

RST

Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device.

ALE/$\overline{PROG}$

Address Latch Enable output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input ($\overline{PROG}$) during Flash programming.

In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external Data Memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

$\overline{PSEN}$

Program Store Enable is the read strobe to external program memory.

en the AT89C51 is executing code from external pro-
m memory, $\overline{PSEN}$ is activated twice each machine
le, except that two $\overline{PSEN}$ activations are skipped during
:h access to external data memory.

/V_{PP}

ernal Access Enable. $\overline{EA}$ must be strapped to GND in
er to enable the device to fetch code from external pro-
m memory locations starting at 0000H up to FFFFH.
:e, however, that if lock bit 1 is programmed, $\overline{EA}$ will be
ımally latched on reset.

should be strapped to V_{CC} for internal program execu-
ıs.

s pin also receives the 12-volt programming enable volt-
e (V_{PP}) during Flash programming, for parts that require
volt V_{PP}.

AL1

ut to the inverting oscillator amplifier and input to the
ernal clock operating circuit.

AL2

tput from the inverting oscillator amplifier.

scillator Characteristics

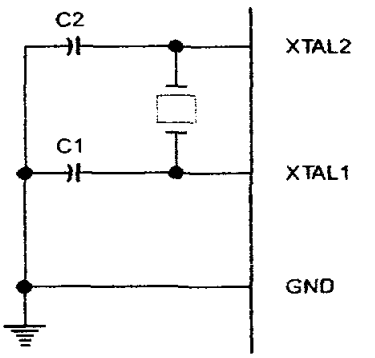
AL1 and XTAL2 are the input and output, respectively,
an inverting amplifier which can be configured for use as
on-chip oscillator, as shown in Figure 1. Either a quartz
stal or ceramic resonator may be used. To drive the
vice from an external clock source, XTAL2 should be left
connected while XTAL1 is driven as shown in Figure 2.
ere are no requirements on the duty cycle of the external
ck signal, since the input to the internal clocking circuitry
hrough a divide-by-two flip-flop, but minimum and maxi-
m voltage high and low time specifications must be
served.

le Mode

dle mode, the CPU puts itself to sleep while all the on-
p peripherals remain active. The mode is invoked by
tware. The content of the on-chip RAM and all the spe-
l functions registers remain unchanged during this
de. The idle mode can be terminated by any enabled
errupt or by a hardware reset.

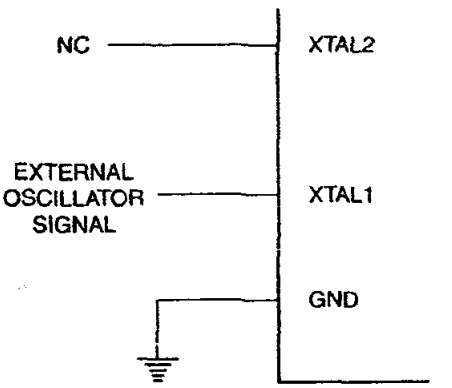
It should be noted that when idle is terminated by a hard ware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.

Figure 1. Oscillator Connections



Note: C1, C2 = 30 pF ± 10 pF for Crystals
= 40 pF ± 10 pF for Ceramic Resonators

Figure 2. External Clock Drive Configuration



tatus of External Pins During Idle and Power Down Modes

ode	Program Memory	ALE	$\overline{PSEN}$	PORT0	PORT1	PORT2	PORT3
le	Internal	1	1	Data	Data	Data	Data
le	External	1	1	Float	Data	Address	Data
ower Down	Internal	0	0	Data	Data	Data	Data
ower Down	External	0	0	Float	Data	Data	Data

wer Down Mode

ne power down mode the oscillator is stopped, and the ruction that invokes power down is the last instruction cuted. The on-chip RAM and Special Function Regis- retain their values until the power down mode is termi- d. The only exit from power down is a hardware reset. et redefines the SFRs but does not change the on-chip M. The reset should not be activated before V_{CC} is ored to its normal operating level and must be held ve long enough to allow the oscillator to restart and sta- e.

Program Memory Lock Bits

On the chip are three lock bits which can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in the table below:

When lock bit 1 is programmed, the logic level at the $\overline{EA}$ pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value, and holds that value until reset is activated. It is necessary that the latched value of $\overline{EA}$ be in agreement with the current logic level at that pin in order for the device to function properly.

ck Bit Protection Modes

Program Lock Bits				Protection Type
	LB1	LB2	LB3	
1	U	U	U	No program lock features.
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, $\overline{EA}$ is sampled and latched on reset, and further programming of the Flash is disabled.
3	P	P	U	Same as mode 2, also verify is disabled.
4	P	P	P	Same as mode 3, also external execution is disabled.

ogramming the Flash

AT89C51 is normally shipped with the on-chip Flash mory array in the erased state (that is, contents = FFH) ready to be programmed. The programming interface epts either a high-voltage (12-volt) or a low-voltage C) program enable signal. The low voltage program- g mode provides a convenient way to program the 9C51 inside the user's system, while the high-voltage gramming mode is compatible with conventional third y Flash or EPROM programmers.

AT89C51 is shipped with either the high-voltage or -voltage programming mode enabled. The respective -side marking and device signature codes are listed in following table.

	V_{PP} = 12V	V_{PP} = 5V
p-Side Mark	AT89C51 xxxx yyww	AT89C51 xxxx-5 yyww
gnature	(030H)=1EH (031H)=51H (032H)=FFH	(030H)=1EH (031H)=51H (032H)=05H

AT89C51 code memory array is programmed byte-by- e in either programming mode. *To program any non- nk byte in the on-chip Flash Memory, the entire memory st be erased using the Chip Erase Mode.*

Programming Algorithm: Before programming the AT89C51, the address, data and control signals should be set up according to the Flash programming mode table and Figures 3 and 4. To program the AT89C51, take the following steps.

1. Input the desired memory location on the address lines.
2. Input the appropriate data byte on the data lines.
3. Activate the correct combination of control signals.
4. Raise $\overline{EA}/V_{PP}$ to 12V for the high-voltage programming mode.
5. Pulse ALE/$\overline{PROG}$ once to program a byte in the Flash array or the lock bits. The byte-write cycle is self-timed and typically takes no more than 1.5 ms. Repeat steps 1 through 5, changing the address and data for the entire array or until the end of the object file is reached.

$\overline{Data}$ Polling: The AT89C51 features $\overline{Data}$ Polling to indicate the end of a write cycle. During a write cycle, an attempted read of the last byte written will result in the complement of the written datum on PO.7. Once the write cycle has been completed, true data are valid on all outputs, and the next cycle may begin. $\overline{Data}$ Polling may begin any time after a write cycle has been initiated.

Ready/$\overline{Busy}$: The progress of byte programming can also be monitored by the RDY/$\overline{BSY}$ output signal. P3.4 is pulled low after ALE goes high during programming to indicate BUSY. P3.4 is pulled high again when programming is done to indicate READY.

gram Verify: If lock bits LB1 and LB2 have not been ırammed, the programmed code data can be read back he address and data lines for verification. The lock bits not be verified directly. Verification of the lock bits is ieved by observing that their features are enabled.

p Erase: The entire Flash array is erased electrically ısing the proper combination of control signals and by ling ALE/$\overline{PROG}$ low for 10 ms. The code array is written all "1"s. The chip erase operation must be executed re the code memory can be re-programmed.

ıding the Signature Bytes: The signature bytes are 1 by the same procedure as a normal verification of tions 030H,

H, and 032H, except that P3.6 and P3.7 must be pulled logic low. The values returned are as follows.

(030H) = 1EH indicates manufactured by Atmel
(031H) = 51H indicates 89C51
(032H) = FFH indicates 12V programming
(032H) = 05H indicates 5V programming

Programming Interface

Every code byte in the Flash array can be written and the entire array can be erased by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

All major programming vendors offer worldwide support for the Atmel microcontroller series. Please contact your local programming vendor for the appropriate software revision.

Flash Programming Modes

ode		RST	$\overline{PSEN}$	ALE/$\overline{PROG}$	$\overline{EA}$/V_{PP}	P2.6	P2.7	P3.6	P3.7
ite Code Data		H	L		H/12V	L	H	H	H
ad Code Data		H	L	H	H	L	L	H	H
ite Lock	Bit - 1	H	L		H/12V	H	H	H	H
	Bit - 2	H	L		H/12V	H	H	L	L
	Bit - 3	H	L		H/12V	H	L	H	L
ip Erase		H	L	(1)	H/12V	H	L	L	L
ad Signature Byte		H	L	H	H	L	L	L	L

e: 1. Chip Erase requires a 10-ms PROG pulse.

ure 3. Programming the Flash

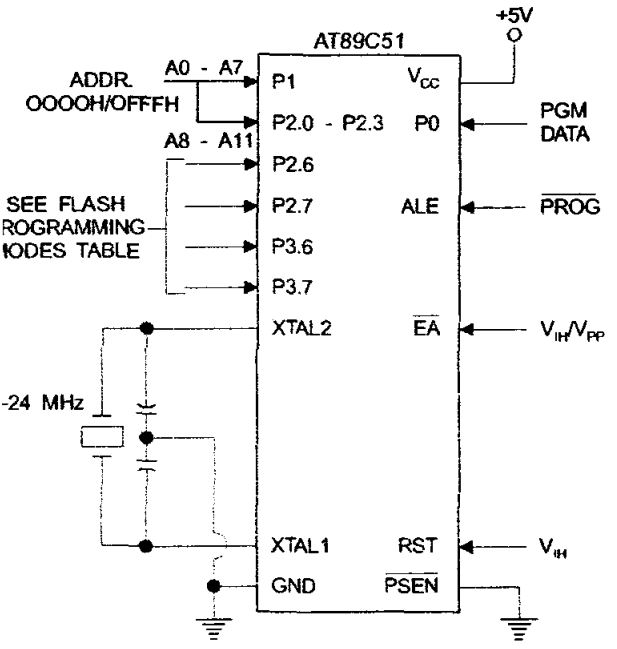
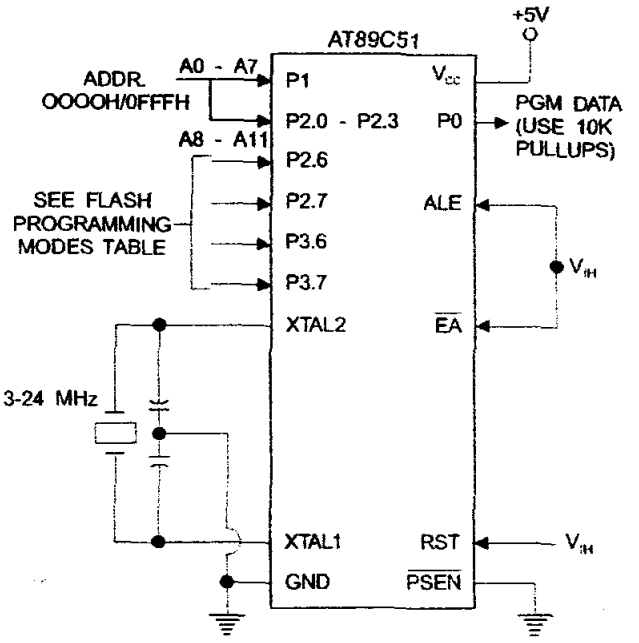


Figure 4. Verifying the Flash



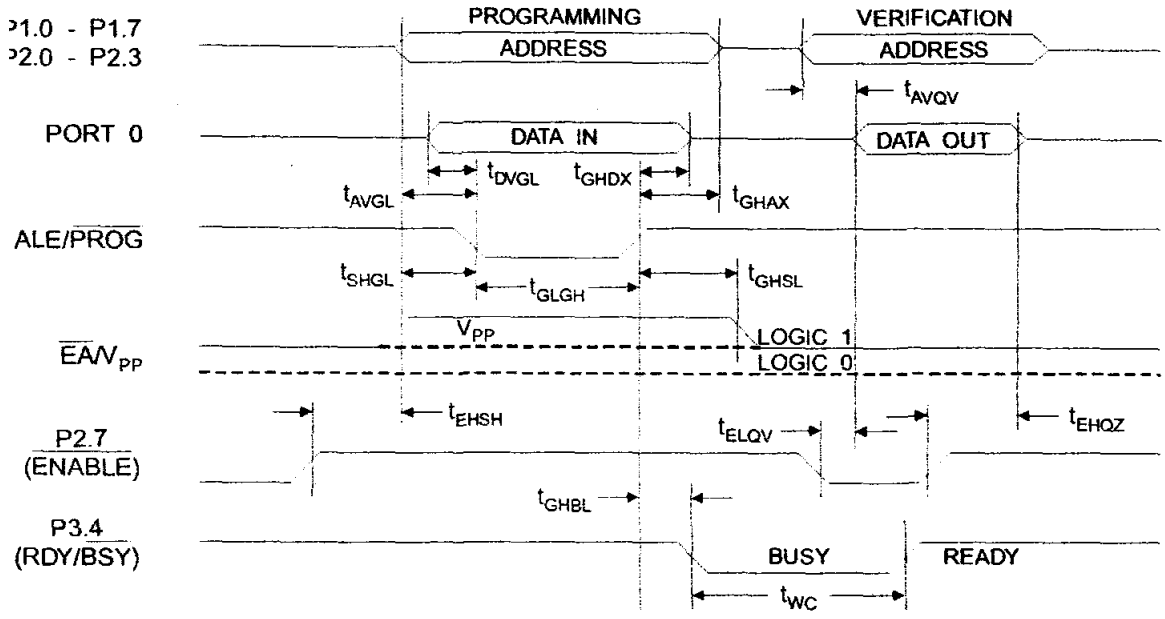
ash Programming and Verification Characteristics

= 0°C to 70°C, V_{CC} = 5.0 ± 10%

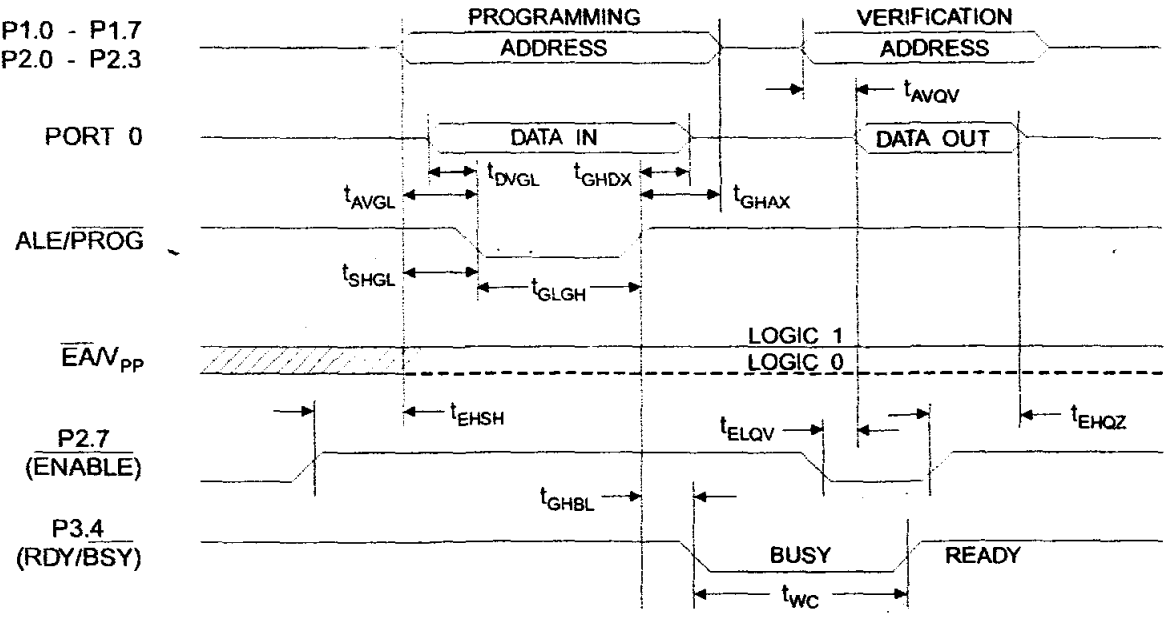
ymbol	Parameter	Min	Max	Units
$_{PP}$[1]	Programming Enable Voltage	11.5	12.5	V
$_{P}$[1]	Programming Enable Current		1.0	mA
t_{CLCL}	Oscillator Frequency	3	24	MHz
VGL	Address Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
HAX	Address Hold After $\overline{PROG}$	$48t_{CLCL}$		
VGL	Data Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
HDX	Data Hold After $\overline{PROG}$	$48t_{CLCL}$		
HSH	P2.7 ($\overline{ENABLE}$) High to V_{PP}	$48t_{CLCL}$		
HGL	V_{PP} Setup to $\overline{PROG}$ Low	10		µs
HSL[1]	V_{PP} Hold After $\overline{PROG}$	10		µs
LGH	$\overline{PROG}$ Width	1	110	µs
VQV	Address to Data Valid		$48t_{CLCL}$	
LQV	$\overline{ENABLE}$ Low to Data Valid		$48t_{CLCL}$	
HQZ	Data Float After $\overline{ENABLE}$	0	$48t_{CLCL}$	
HBL	$\overline{PROG}$ High to $\overline{BUSY}$ Low		1.0	µs
WC	Byte Write Cycle Time		2.0	ms

te: 1. Only used in 12-volt programming mode.

sh Programming and Verification Waveforms - High Voltage Mode (V_{PP} = 12V)



sh Programming and Verification Waveforms - Low Voltage Mode (V_{PP} = 5V)



solute Maximum Ratings*

erating Temperature	-55°C to +125°C
rage Temperature	-65°C to +150°C
tage on Any Pin h Respect to Ground	-1.0V to +7.0V
ximum Operating Voltage	6.6V
Output Current	15.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Characteristics

-40°C to 85°C, V_{CC} = 5.0V ± 20% (unless otherwise noted)

nbol	Parameter	Condition	Min	Max	Units
	Input Low Voltage	(Except $\overline{EA}$)	-0.5	0.2 V_{CC} - 0.1	V
1	Input Low Voltage ($\overline{EA}$)		-0.5	0.2 V_{CC} - 0.3	V
	Input High Voltage	(Except XTAL1, RST)	0.2 V_{CC} + 0.9	V_{CC} + 0.5	V
H1	Input High Voltage	(XTAL1, RST)	0.7 V_{CC}	V_{CC} + 0.5	V
	Output Low Voltage(1) (Ports 1,2,3)	I_{OL} = 1.6 mA		0.45	V
L1	Output Low Voltage(1) (Port 0, ALE, $\overline{PSEN}$)	I_{OL} = 3.2 mA		0.45	V
H	Output High Voltage (Ports 1,2,3, ALE, $\overline{PSEN}$)	I_{OH} = -60 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -25 µA	0.75 V_{CC}		V
		I_{OH} = -10 µA	0.9 V_{CC}		V
H1	Output High Voltage (Port 0 in External Bus Mode)	I_{OH} = -800 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -300 µA	0.75 V_{CC}		V
		I_{OH} = -80 µA	0.9 V_{CC}		V
	Logical 0 Input Current (Ports 1,2,3)	V_{IN} = 0.45V		-50	µA
	Logical 1 to 0 Transition Current (Ports 1,2,3)	V_{IN} = 2V, VCC = 5V ± 10%		-650	µA
	Input Leakage Current (Port 0, $\overline{EA}$)	0.45 < V_{IN} < V_{CC}		±10	µA
ST	Reset Pulldown Resistor		50	300	KΩ
	Pin Capacitance	Test Freq. = 1 MHz, T_A = 25°C		10	pF
	Power Supply Current	Active Mode, 12 MHz		20	mA
		Idle Mode, 12 MHz		5	mA
	Power Down Mode(2)	V_{CC} = 6V		100	µA
		V_{CC} = 3V		40	µA

es:
1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
   Maximum I_{OL} per port pin: 10 mA
   Maximum I_{OL} per 8-bit port: Port 0: 26 mA
   Ports 1, 2, 3: 15 mA
   Maximum total I_{OL} for all output pins: 71 mA
   If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. Minimum V_{CC} for Power Down is 2V.

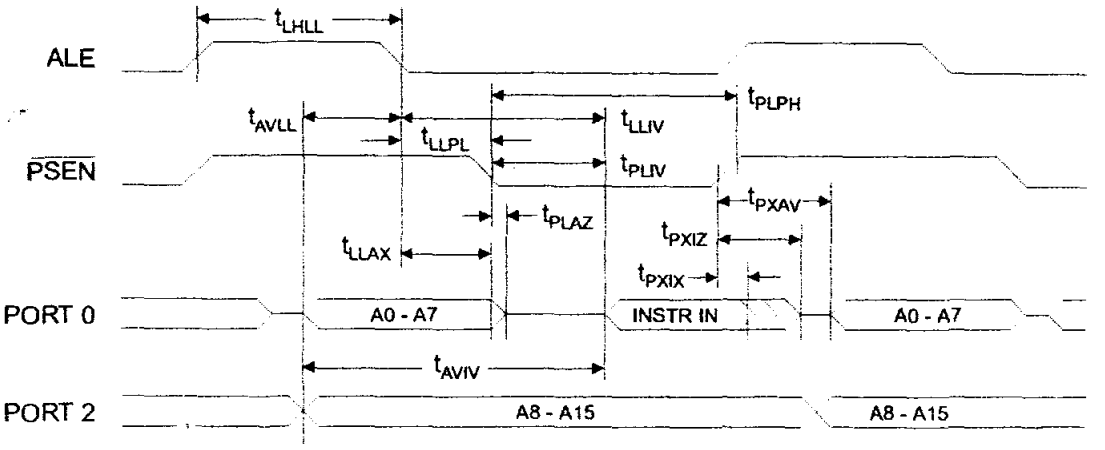
; Characteristics

der Operating Conditions; Load Capacitance for Port 0, ALE/$\overline{PROG}$, and $\overline{PSEN}$ = 100 pF; Load Capacitance for all other puts = 80 pF)

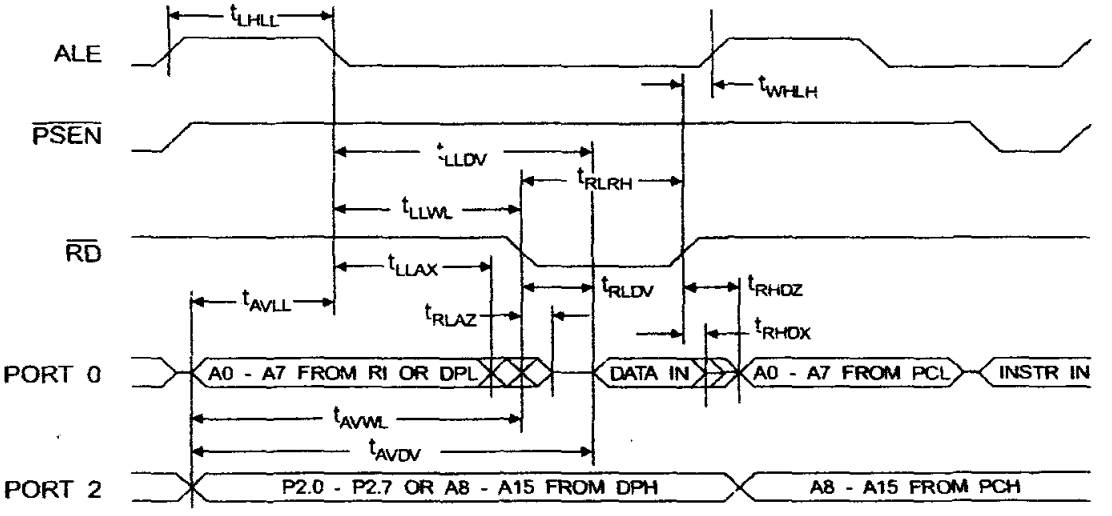
ternal Program and Data Memory Characteristics

mbol	Parameter	12 MHz Oscillator		16 to 24 MHz Oscillator		Units
		Min	Max	Min	Max	
CLCL	Oscillator Frequency			0	24	MHz
LL	ALE Pulse Width	127		$2t_{CLCL}$-40		ns
LL	Address Valid to ALE Low	43		t_{CLCL}-13		ns
AX	Address Hold After ALE Low	48		t_{CLCL}-20		ns
LIV	ALE Low to Valid Instruction In		233		$4t_{CLCL}$-65	ns
LPL	ALE Low to $\overline{PSEN}$ Low	43		t_{CLCL}-13		ns
PLPH	$\overline{PSEN}$ Pulse Width	205		$3t_{CLCL}$-20		ns
PLIV	$\overline{PSEN}$ Low to Valid Instruction In		145		$3t_{CLCL}$-45	ns
PXIX	Input Instruction Hold After $\overline{PSEN}$	0		0		ns
PXIZ	Input Instruction Float After $\overline{PSEN}$		59		t_{CLCL}-10	ns
PXAV	$\overline{PSEN}$ to Address Valid	75		t_{CLCL}-8		ns
AVIV	Address to Valid Instruction In		312		$5t_{CLCL}$-55	ns
PLAZ	$\overline{PSEN}$ Low to Address Float		10		10	ns
RLRH	$\overline{RD}$ Pulse Width	400		$6t_{CLCL}$-100		ns
WLWH	$\overline{WR}$ Pulse Width	400		$6t_{CLCL}$-100		ns
RLDV	$\overline{RD}$ Low to Valid Data In		252		$5t_{CLCL}$-90	ns
RHDX	Data Hold After $\overline{RD}$	0		0		ns
RHDZ	Data Float After $\overline{RD}$		97		$2t_{CLCL}$-28	ns
LLDV	ALE Low to Valid Data In		517		$8t_{CLCL}$-150	ns
AVDV	Address to Valid Data In		585		$9t_{CLCL}$-165	ns
LLWL	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	200	300	$3t_{CLCL}$-50	$3t_{CLCL}$+50	ns
AVWL	Address to $\overline{RD}$ or $\overline{WR}$ Low	203		$4t_{CLCL}$-75		ns
QVWX	Data Valid to $\overline{WR}$ Transition	23		t_{CLCL}-20		ns
QVWH	Data Valid to $\overline{WR}$ High	433		$7t_{CLCL}$-120		ns
WHQX	Data Hold After $\overline{WR}$	33		t_{CLCL}-20		ns
RLAZ	$\overline{RD}$ Low to Address Float		0		0	ns
WHLH	$\overline{RD}$ or $\overline{WR}$ High to ALE High	43	123	t_{CLCL}-20	t_{CLCL}+25	ns

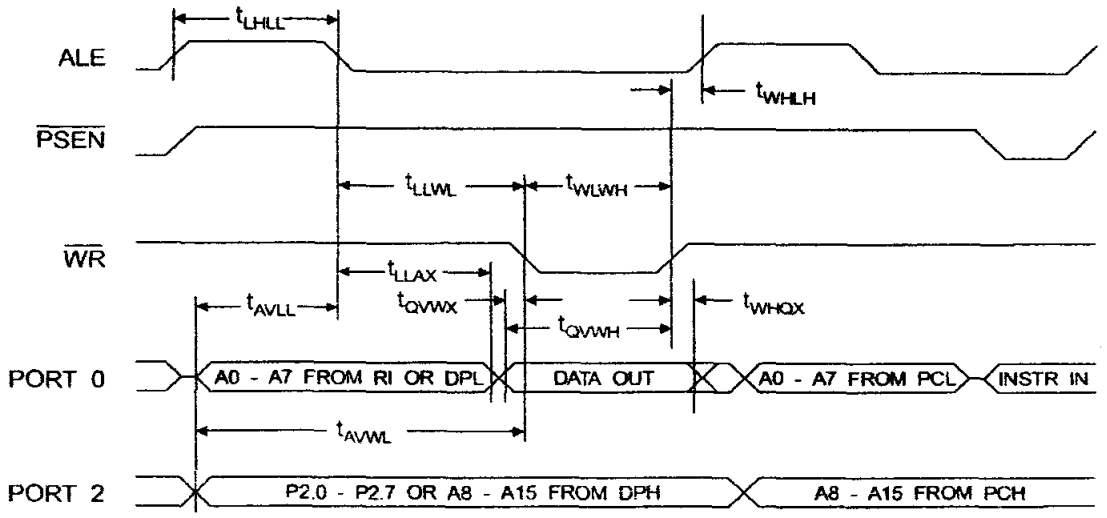
External Program Memory Read Cycle



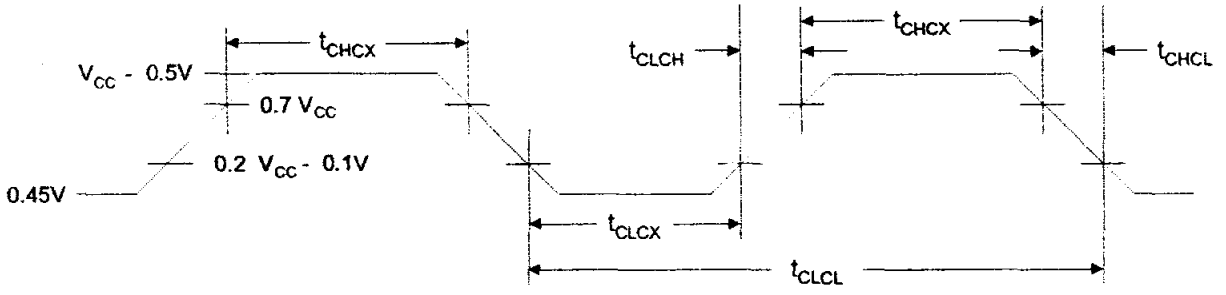
External Data Memory Read Cycle



ternal Data Memory Write Cycle



ternal Clock Drive Waveforms



ternal Clock Drive

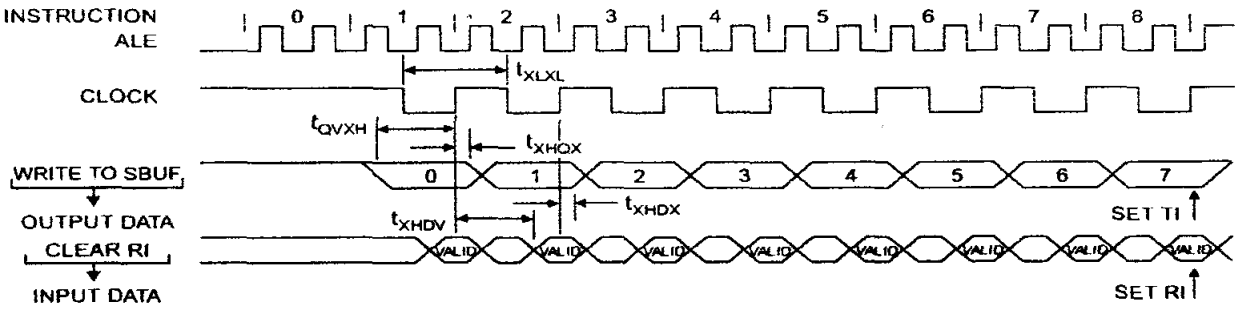
ymbol	Parameter	Min	Max	Units
t_{CLCL}	Oscillator Frequency	0	24	MHz
LCL	Clock Period	41.6		ns
HCX	High Time	15		ns
LCX	Low Time	15		ns
LCH	Rise Time		20	ns
HCL	Fall Time		20	ns

ial Port Timing: Shift Register Mode Test Conditions

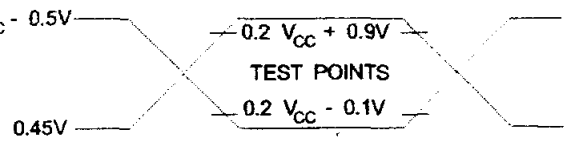
= 5.0 V ± 20%; Load Capacitance = 80 pF)

bol	Parameter	12 MHz Osc		Variable Oscillator		Units
		Min	Max	Min	Max	
_	Serial Port Clock Cycle Time	1.0		$12t_{CLCL}$		µs
H	Output Data Setup to Clock Rising Edge	700		$10t_{CLCL}$-133		ns
X	Output Data Hold After Clock Rising Edge	50		$2t_{CLCL}$-117		ns
X	Input Data Hold After Clock Rising Edge	0		0		ns
V	Clock Rising Edge to Input Data Valid		700		$10t_{CLCL}$-133	ns

ft Register Mode Timing Waveforms

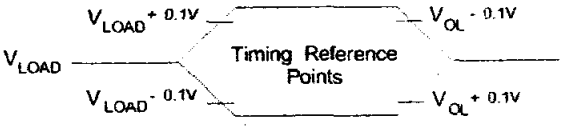


Testing Input/Output Waveforms[1]



1. AC Inputs during testing are driven at V_{CC} - 0.5V for a logic 1 and 0.45V for a logic 0. Timing measurements are made at V_{IH} min. for a logic 1 and V_{IL} max. for a logic 0.

Float Waveforms[1]



Note: 1. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when 100 mV change from the loaded V_{OH}/V_{OL} level occurs.

ering Information

peed Hz)	Power Supply	Ordering Code	Package	Operation Range
12	5V ± 20%	AT89C51-12AC	44A	Commercial
		AT89C51-12JC	44J	(0°C to 70°C)
		AT89C51-12PC	40P6	
		AT89C51-12QC	44Q	
		AT89C51-12AI	44A	Industrial
		AT89C51-12JI	44J	(-40°C to 85°C)
		AT89C51-12PI	40P6	
		AT89C51-12QI	44Q	
		AT89C51-12AA	44A	Automotive
		AT89C51-12JA	44J	(-40°C to 105°C)
		AT89C51-12PA	40P6	
		AT89C51-12QA	44Q	
16	5V ± 20%	AT89C51-16AC	44A	Commercial
		AT89C51-16JC	44J	(0°C to 70°C)
		AT89C51-16PC	40P6	
		AT89C51-16QC	44Q	
		AT89C51-16AI	44A	Industrial
		AT89C51-16JI	44J	(-40°C to 85°C)
		AT89C51-16PI	40P6	
		AT89C51-16QI	44Q	
		AT89C51-16AA	44A	Automotive
		AT89C51-16JA	44J	(-40°C to 105°C)
		AT89C51-16PA	40P6	
		AT89C51-16QA	44Q	
20	5V ± 20%	AT89C51-20AC	44A	Commercial
		AT89C51-20JC	44J	(0°C to 70°C)
		AT89C51-20PC	40P6	
		AT89C51-20QC	44Q	
		AT89C51-20AI	44A	Industrial
		AT89C51-20JI	44J	(-40°C to 85°C)
		AT89C51-20PI	40P6	
		AT89C51-20QI	44Q	

ering Information

peed MHz)	Power Supply	Ordering Code	Package	Operation Range
24	5V ± 20%	AT89C51-24AC	44A	Commercial (0°C to 70°C)
		AT89C51-24JC	44J	
		AT89C51-24PC	44P6	
		AT89C51-24QC	44Q	
		AT89C51-24AI	44A	Industrial (-40°C to 85°C)
		AT89C51-24JI	44J	
		AT89C51-24PI	44P6	
		AT89C51-24QI	44Q	

	Package Type
	44 Lead, Thin Plastic Gull Wing Quad Flatpack (TQFP)
	44 Lead, Plastic J-Leaded Chip Carrier (PLCC)
	40 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
	44 Lead, Plastic Gull Wing Quad Flatpack (PQFP)

GlobalOptoisolator™

VDE | UL | CSA | SETI | SEMKO | DEMKO | NEMKO | BABT

6-Pin DIP Zero-Cross Optoisolators Triac Driver Output (400 Volts Peak)

MOC3041 [IFT = 15 mA Max]
MOC3042 [IFT = 10 mA Max]
MOC3043* [IFT = 5 mA Max]

*Motorola Preferred Device

The MOC3041, MOC3042 and MOC3043 devices consist of gallium arsenide infrared emitting diodes optically coupled to a monolithic silicon detector performing the function of a Zero Voltage Crossing bilateral triac driver.

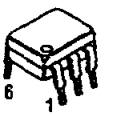
They are designed for use with a triac in the interface of logic systems to equipment powered from 115 Vac lines, such as solid–state relays, industrial controls, motors, solenoids and consumer appliances, etc.

- Simplifies Logic Control of 115 Vac Power
- Zero Voltage Crossing
- dv/dt of 2000 V/µs Typical, 1000 V/µs Guaranteed
- ***To order devices that are tested and marked per VDE 0884 requirements, the suffix "V" must be included at end of part number. VDE 0884 is a test option.***

Recommended for 115/240 Vac(rms) Applications:

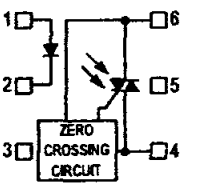
- Solenoid/Valve Controls
- Lighting Controls
- Static Power Switches
- AC Motor Drives
- Temperature Controls
- E.M. Contactors
- AC Motor Starters
- Solid State Relays

STYLE 6 PLASTIC



STANDARD THRU HOLE
CASE 730A–04

COUPLER SCHEMATIC



1. ANODE
2. CATHODE
3. NC
4. MAIN TERMINAL
5. SUBSTRATE
   DO NOT CONNECT
6. MAIN TERMINAL

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
INFRARED EMITTING DIODE			
Reverse Voltage	V_R	6	Volts
Forward Current — Continuous	I_F	60	mA
Total Power Dissipation @ T_A = 25°C Negligible Power in Output Driver Derate above 25°C	P_D	120 1.41	mW mW/°C
OUTPUT DRIVER			
Off–State Output Terminal Voltage	V_{DRM}	400	Volts
Peak Repetitive Surge Current (PW = 100 µs, 120 pps)	I_{TSM}	1	A
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	150 1.76	mW mW/°C
TOTAL DEVICE			
Isolation Surge Voltage(1) (Peak ac Voltage, 60 Hz, 1 Second Duration)	V_{ISO}	7500	Vac(pk)
Total Power Dissipation @ T_A = 25°C Derate above 25°C	P_D	250 2.94	mW mW/°C
Junction Temperature Range	T_J	–40 to +100	°C
Ambient Operating Temperature Range(2)	T_A	–40 to +85	°C
Storage Temperature Range(2)	T_{stg}	–40 to +150	°C
Soldering Temperature (10 s)	T_L	260	°C

1. Isolation surge voltage, V_{ISO}, is an internal device dielectric breakdown rating.
   For this test, Pins 1 and 2 are common, and Pins 4, 5 and 6 are common.
2. Refer to Quality and Reliability Section in Opto Data Book for information on test conditions.

Preferred devices are Motorola recommended choices for future use and best overall value.

GlobalOptoisolator is a trademark of Motorola, Inc.

(Replaces MOC3040/D)

MOTOROLA

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
INPUT LED						
Reverse Leakage Current (V_R = 6 V)		I_R	—	0.05	100	μA
Forward Voltage (I_F = 30 mA)		V_F	—	1.3	1.5	Volts
OUTPUT DETECTOR (I_F = 0 unless otherwise noted)						
Leakage with LED Off, Either Direction (Rated V_{DRM}(1))		I_{DRM1}	—	2	100	nA
Peak On-State Voltage, Either Direction (I_{TM} = 100 mA Peak)		V_{TM}	—	1.8	3	Volts
Critical Rate of Rise of Off-State Voltage(3)		dv/dt	1000	2000	—	V/μs
COUPLED						
LED Trigger Current, Current Required to Latch Output (Main Terminal Voltage = 3 V(2))	MOC3041	I_{FT}	—	—	15	mA
	MOC3042		—	—	10	
	MOC3043		—	—	5	
Holding Current, Either Direction		I_H	—	250	—	μA
Isolation Voltage (f = 60 Hz, t = 1 sec)		V_{ISO}	7500	—	—	Vac(pk)
ZERO CROSSING						
Inhibit Voltage (I_F = Rated I_{FT}, MT1–MT2 Voltage above which device will not trigger.)		V_{IH}	—	5	20	Volts
Leakage in Inhibited State (I_F = Rated I_{FT}, Rated V_{DRM}, Off State)		I_{DRM2}	—	—	500	μA

1. Test voltage must be applied within dv/dt rating.
2. All devices are guaranteed to trigger at an I_F value less than or equal to max I_{FT}. Therefore, recommended operating I_F lies between I_{FT} (15 mA for MOC3041, 10 mA for MOC3042, 5 mA for MOC3043) and absolute max I_F (60 mA).
3. This is static dv/dt. See Figure 7 for test circuit. Commutating dv/dt is a function of the load-driving thyristor(s) only.

TYPICAL ELECTRICAL CHARACTERISTICS

T_A = 25°C

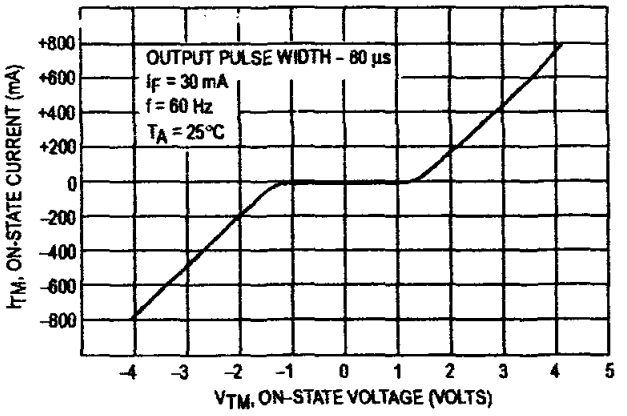


Figure 1. On-State Characteristics

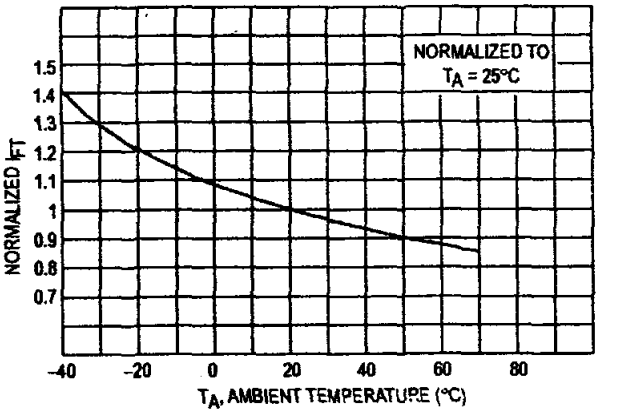


Figure 2. Trigger Current versus Temperature

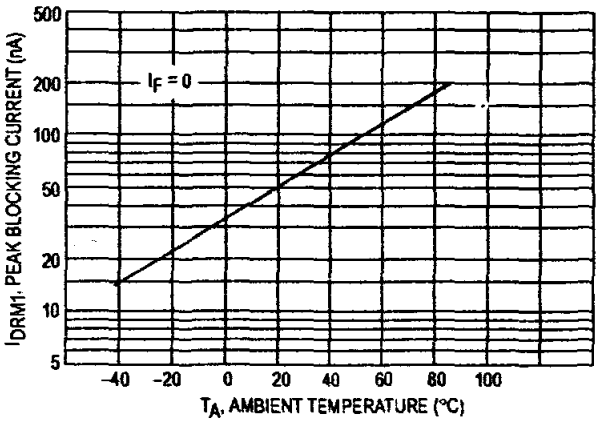


Figure 3. I_{DRM1}, Peak Blocking Current versus Temperature

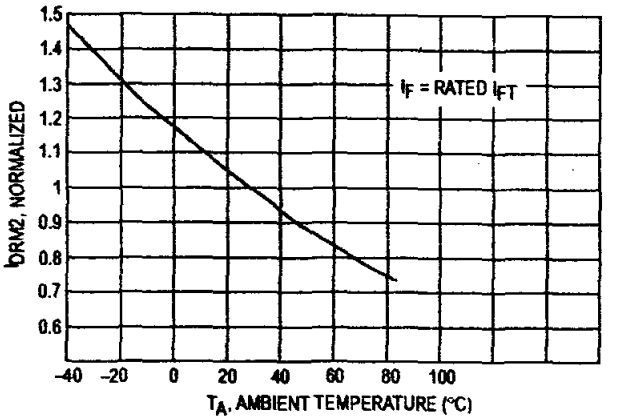


Figure 4. I_{DRM2}, Leakage in Inhibit State versus Temperature

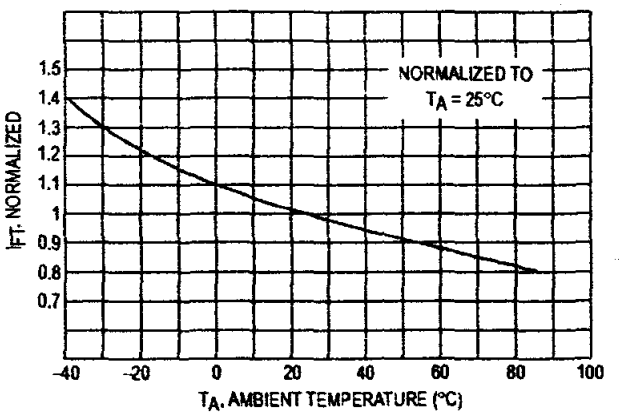


Figure 5. Trigger Current versus Temperature

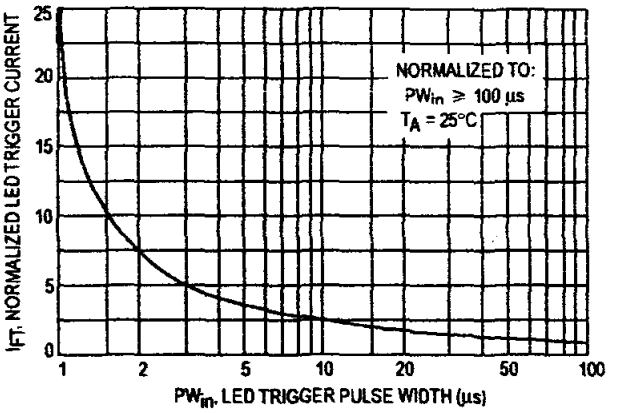
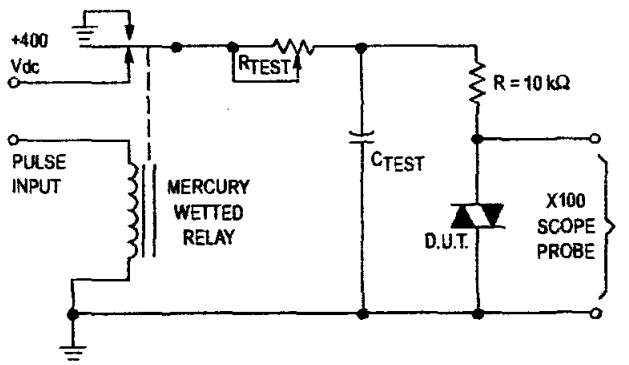


Figure 6. LED Current Required to Trigger versus LED Pulse Width



1. The mercury wetted relay provides a high speed repeated pulse to the D.U.T.
2. 100x scope probes are used, to allow high speeds and voltages.
3. The worst-case condition for static dv/dt is established by triggering the D.U.T. with a normal LED input current, then removing the current. The variable R_{TEST} allows the dv/dt to be gradually increased until the D.U.T. continues to trigger in response to the applied voltage pulse, even after the LED current has been removed. The dv/dt is then decreased until the D.U.T. stops triggering. τ_{RC} is measured at this point and recorded.

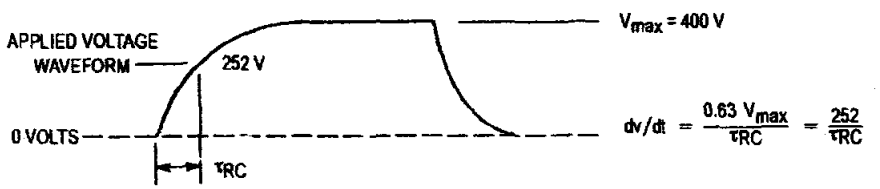
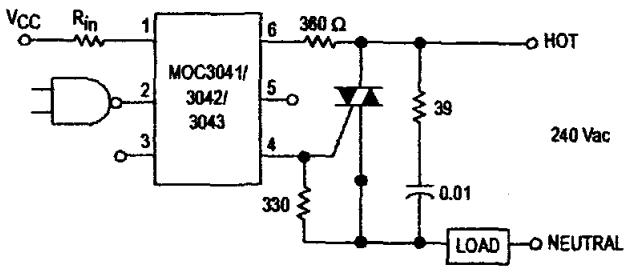


Figure 7. Static dv/dt Test Circuit

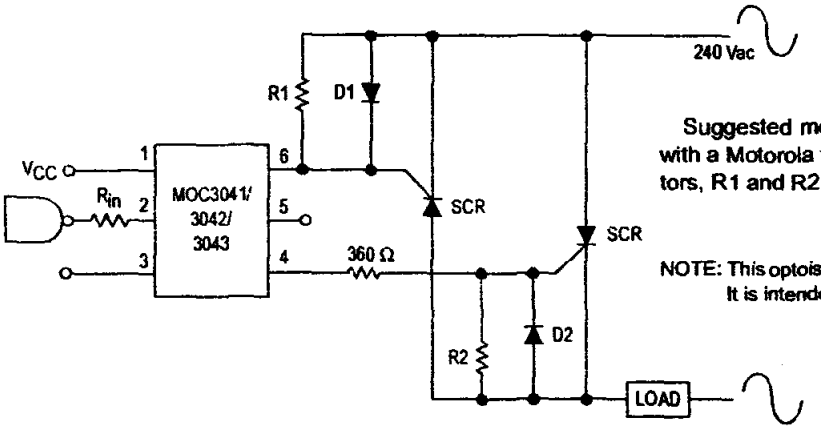


* For highly inductive loads (power factor < 0.5), change this value to 360 ohms.

Typical circuit for use when hot line switching is required. In this circuit the "hot" side of the line is switched and the load connected to the cold or neutral side. The load may be connected to either the neutral or hot line.

R_{in} is calculated so that I_F is equal to the rated I_{FT} of the part, 5 mA for the MOC3043, 10 mA for the MOC3042, or 15 mA for the MOC3041. The 39 ohm resistor and 0.01 μF capacitor are for snubbing of the triac and may or may not be necessary depending upon the particular triac and load used.

Figure 8. Hot–Line Switching Application Circuit

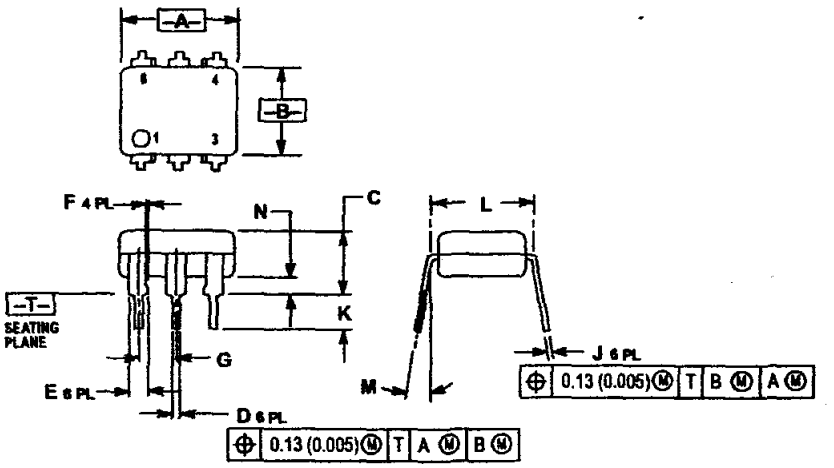


Suggested method of firing two, back–to–back SCR's, with a Motorola triac driver. Diodes can be 1N4001; resistors, R1 and R2, are optional 330 ohms.

NOTE: This optoisolator should not be used to drive a load directly. It is intended to be a trigger device only.

Figure 9. Inverse–Parallel SCR Driver Circuit

PACKAGE DIMENSIONS

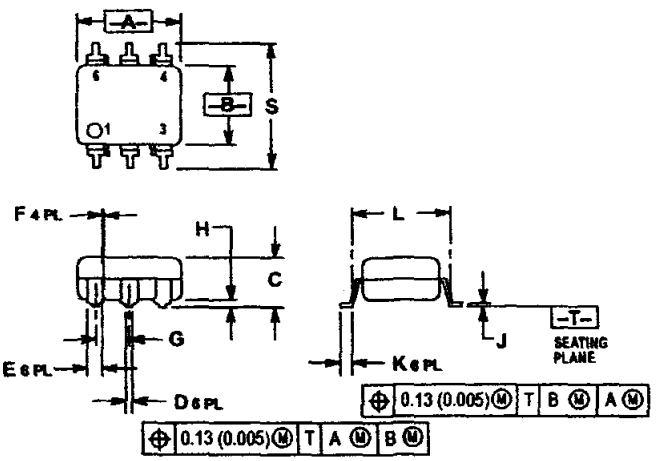


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.320	0.350	8.13	8.89
B	0.240	0.260	6.10	6.60
C	0.115	0.200	2.93	5.08
D	0.016	0.020	0.41	0.50
E	0.040	0.070	1.02	1.77
F	0.010	0.014	0.25	0.36
G	0.100 BSC		2.54 BSC	
J	0.008	0.012	0.21	0.30
K	0.100	0.150	2.54	3.81
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.015	0.100	0.38	2.54

STYLE 6:
PIN 1. ANODE
2. CATHODE
3. NC
4. MAIN TERMINAL
5. SUBSTRATE
6. MAIN TERMINAL

CASE 730A–04
ISSUE G

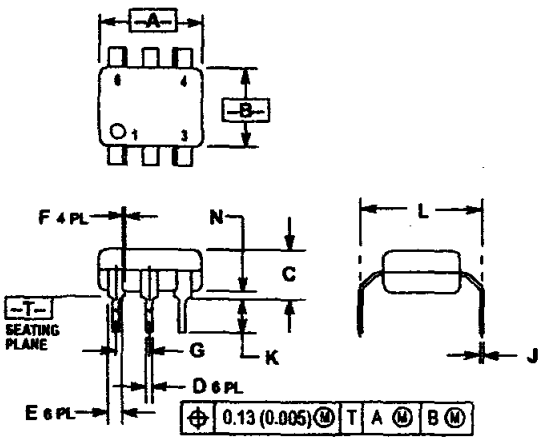


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.320	0.350	8.13	8.89
B	0.240	0.260	6.10	6.60
C	0.115	0.200	2.93	5.08
D	0.016	0.020	0.41	0.50
E	0.040	0.070	1.02	1.77
F	0.010	0.014	0.25	0.36
G	0.100 BSC		2.54 BSC	
H	0.020	0.025	0.51	0.63
J	0.008	0.012	0.20	0.30
K	0.006	0.035	0.16	0.88
L	0.320 BSC		8.13 BSC	
S	0.332	0.390	8.43	9.90

***Consult factory for leadform option availability**

CASE 730C–04
ISSUE D



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.320	0.350	8.13	8.89
B	0.240	0.260	6.10	6.60
C	0.115	0.200	2.93	5.08
D	0.016	0.020	0.41	0.50
E	0.040	0.070	1.02	1.77
F	0.010	0.014	0.25	0.36
G	0.100 BSC		2.54 BSC	
J	0.008	0.012	0.21	0.30
K	0.100	0.150	2.54	3.81
L	0.400	0.425	10.16	10.80
N	0.015	0.040	0.38	1.02

***Consult factory for leadform option availability**

CASE 730D–05
ISSUE D

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6F Seibu–Butsuryu–Center, 3–14–2 Tatsumi Koto–Ku, Tokyo 135, Japan. 03–3521–8315

HONG KONG: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,
51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852–26629298

Triacs sensitive gate

BT136 series E

GENERAL DESCRIPTION

Passivated, sensitive gate triacs in a plastic envelope, intended for use in general purpose bidirectional switching and phase control applications, where high sensitivity is required in all four quadrants.

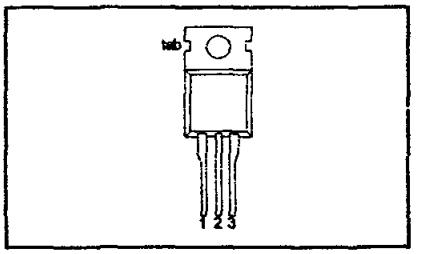
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	UNIT
	BT136-	600E	800E	
V_{DRM}	Repetitive peak off-state voltages	600	800	V
$I_{T(RMS)}$	RMS on-state current	4	4	A
I_{TSM}	Non-repetitive peak on-state current	25	25	A

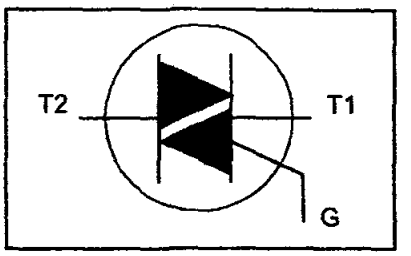
PINNING - TO220AB

PIN	DESCRIPTION
1	main terminal 1
2	main terminal 2
3	gate
tab	main terminal 2

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.		UNIT
				-600	-800	
V_{DRM}	Repetitive peak off-state voltages		-	600[1]	800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{mb} \leq 107$ °C	-	4		A
I_{TSM}	Non-repetitive peak on-state current	full sine wave; $T_j = 25$ °C prior to surge				
		t = 20 ms	-	25		A
		t = 16.7 ms	-	27		A
I^2t	I^2t for fusing	t = 10 ms	-	3.1		A^2s
dI_T/dt	Repetitive rate of rise of on-state current after triggering	I_{TM} = 6 A; I_G = 0.2 A; dI_G/dt = 0.2 A/µs				
		T2+ G+	-	50		A/µs
		T2+ G-	-	50		A/µs
		T2- G-	-	50		A/µs
		T2- G+	-	10		A/µs
I_{GM}	Peak gate current		-	2		A
V_{GM}	Peak gate voltage		-	5		V
P_{GM}	Peak gate power		-	5		W
$P_{G(AV)}$	Average gate power	over any 20 ms period	-	0.5		W
T_{stg}	Storage temperature		-40	150		°C
T_j	Operating junction temperature		-	125		°C

1 Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 3 A/µs.

HERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base	full cycle	-	-	3.0	K/W
		half cycle	-	-	3.7	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	in free air	-	60	-	K/W

TATIC CHARACTERISTICS

T_j = 25 °C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS		MIN.	TYP.	MAX.	UNIT
I_{GT}	Gate trigger current	V_D = 12 V; I_T = 0.1 A					
			T2+ G+	-	2.5	10	mA
			T2+ G-	-	4.0	10	mA
			T2- G-	-	5.0	10	mA
			T2- G+	-	11	25	mA
I_L	Latching current	V_D = 12 V; I_{GT} = 0.1 A					
			T2+ G+	-	3.0	15	mA
			T2+ G-	-	10	20	mA
			T2- G-	-	2.5	15	mA
			T2- G+	-	4.0	20	mA
I_H	Holding current	V_D = 12 V; I_{GT} = 0.1 A		-	2.2	15	mA
V_T	On-state voltage	I_T = 5 A		-	1.4	1.70	V
V_{GT}	Gate trigger voltage	V_D = 12 V; I_T = 0.1 A		-	0.7	1.5	V
		V_D = 400 V; I_T = 0.1 A; T_j = 125 °C		0.25	0.4	-	V
I_D	Off-state leakage current	$V_D = V_{DRM(max)}$; T_j = 125 °C		-	0.1	0.5	mA

YNAMIC CHARACTERISTICS

T_j = 25 °C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
dV_D/dt	Critical rate of rise of off-state voltage	V_{DM} = 67% $V_{DRM(max)}$; T_j = 125 °C; exponential waveform; gate open circuit	-	50	-	V/µs
t_{gt}	Gate controlled turn-on time	I_{TM} = 6 A; $V_D = V_{DRM(max)}$; I_G = 0.1 A; dI_G/dt = 5 A/µs	-	2	-	µs

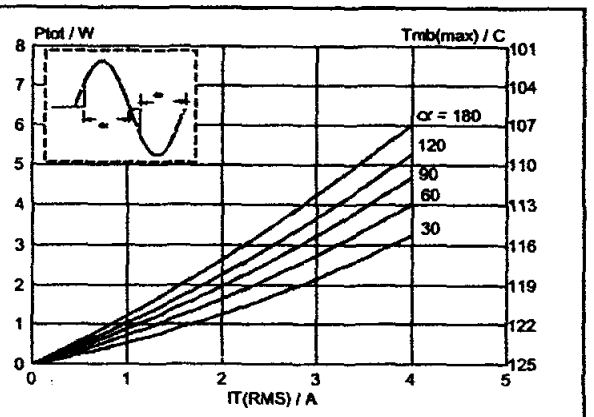


Fig.1. Maximum on-state dissipation, P_{tot}, versus rms on-state current, $I_{T(RMS)}$, where α = conduction angle.

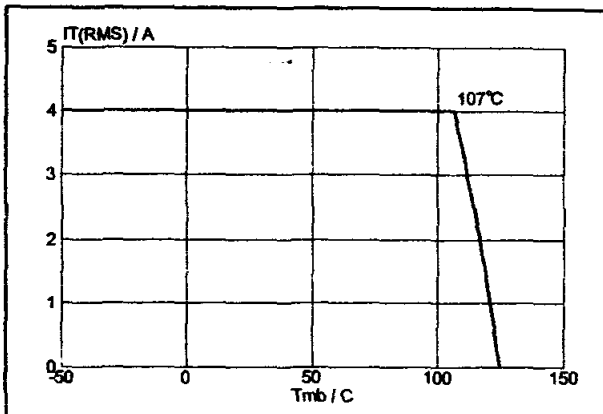


Fig.4. Maximum permissible rms current $I_{T(RMS)}$, versus mounting base temperature T_{mb}.

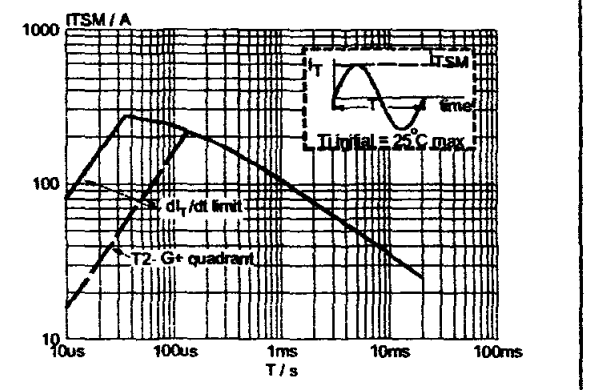


Fig.2. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus pulse width t_p, for sinusoidal currents, $t_p \leq 20ms$.

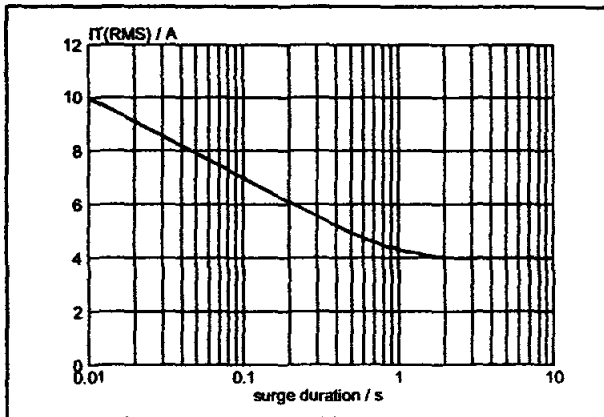


Fig.5. Maximum permissible repetitive rms on-state current $I_{T(RMS)}$, versus surge duration, for sinusoidal currents, f = 50 Hz; $T_{mb} \leq 107°C$.

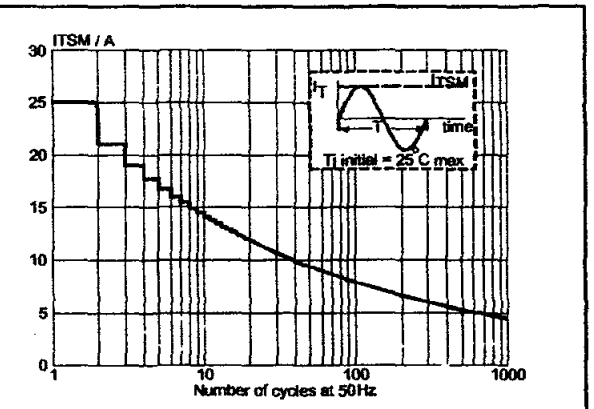


Fig.3. Maximum permissible non-repetitive peak on-state current I_{TSM}, versus number of cycles, for sinusoidal currents, f = 50 Hz.

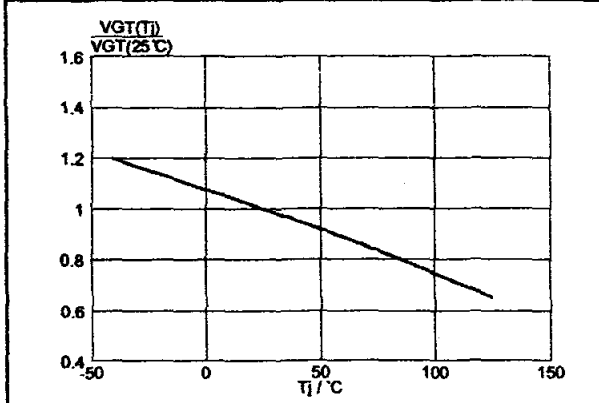


Fig.6. Normalised gate trigger voltage $V_{GT}(T_j)/ V_{GT}(25°C)$, versus junction temperature T_j.

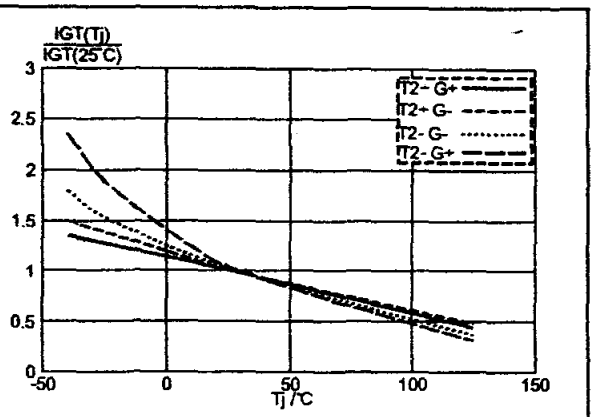


Fig.7. Normalised gate trigger current $I_{GT}(T_j)/ I_{GT}(25°C)$, versus junction temperature T_j.

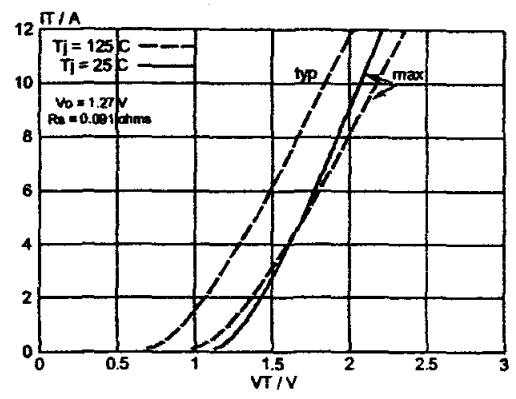


Fig.10. Typical and maximum on-state characteristic.

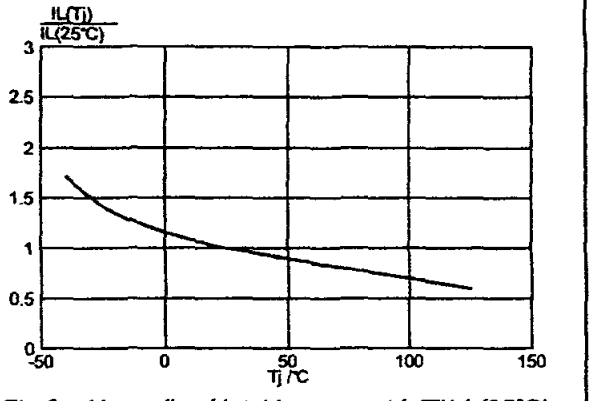


Fig.8. Normalised latching current $I_L(T_j)/ I_L(25°C)$, versus junction temperature T_j.

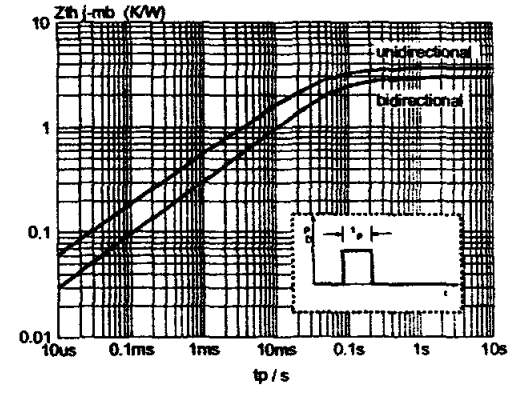


Fig.11. Transient thermal impedance $Z_{th\ j\text{-}mb}$, versus pulse width t_p.

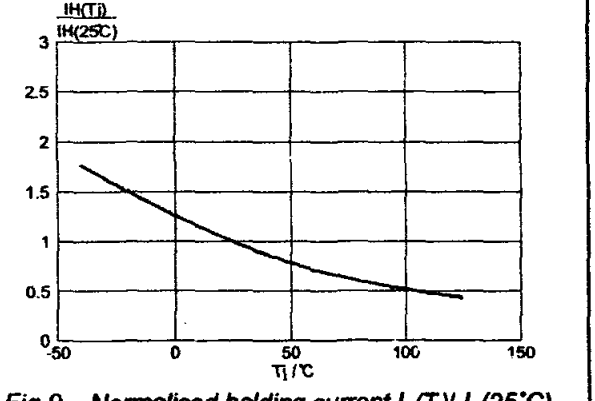


Fig.9. Normalised holding current $I_H(T_j)/ I_H(25°C)$, versus junction temperature T_j.

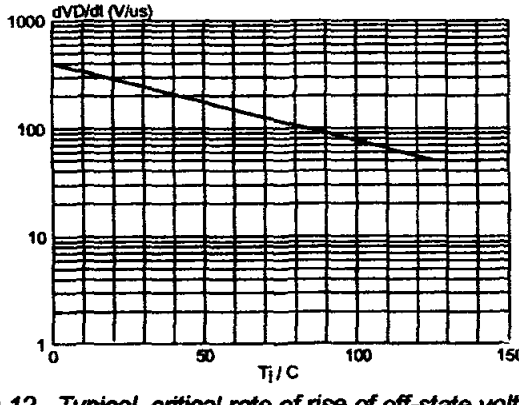


Fig.12. Typical, critical rate of rise of off-state voltage, dV_D/dt versus junction temperature T_j.

MECHANICAL DATA

Dimensions in mm

Net Mass: 2 g

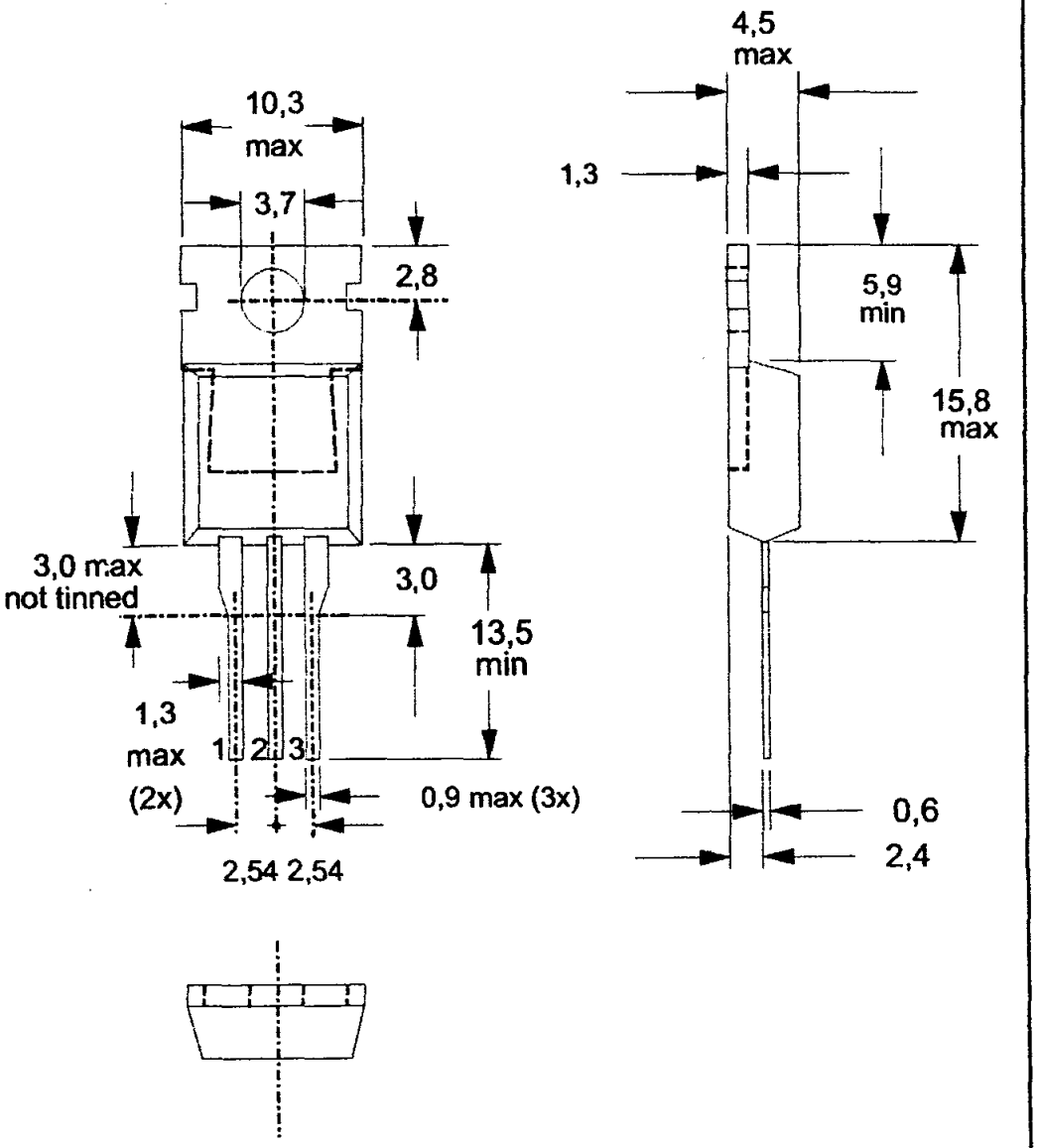


Fig.13. SOT78 (TO220AB). pin 2 connected to mounting base.

Notes
1. Refer to mounting instructions for SOT78 (TO220) envelopes.
2. Epoxy meets UL94 V0 at 1/8".

DEFINITIONS

DATA SHEET STATUS		
DATA SHEET STATUS[2]	**PRODUCT STATUS[3]**	**DEFINITIONS**
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in ordere to improve the design and supply the best possible product
Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A

Limiting values

Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information

Where application information is given, it is advisory and does not form part of the specification.

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices or systems where malfunction of these products can be reasonably expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

2 Please consult the most recently issued datasheet before initiating or completing a design.

3 The product status of the device(s) described in this datasheet may have changed since this datasheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

MOTOROLA
SEMICONDUCTOR TECHNICAL DATA

Order this document
by 2N3055/D

Complementary Silicon Power Transistors

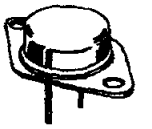
. . . designed for general–purpose switching and amplifier applications.

- DC Current Gain — h_{FE} = 20–70 @ I_C = 4 Adc
- Collector–Emitter Saturation Voltage —
  $V_{CE(sat)}$ = 1.1 Vdc (Max) @ I_C = 4 Adc
- Excellent Safe Operating Area

NPN
2N3055*
PNP
MJ2955*

*Motorola Preferred Device

15 AMPERE
POWER TRANSISTORS
COMPLEMENTARY
SILICON
60 VOLTS
115 WATTS



CASE 1–07
TO–204AA
(TO–3)

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector–Emitter Voltage	V_{CEO}	60	Vdc
Collector–Emitter Voltage	V_{CER}	70	Vdc
Collector–Base Voltage	V_{CB}	100	Vdc
Emitter–Base Voltage	V_{EB}	7	Vdc
Collector Current — Continuous	I_C	15	Adc
Base Current	I_B	7	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	115 0.657	Watts W/°C
Operating and Storage Junction Temperature Range	T_J, T_{stg}	–65 to +200	°C

THERMAL CHARACTERISTICS

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.52	°C/W

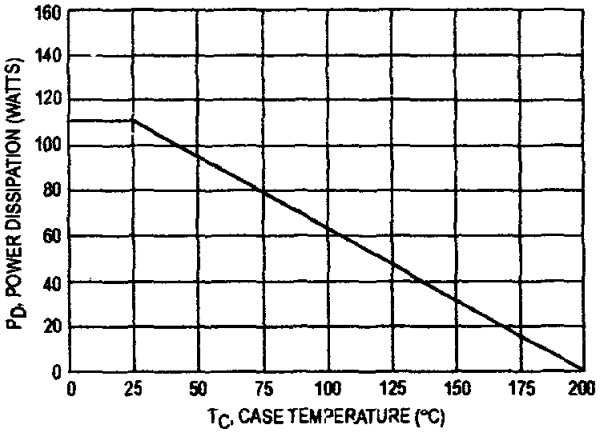


Figure 1. Power Derating

Preferred devices are Motorola recommended choices for future use and best overall value.

MOTOROLA

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS				
Collector–Emitter Sustaining Voltage (1) (I_C = 200 mAdc, I_B = 0)	$V_{CEO(sus)}$	60	—	Vdc
Collector–Emitter Sustaining Voltage (1) (I_C = 200 mAdc, R_{BE} = 100 Ohms)	$V_{CER(sus)}$	70	—	Vdc
Collector Cutoff Current (V_{CE} = 30 Vdc, I_B = 0)	I_{CEO}	—	0.7	mAdc
Collector Cutoff Current (V_{CE} = 100 Vdc, $V_{BE(off)}$ = 1.5 Vdc) (V_{CE} = 100 Vdc, $V_{BE(off)}$ = 1.5 Vdc, T_C = 150°C)	I_{CEX}	— —	1.0 5.0	mAdc
Emitter Cutoff Current (V_{BE} = 7.0 Vdc, I_C = 0)	I_{EBO}	—	5.0	mAdc
ON CHARACTERISTICS (1)				
DC Current Gain (I_C = 4.0 Adc, V_{CE} = 4.0 Vdc) (I_C = 10 Adc, V_{CE} = 4.0 Vdc)	h_{FE}	20 5.0	70 —	—
Collector–Emitter Saturation Voltage (I_C = 4.0 Adc, I_B = 400 mAdc) (I_C = 10 Adc, I_B = 3.3 Adc)	$V_{CE(sat)}$	—	1.1 3.0	Vdc
Base–Emitter On Voltage (I_C = 4.0 Adc, V_{CE} = 4.0 Vdc)	$V_{BE(on)}$	—	1.5	Vdc
SECOND BREAKDOWN				
Second Breakdown Collector Current with Base Forward Biased (V_{CE} = 40 Vdc, t = 1.0 s, Nonrepetitive)	$I_{s/b}$	2.87	—	Adc
DYNAMIC CHARACTERISTICS				
Current Gain — Bandwidth Product (I_C = 0.5 Adc, V_{CE} = 10 Vdc, f = 1.0 MHz)	f_T	2.5	—	MHz
*Small–Signal Current Gain (I_C = 1.0 Adc, V_{CE} = 4.0 Vdc, f = 1.0 kHz)	h_{fe}	15	120	—
*Small–Signal Current Gain Cutoff Frequency (V_{CE} = 4.0 Vdc, I_C = 1.0 Adc, f = 1.0 kHz)	f_{hfe}	10	—	kHz

*Indicates Within JEDEC Registration. (2N3055)
(1) Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

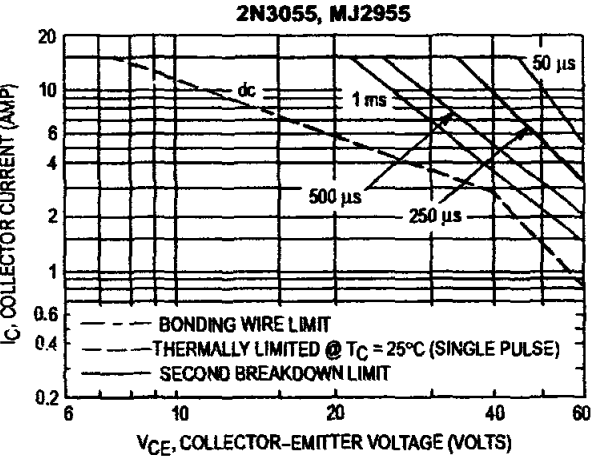


Figure 2. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 2 is based on T_C = 25°C; $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated for temperature according to Figure 1.

NPN
2N3055

PNP
MJ2955

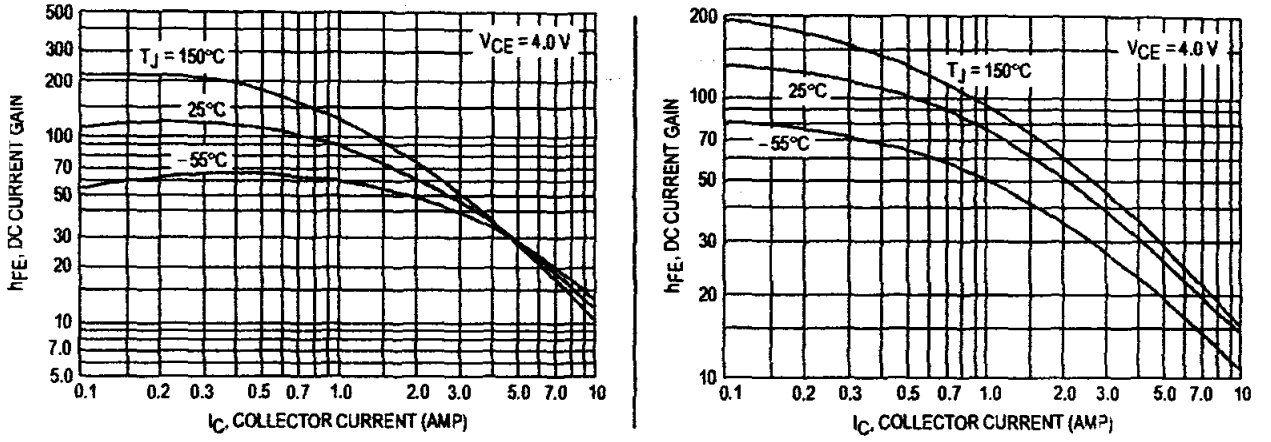


Figure 3. DC Current Gain

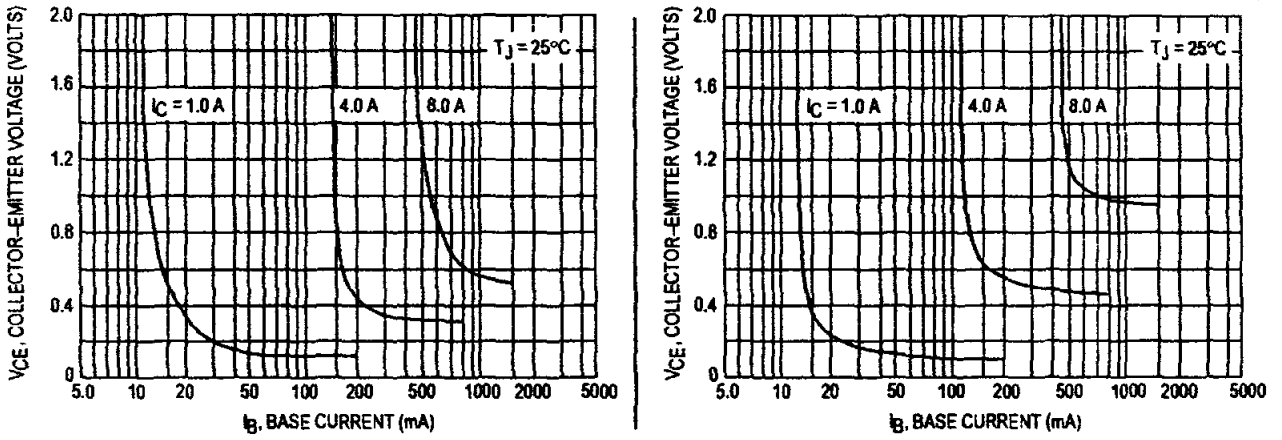


Figure 4. Collector Saturation Region

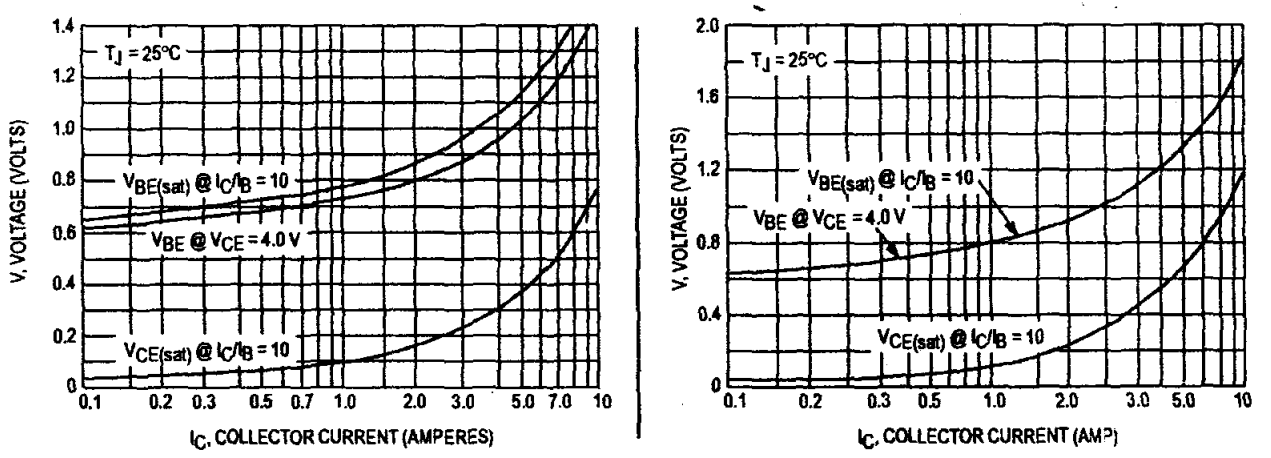
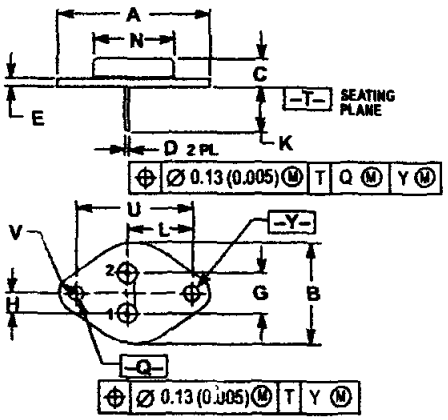


Figure 5. "On" Voltages

PACKAGE DIMENSIONS



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ALL RULES AND NOTES ASSOCIATED WITH REFERENCED TO-204AA OUTLINE SHALL APPLY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.550 REF		39.37 REF	
B	—	1.050	—	26.67
C	0.250	0.335	6.35	8.51
D	0.038	0.043	0.97	1.09
E	0.055	0.070	1.40	1.77
G	0.430 BSC		10.92 BSC	
H	0.215 BSC		5.46 BSC	
K	0.440	0.480	11.18	12.19
L	0.665 BSC		16.89 BSC	
N	—	0.830	—	21.08
Q	0.151	0.165	3.84	4.19
U	1.187 BSC		30.15 BSC	
V	0.131	0.188	3.33	4.77

STYLE 1:
PIN 1. BASE
2. EMITTER
CASE: COLLECTOR

CASE 1-07
TO-204AA (TO-3)
ISSUE Z

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FAIRCHILD
SEMICONDUCTOR™

BD135/137/139

Medium Power Linear and Switching Applications

- Complement to BD136, BD138 and BD140 respectively

1 TO-126

1. Emitter 2.Collector 3.Base

NPN Epitaxial Silicon Transistor

Absolute Maximum Ratings T_C=25°C unless otherwise noted

Symbol	Parameter		Value	Units
V_{CBO}	Collector-Base Voltage	: BD135	45	V
		: BD137	60	V
		: BD139	80	V
V_{CEO}	Collector-Emitter Voltage	: BD135	45	V
		: BD137	60	V
		: BD139	80	V
V_{EBO}	Emitter-Base Voltage		5	V
I_C	Collector Current (DC)		1.5	A
I_{CP}	Collector Current (Pulse)		3.0	A
I_B	Base Current		0.5	A
P_C	Collector Dissipation (T_C=25°C)		12.5	W
P_C	Collector Dissipation (T_a=25°C)		1.25	W
T_J	Junction Temperature		150	°C
T_{STG}	Storage Temperature		- 55 ~ 150	°C

Electrical Characteristics T_C=25°C unless otherwise noted

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V_{CEO}(sus)	Collector-Emitter Sustaining Voltage					
	: BD135	I_C = 30mA, I_B = 0	45			V
	: BD137		60			V
	: BD139		80			V
I_{CBO}	Collector Cut-off Current	V_{CB} = 30V, I_E = 0			0.1	μA
I_{EBO}	Emitter Cut-off Current	V_{EB} = 5V, I_C = 0			10	μA
h_{FE1}	DC Current Gain : ALL DEVICE	V_{CE} = 2V, I_C = 5mA	25			
h_{FE2}	: ALL DEVICE	V_{CE} = 2V, I_C = 0.5A	25			
h_{FE3}	: BD135	V_{CE} = 2V, I_C = 150mA	40		250	
	: BD137, BD139		40		160	
V_{CE}(sat)	Collector-Emitter Saturation Voltage	I_C = 500mA, I_B = 50mA			0.5	V
V_{BE}(on)	Base-Emitter ON Voltage	V_{CE} = 2V, I_C = 0.5A			1	V

h_{FE} Classification

Classification	6	10	16
h_{FE3}	40 ~ 100	63 ~ 160	100 ~ 250

Typical Characteristics

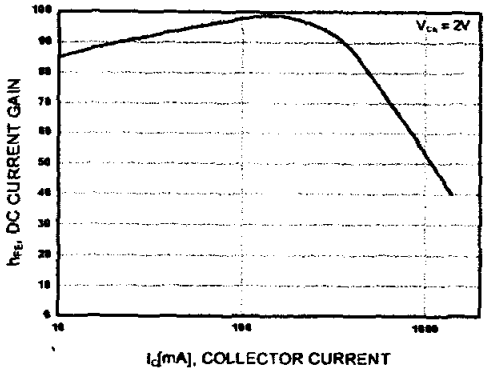


Figure 1. DC current Gain

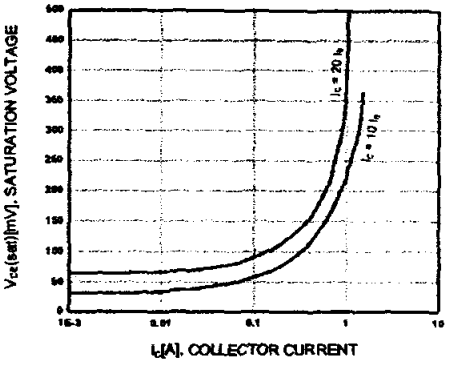


Figure 2. Collector-Emitter Saturation Voltage

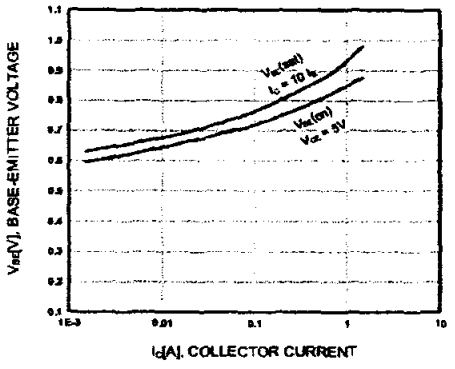


Figure 3. Base-Emitter Voltage

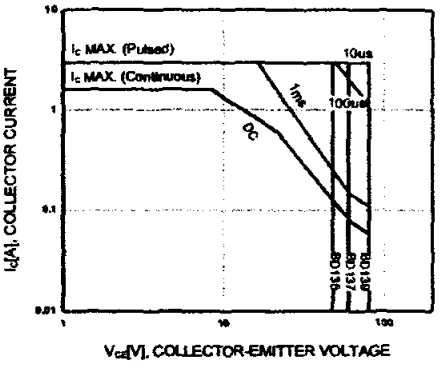


Figure 4. Safe Operating Area

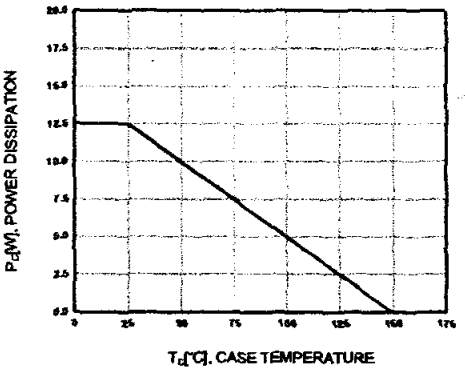
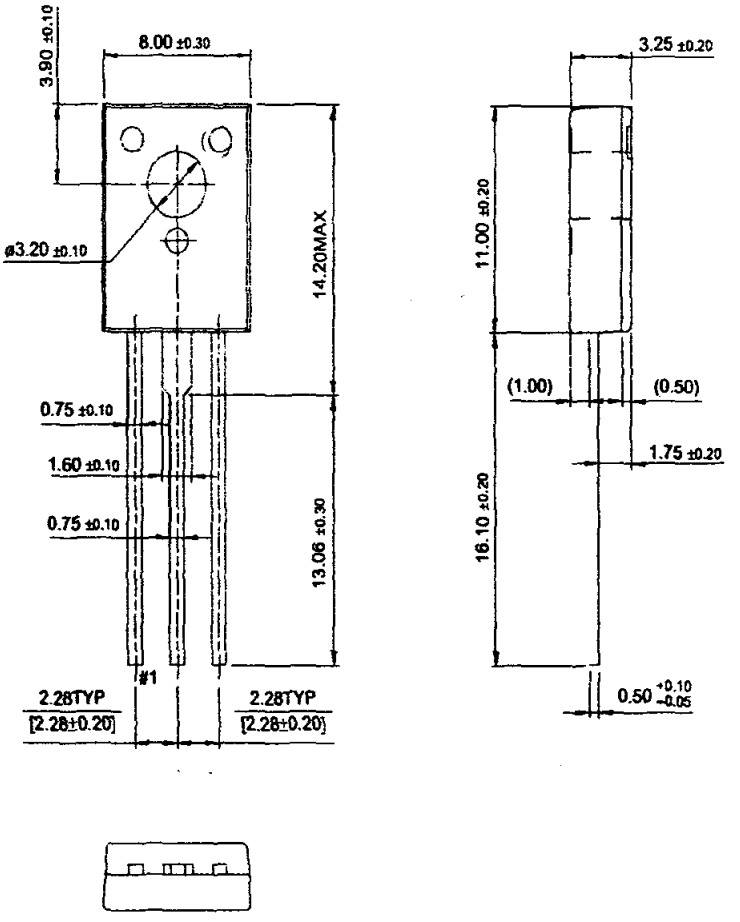


Figure 5. Power Derating

Package Demensions

TO-126



Dimensions in Millimeters

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PRODUCT STATUS DEFINITIONS

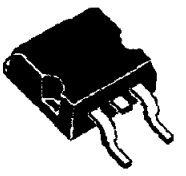
Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

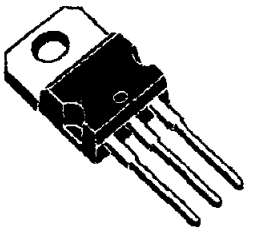
L7800AB/AC SERIES

PRECISION 1A REGULATORS

- OUTPUT CURRENT IN EXCESS OF 1 A
- OUTPUT VOLTAGES OF 5; 6; 8; 9; 12; 15; 18; 20; 24V
- THERMAL OVERLOAD PROTECTION
- OUTPUT TRANSITION SOA PROTECTION
- 2% OUTPUT VOLTAGE TOLERANCE
- GUARANTEED IN EXTENDED TEMPERATURE RANGE



D^2PAK

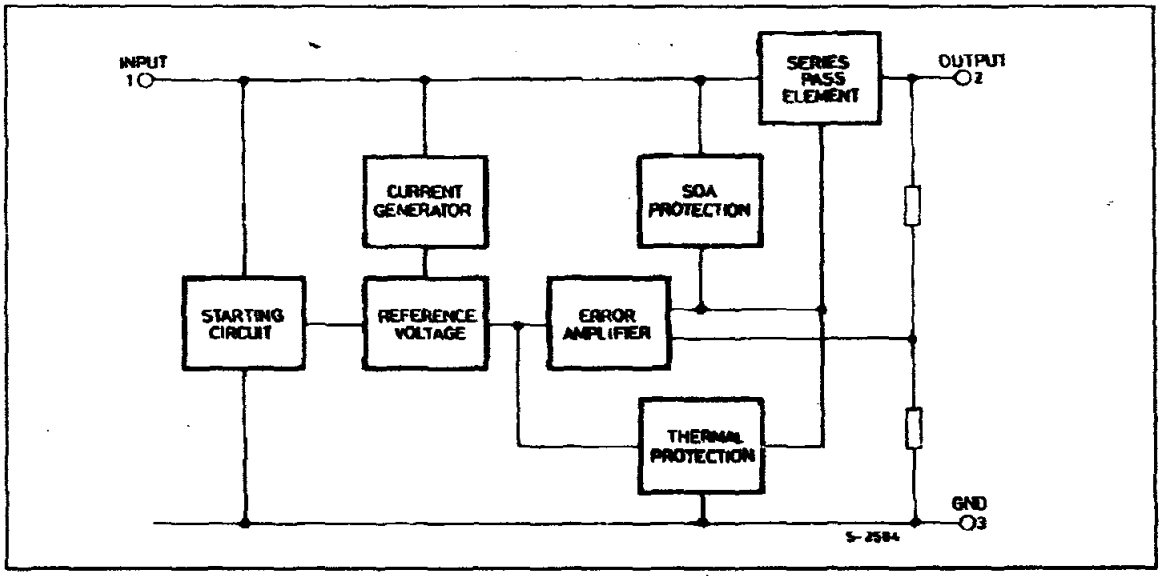


TO-220

DESCRIPTION

The L7800A series of three-terminal positive regulators is available in TO-220 and D^2PAK packages and several fixed output voltages, making it useful in a wide range of applications.These regulators can provide local on-card regulation, eliminating the distribution problems associated with single point regulation. Each type employs internal current limiting, thermal shut-down and safe area protection, making it essentially indestructible. If adequate heat sinking is provided, they can deliver over 1A output current. Although designed primarily as fixed voltage regulators, these devices can be used with external components to obtain adjustable voltages and currents.

BLOCK DIAGRAM



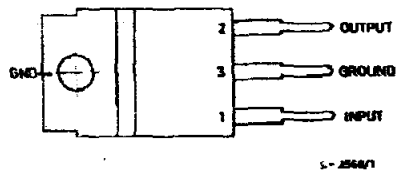
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_i	DC Input Voltage (for V_O = 5 to 18V) (for V_O = 20, 24V)	35 40	V V
I_o	Output Current	Internally limited	
P_{tot}	Power Dissipation	Internally limited	
T_{op}	Operating Junction Temperature Range (for **L7800AC**) (for **L7800AB**)	0 to 150 -40 to 125	°C °C
T_{stg}	Storage Temperature Range	- 65 to 150	°C

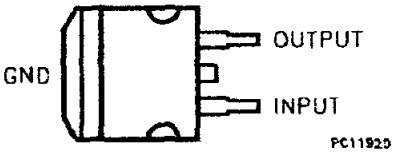
THERMAL DATA

Symbol	Parameter		D^2PAK	TO-220	Unit
$R_{thj\text{-}case}$	Thermal Resistance Junction-case	Max	3	3	°C/W
$R_{thj\text{-}amb}$	Thermal Resistance Junction-ambient	Max	62.5	50	°C/W

CONNECTION DIAGRAM AND ORDERING NUMBERS (top view)



TO-220

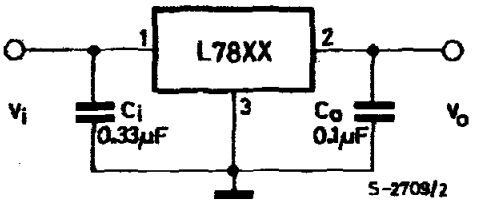


D^2PAK

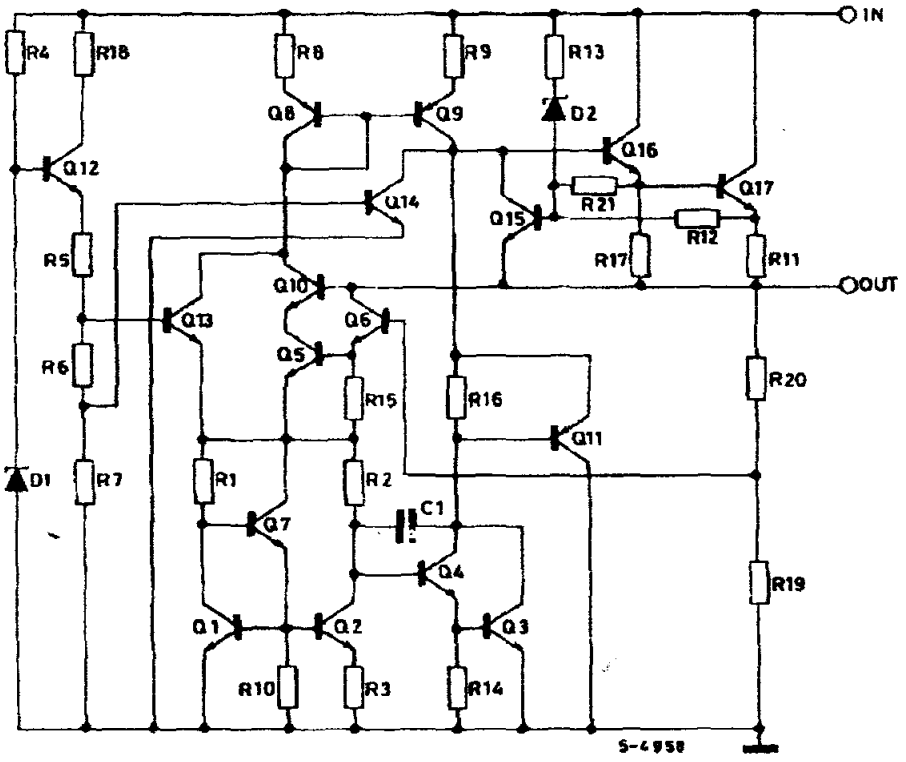
Type	TO-220	D^2PAK (*)	Output Voltage
L7805AB	L7805ABV	L7805ABD2T	5V
L7805AC	L7805ACV	L7805ACD2T	5V
L7806AB	L7806ABV	L7806ABD2T	6V
L7806AC	L7806ACV	L7806ACD2T	6V
L7808AB	L7808ABV	L7808ABD2T	8V
L7808AC	L7808ACV	L7808ACD2T	8V
L7809AB	L7809ABV	L7809ABD2T	9V
L7809AC	L7809ACV	L7809ACD2T	9V
L7812AB	L7812ABV	L7812ABD2T	12V
L7812AC	L7812ACV	L7812ACD2T	12V
L7815AB	L7815ABV	L7815ABD2T	15V
L7815AC	L7815ACV	L7815ACD2T	15V
L7818AB	L7818ABV		18V
L7818AC	L7818ACV		18V
L7820AB	L7820ABV		24V
L7820AC	L7820ACV		24V
L7824AB	L7824ABV		
L7824AC	L7824ACV		

(*) AVAILABLE IN TAPE AND REEL WITH "-TR" SUFFIX

APPLICATION CIRCUIT



SCHEMATIC DIAGRAM



TEST CIRCUITS

Figure 1 : DC Parameter

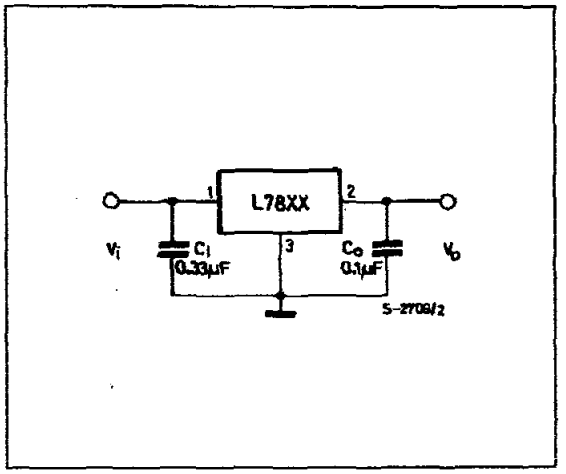


Figure 2 : Load Regulation.

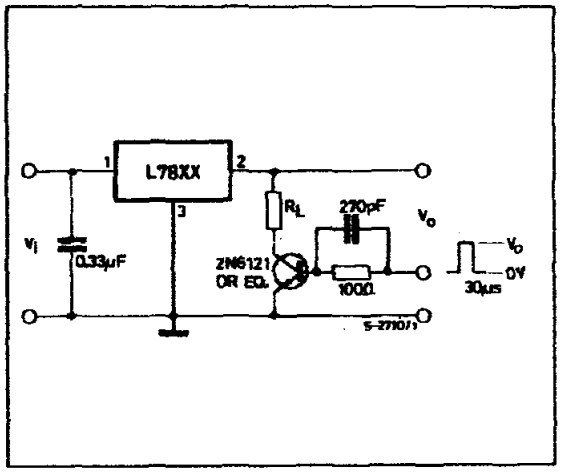
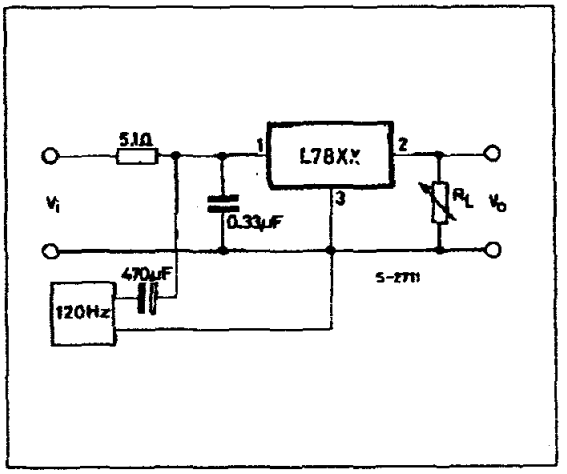


Figure 3 : Ripple Rejection.



ELECTRICAL CHARACTERISTICS FOR L7805A (V_i = 10V, I_o = 1 A, T_j = 0 to 125 °C (L7805AC), T_j = -40 to 125 °C (L7805AB) unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	T_j = 25 °C	4.9	5	5.1	V
V_o	Output Voltage	I_o = 5 mA to 1 A $P_o \leq$ 15 W V_i = 7.5 to 20 V	4.8	5	5.2	V
ΔV_o*	Line Regulation	V_i = 7.5 to 25 V I_o = 500 mA V_i = 8 to 12 V V_i = 8 to 12 V T_j = 25 °C V_i = 7.3 to 20 V T_j = 25 °C		7 10 2 7	50 5 25 50	mV mV mV mV
ΔV_o*	Load Regulation	I_o = 5 mA to 1 A I_o = 5 mA to 1.5 A T_j = 25 °C I_o = 250 to 750 mA		25 30 8	100 100 50	mV mV mV
I_d	Quiescent Current	T_j = 25 °C		4.3	6 6	mA
ΔI_d	Quiescent Current Change	V_i = 8 to 25 V I_o = 500 mA V_i = 7.5 to 20 V T_j = 25 °C I_o = 5 mA to 1 A			0.8 0.8 0.5	mA mA mA
SVR	Supply Voltage Rejection	V_i = 8 to 18 V f= 120 Hz I_o = 500 mA		68		dB
V_d	Dropout Voltage	I_o = 1 A T_j = 25 °C		2		V
e_N	Output Noise Voltage	B = 10Hz to 100KHz T_j = 25 °C		10		µV/V_o
R_o	Output Resistance	f = 1KHz		17		mΩ
I_{sc}	Short Circuit Current	V_i = 35 V T_{amb} = 25 °C		0.2		A
I_{scp}	Short Circuit Peack Current	T_j = 25 °C		2.2		A
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift			-1.1		mV/°C

* Load and line regulation are specified at constant junction temperature. Changes in V_o due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS FOR L7806A (V_i = 11V, I_o = 1 A, T_j = 0 to 125 °C (L7806AC), T_j = -40 to 125 °C (L7806AB) unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	T_j = 25 °C	5.88	6	6.12	V
V_o	Output Voltage	I_o = 5 mA to 1 A $P_o \leq$ 15 W V_i = 8.6 to 21 V	5.76	6	6.24	V
ΔV_o*	Line Regulation	V_i = 8.6 to 25 V I_o = 500 mA V_i = 9 to 13 V V_i = 9 to 13 V T_j = 25 °C V_i = 8.3 to 21 V T_j = 25 °C		9 11 3 9	60 60 30 60	mV mV mV mV
ΔV_o*	Load Regulation	I_o = 5 mA to 1 A I_o = 5 mA to 1.5 A T_j = 25 °C I_o = 250 to 750 mA		25 30 10	100 100 50	mV mV mV
I_d	Quiescent Current	T_j = 25 °C		4.3	6 6	mA
ΔI_d	Quiescent Current Change	V_i = 9 to 25 V I_o = 500 mA V_i = 8.6 to 21 V T_j = 25 °C I_o = 5 mA to 1 A			0.8 0.8 0.5	mA mA mA
SVR	Supply Voltage Rejection	V_i = 9 to 19 V f = 120 Hz I_o = 500 mA		65		dB
V_d	Dropout Voltage	I_o = 1 A T_j = 25 °C		2		V
e_N	Output Noise Voltage	B = 10Hz to 100KHz T_j = 25 °C		10		$\mu V/V_o$
R_o	Output Resistance	f = 1KHz		17		mΩ
I_{sc}	Short Circuit Current	V_i = 35 V T_{amb} = 25 °C		0.2		A
I_{scp}	Short Circuit Peack Current	T_j = 25 °C		2.2		A
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift			-0.8		mV/°C

* Load and line regulation are specified at constant junction temperature. Changes in V_o due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS FOR L7808A (V_i = 14V, I_o = 1 A, T_j = 0 to 125 °C (L7808AC), T_j = -40 to 125 °C (L7808AB) unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	T_j = 25 °C	7.84	8	8.16	V
V_o	Output Voltage	I_o = 5 mA to 1 A $P_o \leq$ 15 W V_i = 10.6 to 23 V	7.7	8	8.3	V
ΔV_o*	Line Regulation	V_i = 10.6 to 25 V I_o = 500 mA V_i = 11 to 17 V V_i = 11 to 17 V T_j = 25 °C V_i = 10.4 to 23 V T_j = 25 °C		12 15 5 12	80 80 40 80	mV mV mV mV
ΔV_o*	Load Regulation	I_o = 5 mA to 1 A I_o = 5 mA to 1.5 A T_j = 25 °C I_o = 250 to 750 mA		25 30 10	100 100 50	mV mV mV
I_d	Quiescent Current	T_j = 25 °C		4.3	6 6	mA
ΔI_d	Quiescent Current Change	V_i = 11 to 25 V I_o = 500 mA V_i = 10.6 to 23 V T_j = 25 °C I_o = 5 mA to 1 A			0.8 0.8 0.5	mA mA mA
SVR	Supply Voltage Rejection	V_i = 11.5 to 21.5 V f = 120 Hz I_o = 500 mA		62		dB
V_d	Dropout Voltage	I_o = 1 A T_j = 25 °C		2		V
e_N	Output Noise Voltage	B = 10Hz to 100KHz T_j = 25 °C		10		µV/V_o
R_o	Output Resistance	f = 1KHz		18		mΩ
I_{sc}	Short Circuit Current	V_i = 35 V T_{amb} = 25 °C		0.2		A
I_{scp}	Short Circuit Peack Current	T_j = 25 °C		2.2		A
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift			-0.8		mV/°C

* Load and line regulation are specified at constant junction temperature. Changes in V_o due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS FOR L7809A (V_i = 15V, I_o = 1 A, T_j = 0 to 125 °C (L7809AC), T_j = -40 to 125 °C (L7809AB) unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	T_j = 25 °C	8.82	9	9.18	V
V_o	Output Voltage	I_o = 5 mA to 1 A $P_o \leq$ 15 W V_i = 10.6 to 23 V	8.65	9	9.35	V
ΔV_o*	Line Regulation	V_i = 10.6 to 25 V I_o = 500 mA V_i = 11 to 17 V V_i = 11 to 17 V T_j = 25 °C V_i = 10.4 to 23 V T_j = 25 °C		12 15 5 12	90 90 45 90	mV mV mV mV
ΔV_o*	Load Regulation	I_o = 5 mA to 1 A I_o = 5 mA to 1.5 A T_j = 25 °C I_o = 250 to 750 mA		25 30 10	100 100 50	mV mV mV
I_d	Quiescent Current	T_j = 25 °C		4.3	6 6	mA
ΔI_d	Quiescent Current Change	V_i = 11 to 25 V I_o = 500 mA V_i = 10.6 to 23 V T_j = 25 °C I_o = 5 mA to 1 A			0.8 0.8 0.5	mA mA mA
SVR	Supply Voltage Rejection	V_i = 11.5 to 21.5 V f = 120 Hz I_o = 500 mA		61		dB
V_d	Dropout Voltage	I_o = 1 A T_j = 25 °C		2		V
e_N	Output Noise Voltage	B = 10Hz to 100KHz T_j = 25 °C		10		µV/V_o
R_o	Output Resistance	f = 1KHz		18		mΩ
I_{sc}	Short Circuit Current	V_i = 35 V T_{amb} = 25 °C		0.2		A
I_{scp}	Short Circuit Peack Current	T_j = 25 °C		2.2		A
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift			-0.8		mV/°C

* Load and line regulation are specified at constant junction temperature. Changes in V_o due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS FOR L7812A (V_i = 19V, I_o = 1 A, T_j = 0 to 125 °C (L7812AC), T_j = -40 to 125 °C (L7812AB) unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	T_j = 25°C	11.75	12	12.25	V
V_o	Output Voltage	I_o = 5 mA to 1 A $P_o \leq$ 15 W V_i = 14.8 to 27 V	11.5	12	12.5	V
ΔV_o*	Line Regulation	V_i = 14.8 to 30 V I_o = 500 mA V_i = 16 to 22 V V_i = 16 to 22 V T_j = 25 °C V_i = 14.5 to 27 V T_j = 25 °C		13 16 6 13	120 120 60 120	mV mV mV mV
ΔV_o*	Load Regulation	I_o = 5 mA to 1 A I_o = 5 mA to 1.5 A T_j = 25 °C I_o = 250 to 750 mA		25 30 10	100 100 50	mV mV mV
I_d	Quiescent Current	T_j = 25 °C		4.4	6 6	mA
ΔI_d	Quiescent Current Change	V_i = 15 to 30 V I_o = 500 mA V_i = 14.8 to 27 V T_j = 25 °C I_o = 5 mA to 1 A			0.8 0.8 0.5	mA mA mA
SVR	Supply Voltage Rejection	V_i = 15 to 25 V f = 120 Hz I_o = 500 mA		60		dB
V_d	Dropout Voltage	I_o = 1 A T_j = 25 °C		2		V
e_N	Output Noise Voltage	B = 10Hz to 100KHz T_j = 25 °C		10		µV/V_o
R_o	Output Resistance	f = 1KHz		18		mΩ
I_{sc}	Short Circuit Current	V_i = 35 V T_{amb} = 25 °C		0.2		A
I_{scp}	Short Circuit Peack Current	T_j = 25 °C		2.2		A
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift			-1		mV/°C

* Load and line regulation are specified at constant junction temperature. Changes in V_o due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS FOR L7815A (V_i = 23V, I_o = 1 A, T_j = 0 to 125 °C (L7815AC), T_j = -40 to 125 °C (L7815AB) unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	T_j = 25 °C	14.7	15	15.3	V
V_o	Output Voltage	I_o = 5 mA to 1 A $P_o \leq$ 15 W V_i = 17.9 to 30 V	14.4	15	15.6	V
ΔV_o*	Line Regulation	V_i = 17.9 to 30 V I_o = 500 mA V_i = 20 to 26 V V_i = 20 to 26 V T_j = 25 °C V_i = 17.5 to 30 V T_j = 25 °C		13 16 6 13	150 150 75 150	mV mV mV mV
ΔV_o*	Load Regulation	I_o = 5 mA to 1 A I_o = 5 mA to 1.5 A T_j = 25 °C I_o = 250 to 750 mA		25 30 10	100 100 50	mV mV mV
I_d	Quiescent Current	T_j = 25 °C		4.4	6 6	mA
ΔI_o	Quiescent Current Change	V_i = 17.5 to 30 V I_o = 500 mA V_i = 17.5 to 30 V T_j = 25 °C I_o = 5 mA to 1 A			0.8 0.8 0.5	mA mA mA
SVR	Supply Voltage Rejection	V_i = 18.5 to 28.5 V f = 120 Hz I_o = 500 mA		58		dB
V_d	Dropout Voltage	I_o = 1 A T_j = 25 °C		2		V
e_N	Output Noise Voltage	B = 10Hz to 100KHz T_j = 25 °C		10		µV/V_o
R_o	Output Resistance	f = 1KHz		19		mΩ
I_{sc}	Short Circuit Current	V_i = 35 V T_{amb} = 25 °C		0.2		A
I_{scp}	Short Circuit Peack Current	T_j = 25 °C		2.2		A
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift			-1		mV/°C

* Load and line regulation are specified at constant junction temperature. Changes in V_o due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS FOR L7818A (V_i = 27V, I_o = 1 A, T_j = 0 to 125 °C (L7818AC), T_j = -40 to 125 °C (L7818AB) unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	T_j = 25 °C	17.64	18	18.36	V
V_o	Output Voltage	I_o = 5 mA to 1 A $P_o \leq$ 15 W V_i = 21 to 33 V	17.3	18	18.7	V
ΔV_o*	Line Regulation	V_i = 21 to 33 V I_o = 500 mA V_i = 24 to 30 V V_i = 24 to 30 V T_j = 25 °C V_i = 20.6 to 33 V T_j = 25 °C		25 28 10 5	180 180 90 180	mV mV mV mV
ΔV_o*	Load Regulation	I_o = 5 mA to 1 A I_o = 5 mA to 1.5 A T_j = 25 °C I_o = 250 to 750 mA		25 30 10	100 100 50	mV mV mV
I_d	Quiescent Current	T_j = 25 °C		4.5	6 6	mA
ΔI_d	Quiescent Current Change	V_i = 21 to 33 V I_o = 500 mA V_i = 21 to 33 V T_j = 25 °C I_o = 5 mA to 1 A			0.8 0.8 0.5	mA mA mA
SVR	Supply Voltage Rejection	V_i = 22 to 32 V f = 120 Hz I_o = 500 mA		57		dB
V_d	Dropout Voltage	I_o = 1 A T_j = 25 °C		2		V
e_N	Output Noise Voltage	B = 10Hz to 100KHz T_j = 25 °C		10		μV/V_o
R_o	Output Resistance	f = 1KHz		19		mΩ
I_{sc}	Short Circuit Current	V_i = 35 V T_{amb} = 25 °C		0.2		A
I_{scp}	Short Circuit Peack Current	T_j = 25 °C		2.2		A
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift			-1		mV/°C

* Load and line regulation are specified at constant junction temperature. Changes in V_o due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS FOR L7820A (V_i = 28V, I_o = 1 A, T_j = 0 to 125 °C (L7820AC), T_j = -40 to 125 °C (L7820AB) unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	T_j = 25 °C	19.6	20	20.4	V
V_o	Output Voltage	I_o = 5 mA to 1 A $P_o \leq$ 15 W V_i = 23 to 35 V	19.2	20	20.8	V
ΔV_o*	Line Regulation	V_i = 23 to 35 V I_o = 500 mA V_i = 26 to 32 V V_i = 26 to 32 V T_j = 25 °C V_i = 23 to 32 V T_j = 25 °C			200 200 100 200	mV mV mV mV
ΔV_o*	Load Regulation	I_o = 5 mA to 1 A I_o = 5 mA to 1.5 A T_j = 25 °C I_o = 250 to 750 mA		25 30 10	100 100 50	mV mV mV
I_d	Quiescent Current	T_j = 25 °C		4.5	6 6	mA
ΔI_d	Quiescent Current Change	V_i = 23 to 35 V I_o = 500 mA V_i = 23 to 35 V T_j = 25 °C I_o = 5 mA to 1 A			0.8 0.8 0.5	mA mA mA
SVR	Supply Voltage Rejection	V_i = 24 to 35 V f = 120 Hz I_o = 500 mA		56		dB
V_d	Dropout Voltage	I_o = 1 A T_j = 25 °C		2		V
e_N	Output Noise Voltage	B = 10Hz to 100KHz T_j = 25 °C		10		$\mu V/V_o$
R_o	Output Resistance	f = 1KHz		20		mΩ
I_{sc}	Short Circuit Current	V_i = 35 V T_{amb} = 25 °C		0.2		A
I_{scp}	Short Circuit Peack Current	T_j = 25 °C		2.2		A
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift			-1		mV/°C

* *Load and line regulation are specified at constant junction temperature.* Changes in V_o due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

ELECTRICAL CHARACTERISTICS FOR L7824A (V_i = 33V, I_o = 1 A, T_j = 0 to 125 °C (L7824AC), T_j = -40 to 125 °C (L7824AB) unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_o	Output Voltage	T_j = 25 °C	23.5	24	24.5	V
V_o	Output Voltage	I_o = 5 mA to 1 A $P_o \leq$ 15 W V_i = 27.3 to 38 V	23	24	25	V
ΔV_o*	Line Regulation	V_i = 27 to 38 V I_o = 500 mA V_i = 30 to 36 V V_i = 30 to 36 V T_j = 25 °C V_i = 26.7 to 38 V T_j = 25 °C		31 35 14 31	240 240 120 240	mV mV mV mV
ΔV_o*	Load Regulation	I_o = 5 mA to 1 A I_o = 5 mA to 1.5 A T_j = 25 °C I_o = 250 to 750 mA		25 30 10	100 100 50	mV mV mV
I_d	Quiescent Current	T_j = 25 °C		4.6	6 6	mA
ΔI_d	Quiescent Current Change	V_i = 27.3 to 38 V I_o = 500 mA V_i = 27.3 to 38 V T_j = 25 °C I_o = 5 mA to 1 A			0.8 0.8 0.5	mA mA mA
SVR	Supply Voltage Rejection	V_i = 28 to 38 V f = 120 Hz I_o = 500 mA		54		dB
V_d	Dropout Voltage	I_o = 1 A T_j = 25 °C		2		V
e_N	Output Noise Voltage	B = 10Hz to 100KHz T_j = 25 °C		10		µV/V_o
R_o	Output Resistance	f = 1KHz		20		mΩ
I_{sc}	Short Circuit Current	V_i = 35 V T_{amb} = 25 °C		0.2		A
I_{scp}	Short Circuit Peack Current	T_j = 25 °C		2.2		A
$\frac{\Delta V_o}{\Delta T}$	Output Voltage Drift			-1.5		mV/°C

* Load and line regulation are specified at constant junction temperature. Changes in V_o due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

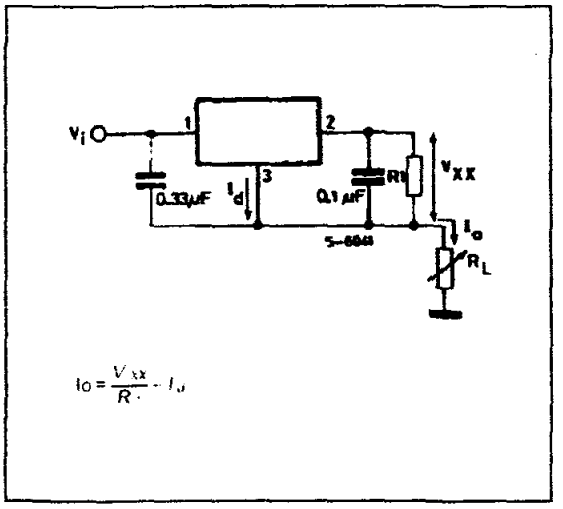
APPLICATIONS INFORMATION

DESIGN CONSIDERATIONS

The L7800A Series of fixed voltage regulators are designed with Thermal Overload Protection that shuts down the circuit when subjected to an excessive power overload condition, Internal Short-circuit Protection that limits the maximum current the circuit will pass, and Output Transistor Safe-Area Compensation that reduces the output short-circuit current as the voltage across the pass transistor is increased.

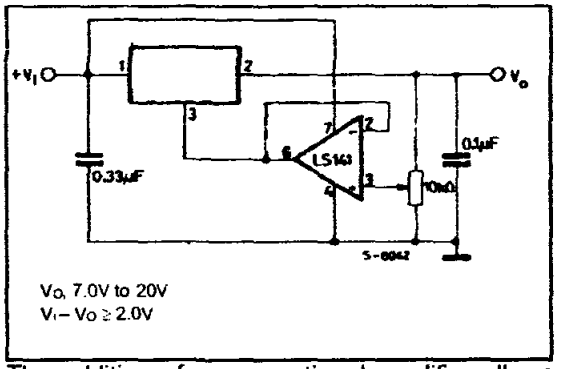
In many low current applications, compensation capacitors are not required. However, it is recommended that the regulator input be bypassed with a capacitor if the regulator is connected to the power supply filter with long wire lengths, or if the output load capacitance is large. An input bypass capacitor should be selected to provide good high-frequency characteristics to insure stable operation under all load conditions. A 0.33µF or larger tantalum, mylar, or other capacitor having low internal impedance at high frequencies should be chosen. The bypass capacitor should be mounted with the shortest possible leads directly across the regulators input terminals. Normally good construction techniques should be used to minimize ground loops and lead resistance drops since the regulator has no external sense lead.

Figure 4 : Current Regulator.



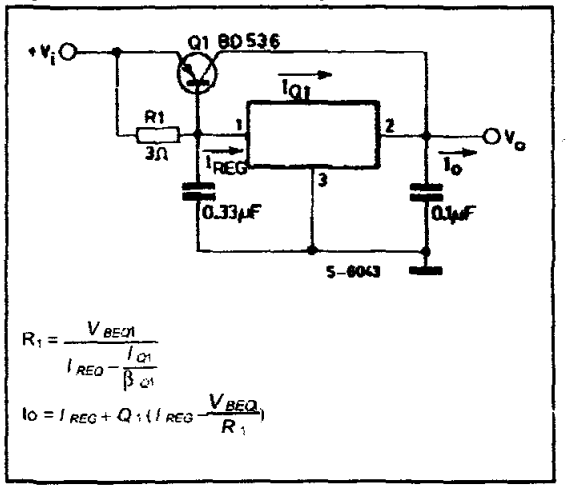
$$Io = \frac{V_{XX}}{R_1} + I_d$$

Figure 5 : Adjustable Output Regulator.



The addition of an operational amplifier allows adjustment to higher or intermediate values while retaining regulation characteristics. The minimum voltage obtainable with this arrangement is 2.0V greater than the regulator voltage.

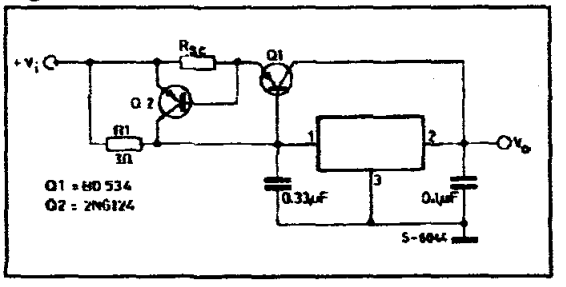
Figure 6 : Current Boost Regulator.



$$R_1 = \frac{V_{BEQ1}}{I_{REG} - \frac{I_{Q1}}{\beta_{Q1}}}$$

$$Io = I_{REG} + Q_1 \left(I_{REG} - \frac{V_{BEQ1}}{R_1}\right)$$

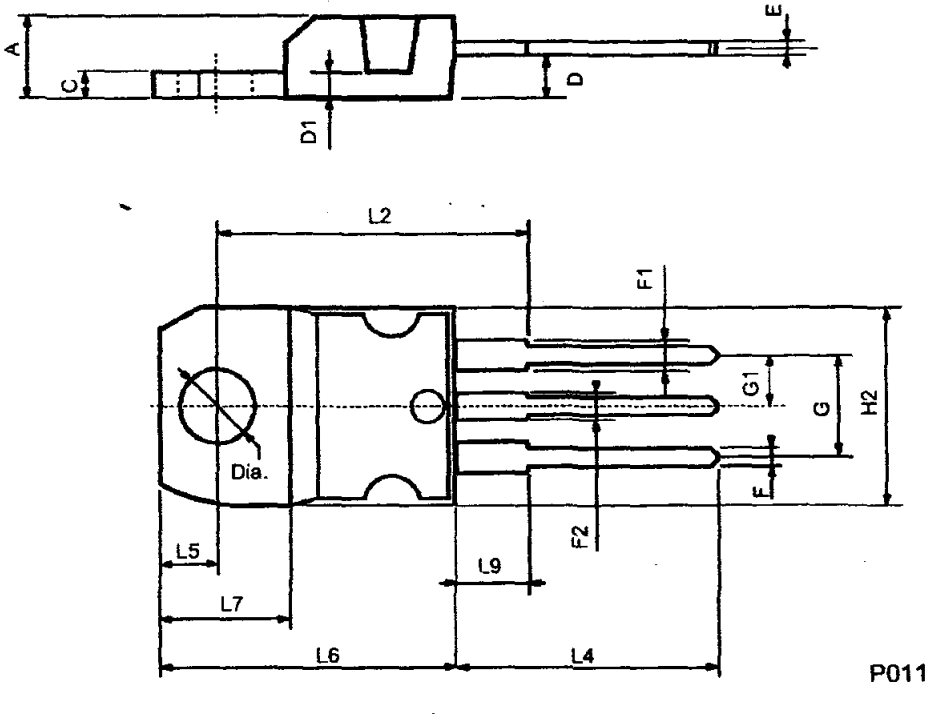
Figure 7 : Short-circuit Protection.



The circuit of figure 6 can be modified to provide supply protection against short circuit by adding a short-circuit sense resistor, R_{SC}, and an additional PNP transistor. The current sensing PNP must be able to handle the short-circuit current of the three-terminal regulator. Therefore, a four-ampere plastic power transistor is specified.

TO-220 MECHANICAL DATA

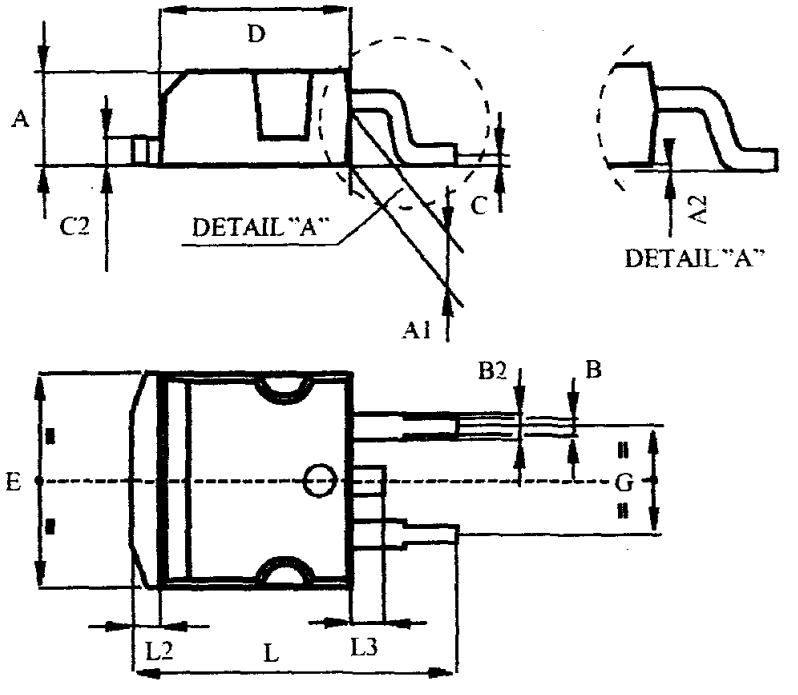
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
C	1.23		1.32	0.048		0.051
D	2.40		2.72	0.094		0.107
D1		1.27			0.050	
E	0.49		0.70	0.019		0.027
F	0.61		0.88	0.024		0.034
F1	1.14		1.70	0.044		0.067
F2	1.14		1.70	0.044		0.067
G	4.95		5.15	0.194		0.203
G1	2.4		2.7	0.094		0.106
H2	10.0		10.40	0.393		0.409
L2		16.4			0.645	
L4	13.0		14.0	0.511		0.551
L5	2.65		2.95	0.104		0.116
L6	15.25		15.75	0.600		0.620
L7	6.2		6.6	0.244		0.260
L9	3.5		3.93	0.137		0.154
DIA.	3.75		3.85	0.147		0.151



P011C

TO-263 (D^2PAK) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
B	0.7		0.93	0.027		0.036
B2	1.14		1.7	0.044		0.067
C	0.45		0.6	0.017		0.023
C2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
E	10		10.4	0.393		0.409
G	4.88		5.28	0.192		0.208
L	15		15.85	0.590		0.624
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.068



P011P6/F