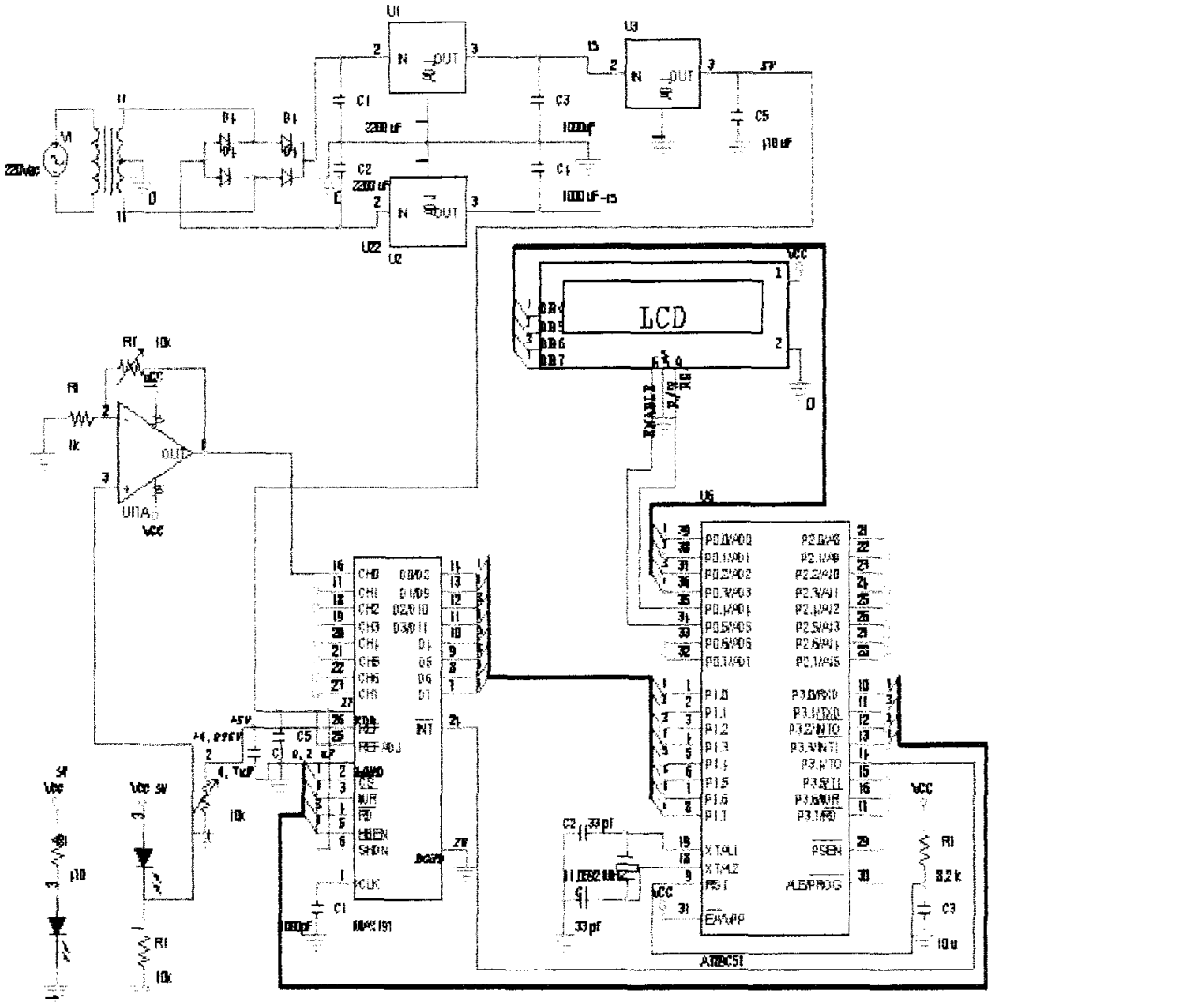
LAMPIRAN



Title	<Title>	
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```
        $MOD51

        CSEG
            ORG   00H
        JMP   START

KATA:       DB    '** TURBIDITY **',0,'NTU',0
VALUE01:    DB    73,74,75,76,77,0
VALUE02:    DB    82,83,84,0
VALUE03:    DB    89,90,91,92,93,0
VALUE04:    DB    111,112,113,114,115,0

;-----------------
;       Delay 4 mS
;-----------------
D4mS:       MOV   R7,#29
D4mS01:     MOV   R6,#64
            DJNZ  R6,$
            DJNZ  R7,D4mS01
            RET

;-----------------
;    Delay 1 S
;-----------------
D1S:        MOV   R7,#20
D1S01:      MOV   R6,#128
D1S02:      MOV   R5,#180
        DJNZ  R5,$
        DJNZ  R6,D1S02
        DJNZ  R7,D1S01
        RET

;------------------------------
;       Enable Pulse Instruction
;------------------------------
EPI:            ANL   A,#00FH               ;4 Bit
        ORL   A,#0D0H       ;Enable High, Instruction Input
        MOV   P0,A
        ANL   A,#0CFH       ;Enable Low, Instruction Input
        MOV   P0,A
            ACALL D4mS                  ;Delay 4 mS
            RET

;---------------------------
;       LCD Control Instruction
;---------------------------
```

```
LCI:        MOV   R5,A
              SWAP  A              ;Ambil 4 Bit (D7..D4)
              ACALL EPI            ;Enable Pulse Instruction
            MOV   A,R5           ;Ambil 4 Bit (D3..D0)
              ACALL EPI            ;Enable Pulse Instruction
              RET

;-----------------------------
;       Inisialisasi LCD 4 Bit
;-----------------------------
IL4B:       MOV   R5,#3          ;Diulang 3 Kali
IL4B01:       MOV   A,#03H               ;Reset Sequence
              ACALL EPI            ;Enable Pulse Instruction
            DJNZ  R5,IL4B01
              MOV   A,#02H               ;Reset Sequence
              ACALL EPI            ;Enable Pulse Instruction

              MOV   A,#28H               ;Function Set
              ACALL LCI            ;(4 Bit, 2 Lines, 5 x 7 Dot Matrik)
              MOV   A,#06H         ;Entry Mode Set
              ACALL LCI            ;(Increment, No Display Shift)
              MOV   A,#0CH         ;Display On/Off Control
              ACALL LCI            ;(Display On, Cursor Off, Blink Off)
            MOV   A,#01H         ;Display Clear
              ACALL LCI            ;LCD Control Instruction
              RET

;------------------------
;       Enable Pulse Data
;------------------------
EPD:        ANL   A,#00FH        ;4 Bit
              ORL   A,#0F0H              ;Enable High, Data Input
            MOV   P0,A
            ANL   A,#0EFH        ;Enable Low, Data Input
            MOV   P0,A
              MOV  R7,#40          ;Delay 40 uS
              DJNZ  R7,$
              RET

;----------------------
;       LCD Control Data
;----------------------
LCD:        MOV   R5,A
              SWAP  A              ;Ambil 4 Bit (D7..D4)
              ACALL EPD            ;Enable Pulse Data
            MOV   A,R5           ;Ambil 4 Bit (D3..D0)
```

```
            ACALL   EPD         ;Enable Pulse Data
            RET

;--------------------
;     Tampilan Awal
;--------------------
KDKL:       MOV     A,#0        ;Kirim Data ke LCD
            MOVC        A,@A+DPTR
        INC     DPTR
            JZ      EscKDKL             ;Huruf sudah habis ?
            ACALL       LCD             ;LCD Control Data
        JMP     KDKL
EscKDKL:    RET

TA:         MOV     A,#080H     ;Cursor Home Line 1 Colom 0
        ACALL   LCI         ;LCD Control Instruction
        MOV     DPTR,#KATA
        ACALL   KDKL        ;Kirim Data ke LCD
        MOV     A,#0C9H     ;Cursor Home Line 2 Colom 9
        ACALL   LCI         ;LCD Control Instruction
        ACALL   KDKL        ;Kirim Data ke LCD
        RET

;----------------------------
;     Tampilkan Data ke LCD
;----------------------------
TDKL:       MOV     A,#0C3H     ;Cursor Home Line 2 Colom 3
        ACALL   LCI         ;LCD Control Instruction
        MOV     R0,#64H
TDKL01:     MOV     A,@R0
        ADD     A,#30H      ;Ubah menjadi kode ASCII
        ACALL   LCD         ;LCD Control Data
        DEC     R0
        CJNE    R0,#5FH,TDKL01
        RET

;--------------------------------
;     Analog Digital Conversion
;--------------------------------
ADC:        CLR     P3.3        ;Chip Select pin
        CLR     P3.2        ;Write pin
        MOV     P1,#40H
        SETB    P3.2        ;Write pin
        SETB    P3.3        ;Chip Select pin
        MOV     R7,#100
            DJNZ    R7,$
```

```
        MOV    P1,#0FFH
        CLR    P3.3        ;Chip Select pin
        CLR    P3.1        ;Read pin
        SETB   P3.0        ;HBEN pin
        MOV    R4,P1       ;4 MSB
        CLR    P3.0        ;HBEN pin
        MOV    R3,P1       ;8 LSB
        SETB   P3.1        ;Read pin
        SETB   P3.3        ;Chip Select pin
        RET

;----------------------
;    Devision 16 bit
;----------------------
D16b:     CLR    C
        MOV    34H,#0      ;Sisa bagi (LSB)
        MOV    35H,#0
        MOV    R7,#16      ;Diulang 16 kali

D01:      MOV    R6,#4
        MOV    R0,#32H
D02:      MOV    A,@R0
        RLC    A           ;Geser ke kiri (35H 34H 33H 32H)
            MOV   @R0,A
            INC    R0
        DJNZ   R6,D02

        MOV    A,34H       ;Pengurangan
        ADD    A,36H
        MOV    38H,A
        MOV    A,35H
        ADDC   A,37H
        MOV    39H,A
        JC     D03
        DJNZ   R7,D01
        RET

D03:      CLR    C
        MOV    A,32H
            ORL    A,#01H
        MOV    32H,A
        MOV    34H,38H
        MOV    35H,39H
        DJNZ   R7,D01
        RET
```

```
;------------------------
;     Konversi Data ADC
;------------------------
KDA:        CLR    C            ; R4 R3
            MOV    A,R3         ; 00 43
            SUBB   A,#70        ; ------- -
            MOV    R3,A         ; R4 R3
            MOV    A,R4
            SUBB   A,#0
            MOV    R4,A

;           MOV    R1,#2
;KDA00:      CLR    C
;           MOV    A,R4         ;       R4 R3
;           RRC    A            ; R4 R3 = -------
;           MOV    R4,A         ;         4
;           MOV    A,R3
;           RRC    A
;           MOV    R3,A
;           DJNZ   R1,KDA00

            MOV    32H,R3
            MOV    33H,R4
            MOV    36H,#018H     ;Bagi 1000
            MOV    37H,#0FCH
            ACALL  D16b          ;Devision 16 bit
            MOV    A,32H
            JZ     KDA01
            MOV    64H,A

KDA01:      MOV    32H,34H
            MOV    33H,35H
            MOV    36H,#09CH     ;Bagi 100
            MOV    37H,#0FFH
            ACALL  D16b          ;Devision 16 bit
            MOV    A,32H
            JZ     KDA02
            MOV    63H,A

KDA02:      MOV    A,34H
            MOV    B,#10         ;Bagi 10
            DIV    AB
            MOV    62H,A
            MOV    60H,B
            RET
```

```
;---------------
;     Cek Data
;---------------
CV:         MOV    A,#0          ;Cek Value
            MOVC   A,@A+DPTR
            JZ     EscCV
            INC    DPTR
            CJNE   A,3H,CV
EscCV:      RET

CD:         MOV    64H,#0F0H     ;F0H + 30H = " " (ASCII)
            MOV    63H,#0F0H     ;F0H + 30H = " " (ASCII)
            CJNE   R4,#0,CD05
            CLR    C
            MOV    A,#70
            SUBB   A,R3
            JC     CD01
            MOV    62H,#0
            MOV    60H,#0
            RET

CD01:       MOV    DPTR,#VALUE01
            ACALL  CV            ;Cek Value
            JZ     CD02
            MOV    62H,#0
            MOV    60H,#2
            RET

CD02:       MOV    DPTR,#VALUE02
            ACALL  CV            ;Cek Value
            JZ     CD03
            MOV    62H,#0
            MOV    60H,#8
            RET

CD03:       MOV    DPTR,#VALUE03
            ACALL  CV            ;Cek Value
            JZ     CD04
            MOV    62H,#3
            MOV    60H,#6
            RET

CD04:       MOV    DPTR,#VALUE04
            ACALL  CV            ;Cek Value
            JZ     CD05
```

```
;---------------
;     Cek Data
;---------------
CV:         MOV    A,#0          ;Cek Value
            MOVC   A,@A+DPTR
            JZ     EscCV
            INC    DPTR
            CJNE   A,3H,CV
EscCV:      RET

CD:         MOV    64H,#0F0H     ;F0H + 30H = " " (ASCII)
            MOV    63H,#0F0H     ;F0H + 30H = " " (ASCII)
            CJNE   R4,#0,CD05
            CLR    C
            MOV    A,#70
            SUBB   A,R3
            JC     CD01
            MOV    62H,#0
            MOV    60H,#0
            RET

CD01:       MOV    DPTR,#VALUE01
            ACALL  CV            ;Cek Value
            JZ     CD02
            MOV    62H,#0
            MOV    60H,#2
            RET

CD02:       MOV    DPTR,#VALUE02
            ACALL  CV            ;Cek Value
            JZ     CD03
            MOV    62H,#0
            MOV    60H,#8
            RET

CD03:       MOV    DPTR,#VALUE03
            ACALL  CV            ;Cek Value
            JZ     CD04
            MOV    62H,#3
            MOV    60H,#6
            RET

CD04:       MOV    DPTR,#VALUE04
            ACALL  CV            ;Cek Value
            JZ     CD05
```

```
        MOV   62H,#4
        MOV   60H,#2
        RET

CD05:     ACALL  KDA          ;Konversi Data ADC
        RET

;--------------------
;       Main Program
;--------------------
START:      MOV   61H,#0FEH     ;FEH + 30H = "." (ASCII)
        ACALL  IL4B         ;Inisialisasi LCD 4 Bit
        ACALL  TA           ;Tampilan Awal

MP01:     ACALL  ADC
        ACALL  CD           ;Cek Data
        ACALL  TDKL          ;Tampilkan Data ke LCD
        ACALL  D1S          ;Delay 1 S
        JMP    MP01
        END
```

LAMPIRAN B

Features

- **Compatible with MCS-51™ Products**
- **4K Bytes of In-System Reprogrammable Flash Memory**
  - **Endurance: 1,000 Write/Erase Cycles**
- **Fully Static Operation: 0 Hz to 24 MHz**
- **Three-Level Program Memory Lock**
- **128 x 8-Bit Internal RAM**
- **32 Programmable I/O Lines**
- **Two 16-Bit Timer/Counters**
- **Six Interrupt Sources**
- **Programmable Serial Channel**
- **Low Power Idle and Power Down Modes**

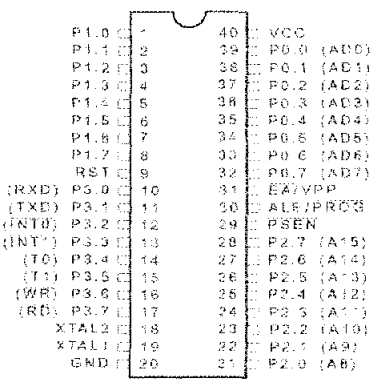
Description

The AT89C51 is a low-power, high-performance CMOS 8-bit microcomputer with 4K bytes of Flash Programmable and Erasable Read Only Memory (PEROM). The device is manufactured using Atmel's high density nonvolatile memory technology and is compatible with the industry standard MCS-51™ instruction set and pinout. The on-chip Flash allows the program memory to be reprogrammed in-system or by a conventional nonvolatile memory programmer. By combining a versatile 8-bit CPU with Flash on a monolithic chip, the Atmel AT89C51 is a powerful microcomputer which provides a highly flexible and cost effective solution to many embedded control applications.

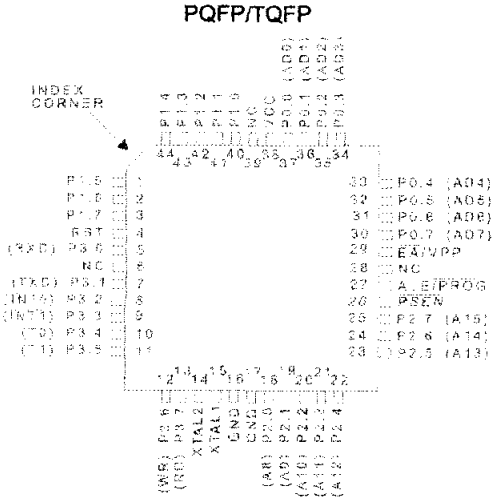
(continued)

Pin Configurations

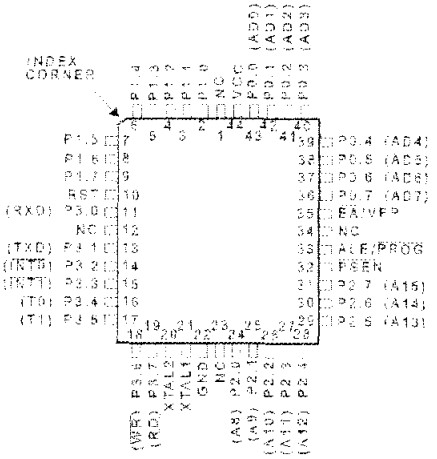
PDIP



PQFP/TQFP



PLCC

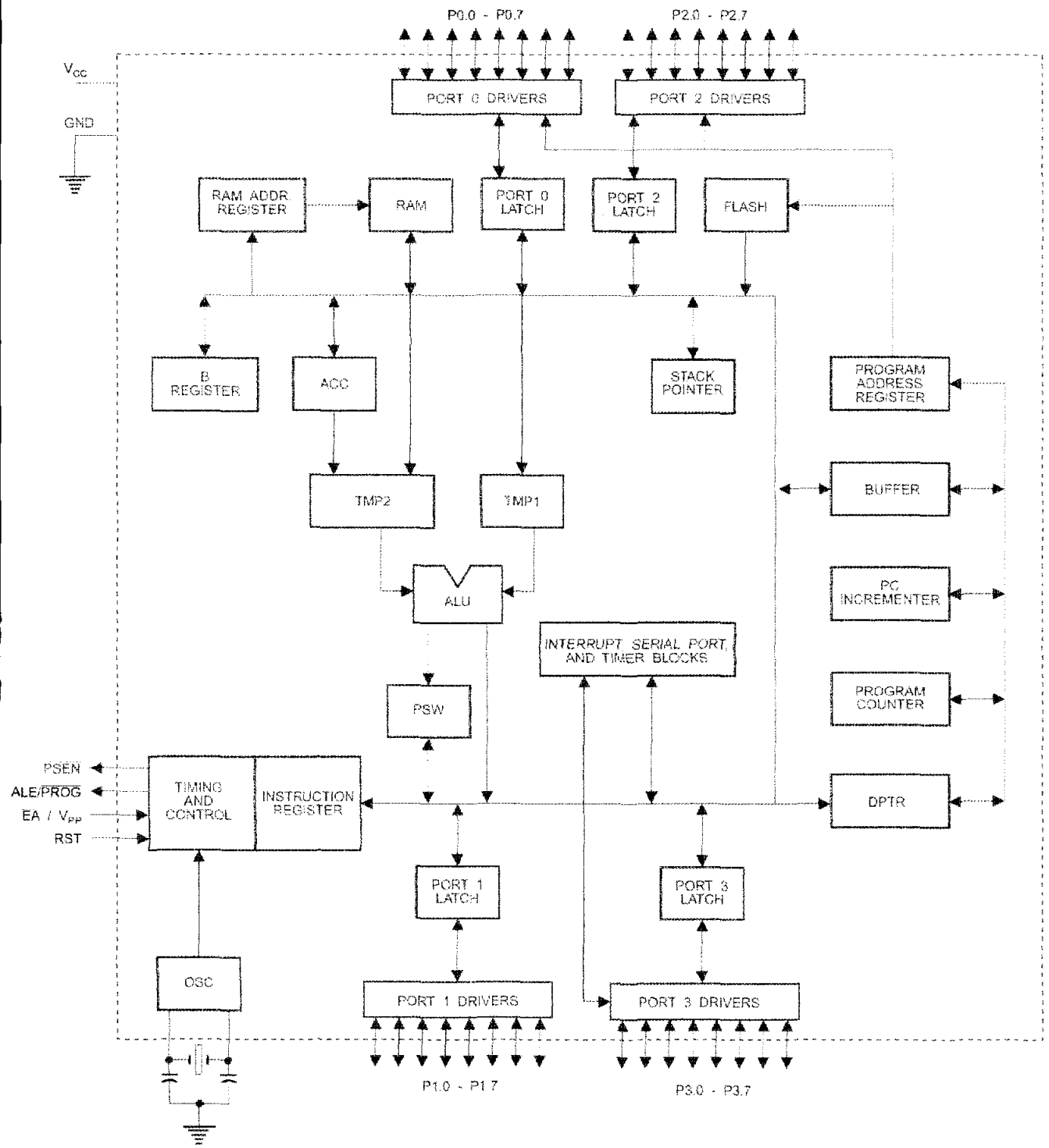


8-Bit Microcontroller with 4K Bytes Flash

AT89C51

0265F-A-12/97

lock Diagram



The AT89C51 provides the following standard features: 4K bytes of Flash, 128 bytes of RAM, 32 I/O lines, two 16-bit timer/counters, a five vector two-level interrupt architecture, a full duplex serial port, on-chip oscillator and clock circuitry. In addition, the AT89C51 is designed with static logic for operation down to zero frequency and supports two software selectable power saving modes. The Idle Mode stops the CPU while allowing the RAM, timer/counters, serial port and interrupt system to continue functioning. The Power Down Mode saves the RAM contents but freezes the oscillator disabling all other chip functions until the next hardware reset.

Pin Description

V_{CC}
Supply voltage.

GND
Ground.

Port 0
Port 0 is an 8-bit open drain bidirectional I/O port. As an output port each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high-impedance inputs.

Port 0 may also be configured to be the multiplexed low-order address/data bus during accesses to external program and data memory. In this mode P0 has internal pullups.

Port 0 also receives the code bytes during Flash programming, and outputs the code bytes during program verification. External pullups are required during program verification.

Port 1
Port 1 is an 8-bit bidirectional I/O port with internal pullups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}) because of the internal pullups.

Port 1 also receives the low-order address bytes during Flash programming and verification.

Port 2
Port 2 is an 8-bit bidirectional I/O port with internal pullups. The Port 2 output buffers can sink/source four TTL inputs. When 1s are written to Port 2 pins they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL}) because of the internal pullups.

Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application it uses strong internal pullups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

Port 3
Port 3 is an 8-bit bidirectional I/O port with internal pullups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}) because of the pullups.

Port 3 also serves the functions of various special features of the AT89C51 as listed below:

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

Port 3 also receives some control signals for Flash programming and verification.

RST
Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device.

ALE/$\overline{PROG}$
Address Latch Enable output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input ($\overline{PROG}$) during Flash programming.

In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external Data Memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

$\overline{PSEN}$
Program Store Enable is the read strobe to external program memory.

When the AT89C51 is executing code from external program memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external data memory.

$\overline{EA}$/V_{PP}
External Access Enable. $\overline{EA}$ must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed, $\overline{EA}$ will be internally latched on reset.

$\overline{EA}$ should be strapped to V_{CC} for internal program executions.

This pin also receives the 12-volt programming enable voltage (V_{PP}) during Flash programming, for parts that require 12-volt V_{PP}.

XTAL1
Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

XTAL2
Output from the inverting oscillator amplifier.

Oscillator Characteristics

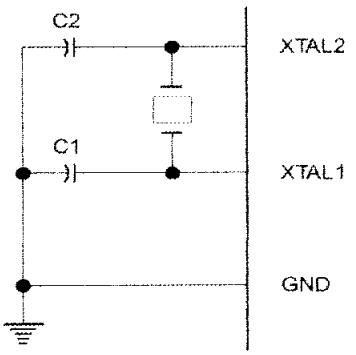
XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier which can be configured for use as an on-chip oscillator, as shown in Figure 1. Either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven as shown in Figure 2. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

Idle Mode

In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special functions registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

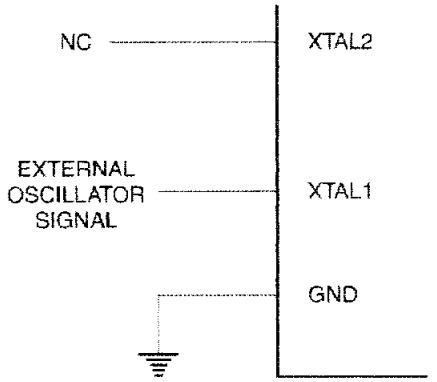
It should be noted that when idle is terminated by a hard ware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.

Figure 1. Oscillator Connections



Note: C1, C2 = 30 pF ± 10 pF for Crystals
= 40 pF ± 10 pF for Ceramic Resonators

Figure 2. External Clock Drive Configuration



Status of External Pins During Idle and Power Down Modes

Mode	Program Memory	ALE	$\overline{PSEN}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power Down	Internal	0	0	Data	Data	Data	Data
Power Down	External	0	0	Float	Data	Data	Data

Power Down Mode

In the power down mode the oscillator is stopped, and the instruction that invokes power down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the power down mode is terminated. The only exit from power down is a hardware reset. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

Program Memory Lock Bits

On the chip are three lock bits which can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in the table below:

When lock bit 1 is programmed, the logic level at the $\overline{EA}$ pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value, and holds that value until reset is activated. It is necessary that the latched value of $\overline{EA}$ be in agreement with the current logic level at that pin in order for the device to function properly.

Lock Bit Protection Modes

Program Lock Bits				Protection Type
	LB1	LB2	LB3	
1	U	U	U	No program lock features.
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, $\overline{EA}$ is sampled and latched on reset, and further programming of the Flash is disabled.
3	P	P	U	Same as mode 2, also verify is disabled.
4	P	P	P	Same as mode 3, also external execution is disabled.

Programming the Flash

The AT89C51 is normally shipped with the on-chip Flash memory array in the erased state (that is, contents = FFH) and ready to be programmed. The programming interface accepts either a high-voltage (12-volt) or a low-voltage (V_{CC}) program enable signal. The low voltage programming mode provides a convenient way to program the AT89C51 inside the user's system, while the high-voltage programming mode is compatible with conventional third party Flash or EPROM programmers.

The AT89C51 is shipped with either the high-voltage or low-voltage programming mode enabled. The respective top-side marking and device signature codes are listed in the following table.

	V_{PP} = 12V	V_{PP} = 5V
Top-Side Mark	AT89C51 xxxx yyww	AT89C51 xxxx-5 yyww
Signature	(030H)=1EH (031H)=51H (032H)=FFH	(030H)=1EH (031H)=51H (032H)=05H

The AT89C51 code memory array is programmed byte-by-byte in either programming mode. *To program any non-blank byte in the on-chip Flash Memory, the entire memory must be erased using the Chip Erase Mode.*

Programming Algorithm: Before programming the AT89C51, the address, data and control signals should be set up according to the Flash programming mode table and Figures 3 and 4. To program the AT89C51, take the following steps.

1. Input the desired memory location on the address lines.
2. Input the appropriate data byte on the data lines.
3. Activate the correct combination of control signals.
4. Raise $\overline{EA}/V_{PP}$ to 12V for the high-voltage programming mode.
5. Pulse ALE/$\overline{PROG}$ once to program a byte in the Flash array or the lock bits. The byte-write cycle is self-timed and typically takes no more than 1.5 ms. Repeat steps 1 through 5, changing the address and data for the entire array or until the end of the object file is reached.

$\overline{Data}$ Polling: The AT89C51 features $\overline{Data}$ Polling to indicate the end of a write cycle. During a write cycle, an attempted read of the last byte written will result in the complement of the written datum on PO.7. Once the write cycle has been completed, true data are valid on all outputs, and the next cycle may begin. $\overline{Data}$ Polling may begin any time after a write cycle has been initiated.

Ready/$\overline{Busy}$: The progress of byte programming can also be monitored by the RDY/$\overline{BSY}$ output signal. P3.4 is pulled low after ALE goes high during programming to indicate BUSY. P3.4 is pulled high again when programming is done to indicate READY.

Program Verify: If lock bits LB1 and LB2 have not been programmed, the programmed code data can be read back via the address and data lines for verification. The lock bits cannot be verified directly. Verification of the lock bits is achieved by observing that their features are enabled.

Chip Erase: The entire Flash array is erased electrically by using the proper combination of control signals and by holding ALE/$\overline{PROG}$ low for 10 ms. The code array is written with all "1"s. The chip erase operation must be executed before the code memory can be re-programmed.

Reading the Signature Bytes: The signature bytes are read by the same procedure as a normal verification of locations 030H,

031H, and 032H, except that P3.6 and P3.7 must be pulled to a logic low. The values returned are as follows.

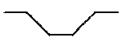
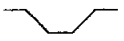
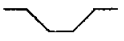
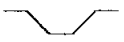
(030H) = 1EH indicates manufactured by Atmel
(031H) = 51H indicates 89C51
(032H) = FFH indicates 12V programming
(032H) = 05H indicates 5V programming

Programming Interface

Every code byte in the Flash array can be written and the entire array can be erased by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

All major programming vendors offer worldwide support for the Atmel microcontroller series. Please contact your local programming vendor for the appropriate software revision.

Flash Programming Modes

Mode		RST	$\overline{PSEN}$	ALE/$\overline{PROG}$	$\overline{EA}$/V_{PP}	P2.6	P2.7	P3.6	P3.7
Write Code Data		H	L		H/12V	L	H	H	H
Read Code Data		H	L	H	H	L	L	H	H
Write Lock	Bit - 1	H	L		H/12V	H	H	H	H
	Bit - 2	H	L		H/12V	H	H	L	L
	Bit - 3	H	L		H/12V	H	L	H	L
Chip Erase		H	L	 (1)	H/12V	H	L	L	L
Read Signature Byte		H	L	H	H	L	L	L	L

Note: 1. Chip Erase requires a 10-ms PROG pulse.

Figure 3. Programming the Flash

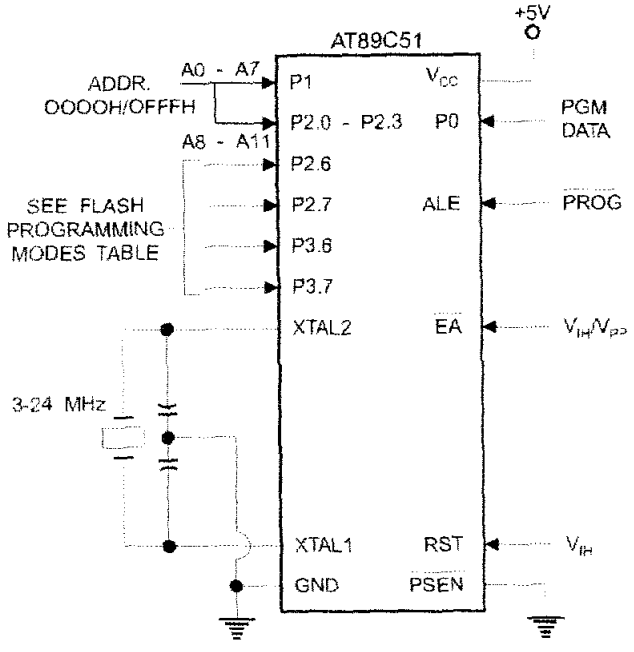
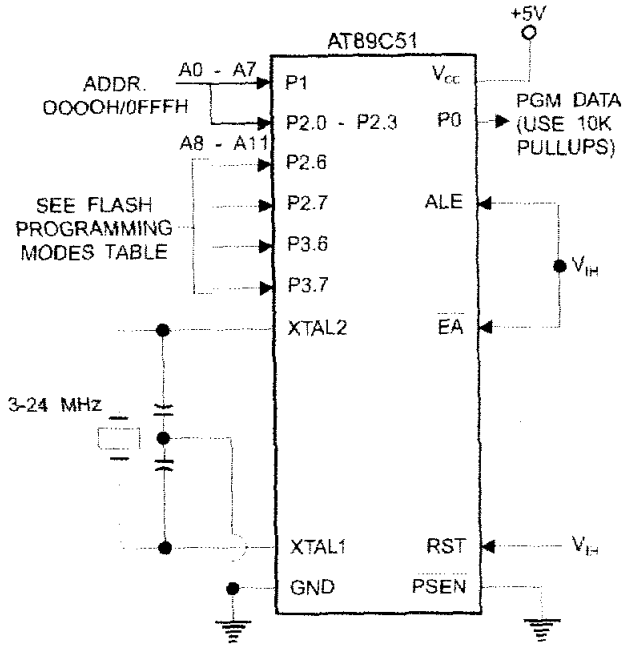


Figure 4. Verifying the Flash



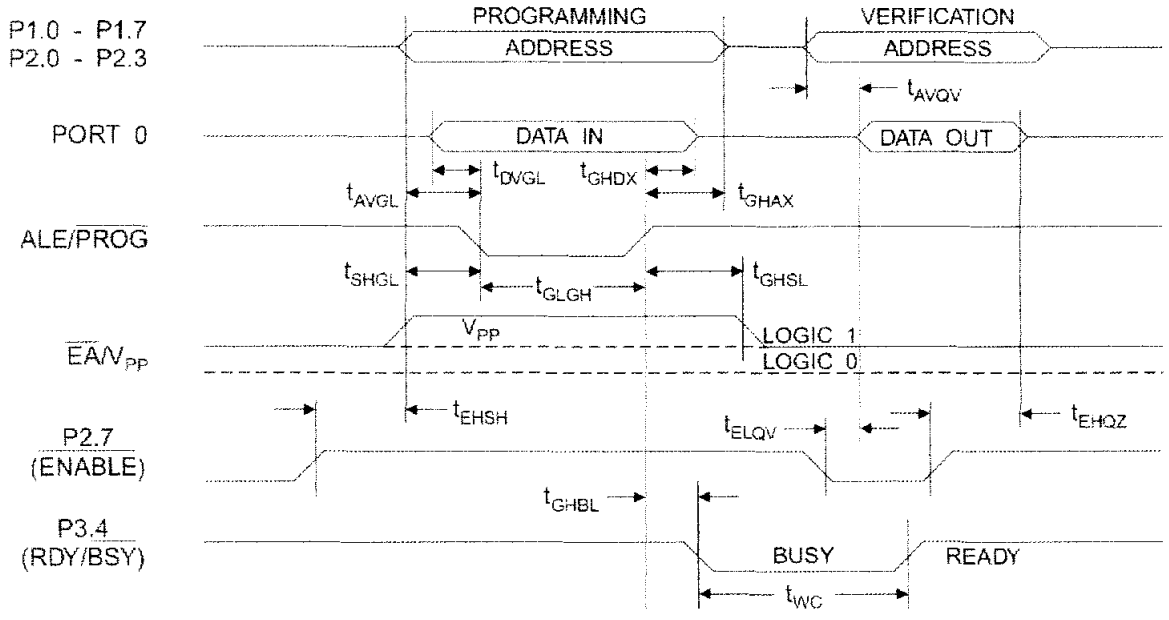
Flash Programming and Verification Characteristics

T_A = 0°C to 70°C, V_{CC} = 5.0 ± 10%

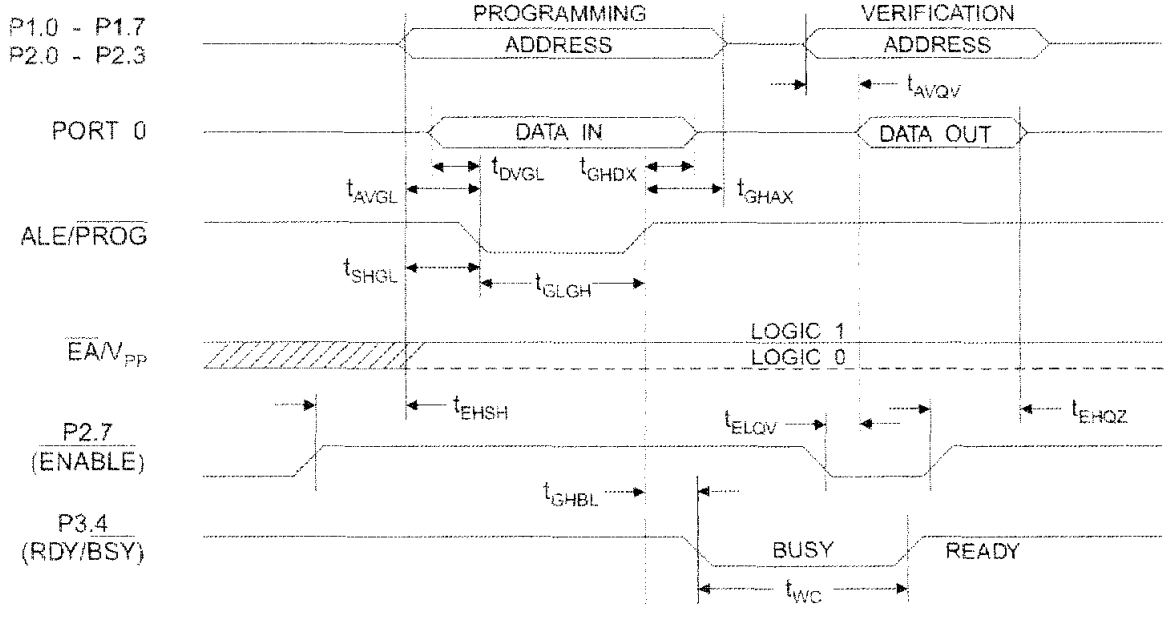
Symbol	Parameter	Min	Max	Units
V_{PP}(1)	Programming Enable Voltage	11.5	12.5	V
I_{PP}(1)	Programming Enable Current		1.0	mA
$1/t_{CLCL}$	Oscillator Frequency	3	24	MHz
t_{AVGL}	Address Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
t_{GHAX}	Address Hold After $\overline{PROG}$	$48t_{CLCL}$		
t_{DVGL}	Data Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
t_{GHDX}	Data Hold After $\overline{PROG}$	$48t_{CLCL}$		
t_{EHSH}	P2.7 ($\overline{ENABLE}$) High to V_{PP}	$48t_{CLCL}$		
t_{SHGL}	V_{PP} Setup to $\overline{PROG}$ Low	10		µs
t_{GHSL}(1)	V_{PP} Hold After $\overline{PROG}$	10		µs
t_{GLGH}	$\overline{PROG}$ Width	1	110	µs
t_{AVQV}	Address to Data Valid		$48t_{CLCL}$	
t_{ELQV}	$\overline{ENABLE}$ Low to Data Valid		$48t_{CLCL}$	
t_{EHQZ}	Data Float After $\overline{ENABLE}$	0	$48t_{CLCL}$	
t_{GHBL}	$\overline{PROG}$ High to $\overline{BUSY}$ Low		1.0	µs
t_{WC}	Byte Write Cycle Time		2.0	ms

Note: 1. Only used in 12-volt programming mode.

Flash Programming and Verification Waveforms - High Voltage Mode (V_{PP} = 12V)



Flash Programming and Verification Waveforms - Low Voltage Mode (V_{PP} = 5V)



Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0V to +7.0V
Maximum Operating Voltage	6.6V
DC Output Current	15.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_A = -40°C to 85°C, V_{CC} = 5.0V ± 20% (unless otherwise noted)

Symbol	Parameter	Condition	Min	Max	Units
V_{IL}	Input Low Voltage	(Except $\overline{EA}$)	-0.5	0.2 V_{CC} - 0.1	V
V_{IL1}	Input Low Voltage ($\overline{EA}$)		-0.5	0.2 V_{CC} - 0.3	V
V_{IH}	Input High Voltage	(Except XTAL1, RST)	0.2 V_{CC} + 0.9	V_{CC} + 0.5	V
V_{IH1}	Input High Voltage	(XTAL1, RST)	0.7 V_{CC}	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage[1] (Ports 1,2,3)	I_{OL} = 1.6 mA		0.45	V
V_{OL1}	Output Low Voltage[1] (Port 0, ALE, $\overline{PSEN}$)	I_{OL} = 3.2 mA		0.45	V
V_{OH}	Output High Voltage (Ports 1,2,3, ALE, $\overline{PSEN}$)	I_{OH} = -60 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -25 µA	0.75 V_{CC}		V
		I_{OH} = -10 µA	0.9 V_{CC}		V
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode)	I_{OH} = -800 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -300 µA	0.75 V_{CC}		V
		I_{OH} = -80 µA	0.9 V_{CC}		V
I_{IL}	Logical 0 Input Current (Ports 1,2,3)	V_{IN} = 0.45V		-50	µA
I_{TL}	Logical 1 to 0 Transition Current (Ports 1,2,3)	V_{IN} = 2V, VCC = 5V ± 10%		-650	µA
I_{LI}	Input Leakage Current (Port 0, $\overline{EA}$)	0.45 < V_{IN} < V_{CC}		±10	µA
RRST	Reset Pulldown Resistor		50	300	KΩ
C_{IO}	Pin Capacitance	Test Freq. = 1 MHz, T_A = 25°C		10	pF
I_{CC}	Power Supply Current	Active Mode, 12 MHz		20	mA
		Idle Mode, 12 MHz		5	mA
	Power Down Mode[2]	V_{CC} = 6V		100	µA
		V_{CC} = 3V		40	µA

Notes: 1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
Maximum I_{OL} per port pin: 10 mA
Maximum I_{OL} per 8-bit port: Port 0: 26 mA
Ports 1, 2, 3: 15 mA
Maximum total I_{OL} for all output pins: 71 mA
If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

2. Minimum V_{CC} for Power Down is 2V.

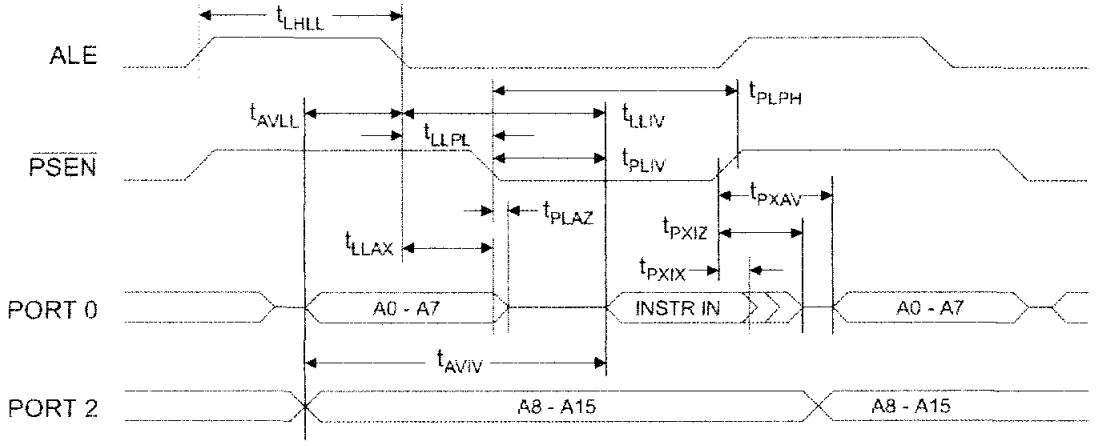
AC Characteristics

(Under Operating Conditions; Load Capacitance for Port 0, ALE/$\overline{PROG}$, and $\overline{PSEN}$ = 100 pF; Load Capacitance for all other outputs = 80 pF)

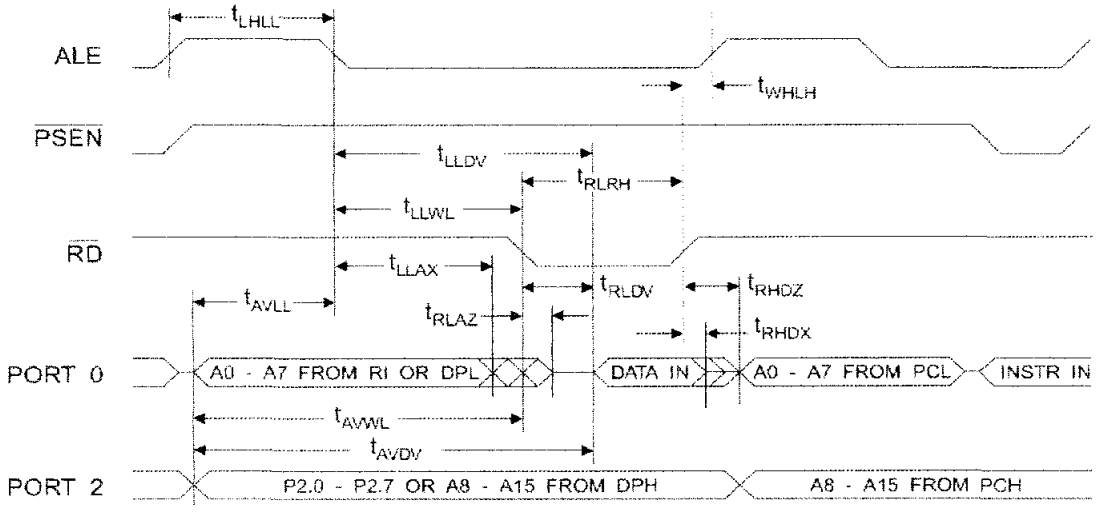
External Program and Data Memory Characteristics

Symbol	Parameter	12 MHz Oscillator		16 to 24 MHz Oscillator		Units
		Min	Max	Min	Max	
$1/t_{CLCL}$	Oscillator Frequency			0	24	MHz
t_{LHLL}	ALE Pulse Width	127		$2t_{CLCL}$-40		ns
t_{AVLL}	Address Valid to ALE Low	43		t_{CLCL}-13		ns
t_{LLAX}	Address Hold After ALE Low	48		t_{CLCL}-20		ns
t_{LLIV}	ALE Low to Valid Instruction In		233		$4t_{CLCL}$-65	ns
t_{LLPL}	ALE Low to $\overline{PSEN}$ Low	43		t_{CLCL}-13		ns
t_{PLPH}	$\overline{PSEN}$ Pulse Width	205		$3t_{CLCL}$-20		ns
t_{PLIV}	$\overline{PSEN}$ Low to Valid Instruction In		145		$3t_{CLCL}$-45	ns
t_{PXIX}	Input Instruction Hold After $\overline{PSEN}$	0		0		ns
t_{PXIZ}	Input Instruction Float After $\overline{PSEN}$		59		t_{CLCL}-10	ns
t_{PXAV}	$\overline{PSEN}$ to Address Valid	75		t_{CLCL}-8		ns
t_{AVIV}	Address to Valid Instruction In		312		$5t_{CLCL}$-55	ns
t_{PLAZ}	$\overline{PSEN}$ Low to Address Float		10		10	ns
t_{RLRH}	$\overline{RD}$ Pulse Width	400		$6t_{CLCL}$-100		ns
t_{WLWH}	$\overline{WR}$ Pulse Width	400		$6t_{CLCL}$-100		ns
t_{RLDV}	$\overline{RD}$ Low to Valid Data In		252		$5t_{CLCL}$-90	ns
t_{RHDX}	Data Hold After $\overline{RD}$	0		0		ns
t_{RHDZ}	Data Float After $\overline{RD}$		97		$2t_{CLCL}$-28	ns
t_{LLDV}	ALE Low to Valid Data In		517		$8t_{CLCL}$-150	ns
t_{AVDV}	Address to Valid Data In		585		$9t_{CLCL}$-165	ns
t_{LLWL}	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	200	300	$3t_{CLCL}$-50	$3t_{CLCL}$+50	ns
t_{AVWL}	Address to $\overline{RD}$ or $\overline{WR}$ Low	203		$4t_{CLCL}$-75		ns
t_{QVWX}	Data Valid to $\overline{WR}$ Transition	23		t_{CLCL}-20		ns
t_{QVWH}	Data Valid to $\overline{WR}$ High	433		$7t_{CLCL}$-120		ns
t_{WHQX}	Data Hold After $\overline{WR}$	33		t_{CLCL}-20		ns
t_{RLAZ}	$\overline{RD}$ Low to Address Float		0		0	ns
t_{WHLH}	$\overline{RD}$ or $\overline{WR}$ High to ALE High	43	123	t_{CLCL}-20	t_{CLCL}+25	ns

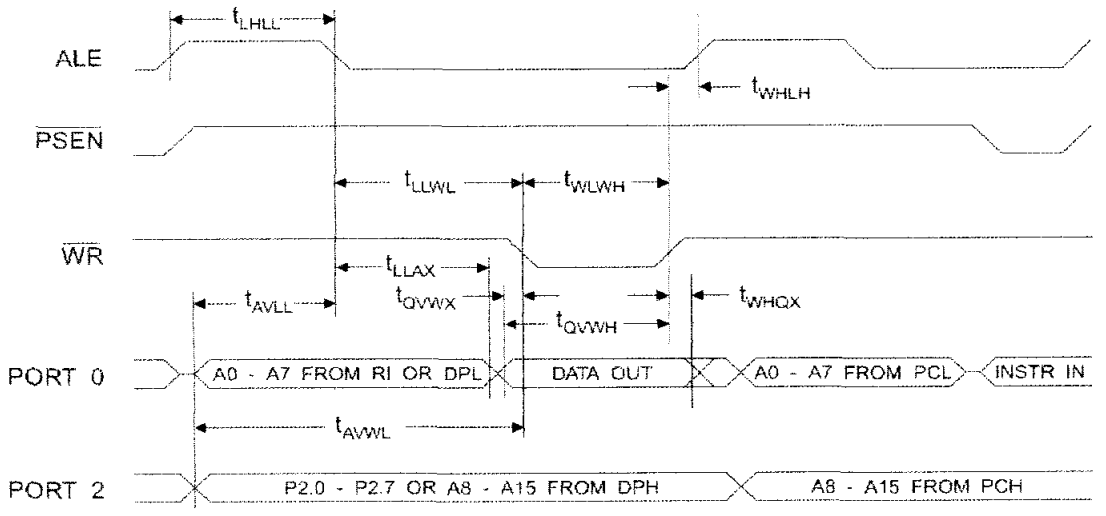
External Program Memory Read Cycle



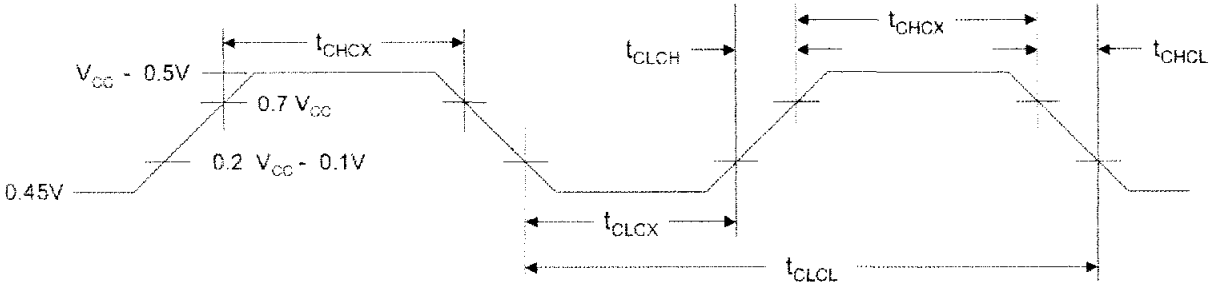
External Data Memory Read Cycle



External Data Memory Write Cycle



External Clock Drive Waveforms



External Clock Drive

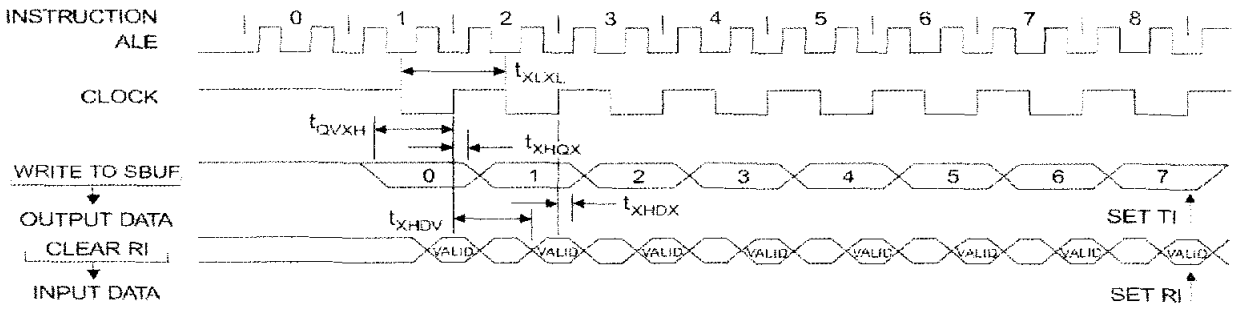
Symbol	Parameter	Min	Max	Units
$1/t_{CLCL}$	Oscillator Frequency	0	24	MHz
t_{CLCL}	Clock Period	41.6		ns
t_{CHCX}	High Time	15		ns
t_{CLCX}	Low Time	15		ns
t_{CLCH}	Rise Time		20	ns
t_{CHCL}	Fall Time		20	ns

Serial Port Timing: Shift Register Mode Test Conditions

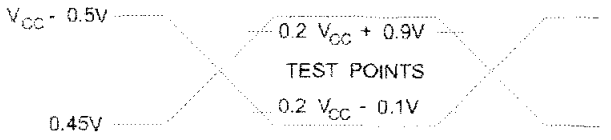
(V_{CC} = 5.0 V ± 20%; Load Capacitance = 80 pF)

Symbol	Parameter	12 MHz Osc		Variable Oscillator		Units
		Min	Max	Min	Max	
t_{XLXL}	Serial Port Clock Cycle Time	1.0		$12t_{CLCL}$		µs
t_{QVXH}	Output Data Setup to Clock Rising Edge	700		$10t_{CLCL}$-133		ns
t_{XHQX}	Output Data Hold After Clock Rising Edge	50		$2t_{CLCL}$-117		ns
t_{XHDX}	Input Data Hold After Clock Rising Edge	0		0		ns
t_{XHDV}	Clock Rising Edge to Input Data Valid		700		$10t_{CLCL}$-133	ns

Shift Register Mode Timing Waveforms

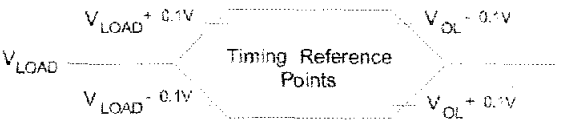


AC Testing Input/Output Waveforms(1)



Note: 1. AC Inputs during testing are driven at V_{CC} - 0.5V for a logic 1 and 0.45V for a logic 0. Timing measurements are made at V_{IH} min. for a logic 1 and V_{IL} max. for a logic 0.

Float Waveforms(1)



Note: 1. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when 100 mV change from the loaded V_{OH}/V_{OL} level occurs.

Ordering Information

Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
12	5V ± 20%	AT89C51-12AC	44A	Commercial
		AT89C51-12JC	44J	(0°C to 70°C)
		AT89C51-12PC	40P6	
		AT89C51-12QC	44Q	
		AT89C51-12AI	44A	Industrial
		AT89C51-12JI	44J	(-40°C to 85°C)
		AT89C51-12PI	40P6	
		AT89C51-12QI	44Q	
		AT89C51-12AA	44A	Automotive
		AT89C51-12JA	44J	(-40°C to 105°C)
		AT89C51-12PA	40P6	
		AT89C51-12QA	44Q	
16	5V ± 20%	AT89C51-16AC	44A	Commercial
		AT89C51-16JC	44J	(0°C to 70°C)
		AT89C51-16PC	40P6	
		AT89C51-16QC	44Q	
		AT89C51-16AI	44A	Industrial
		AT89C51-16JI	44J	(-40°C to 85°C)
		AT89C51-16PI	40P6	
		AT89C51-16QI	44Q	
		AT89C51-16AA	44A	Automotive
		AT89C51-16JA	44J	(-40°C to 105°C)
		AT89C51-16PA	40P6	
		AT89C51-16QA	44Q	
20	5V ± 20%	AT89C51-20AC	44A	Commercial
		AT89C51-20JC	44J	(0°C to 70°C)
		AT89C51-20PC	40P6	
		AT89C51-20QC	44Q	
		AT89C51-20AI	44A	Industrial
		AT89C51-20JI	44J	(-40°C to 85°C)
		AT89C51-20PI	40P6	
		AT89C51-20QI	44Q	

Ordering Information

Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
24	5V ± 20%	AT89C51-24AC	44A	Commercial
		AT89C51-24JC	44J	(0°C to 70°C)
		AT89C51-24PC	44P6	
		AT89C51-24QC	44Q	
		AT89C51-24AI	44A	Industrial
		AT89C51-24JI	44J	(-40°C to 85°C)
		AT89C51-24PI	44P6	
		AT89C51-24QI	44Q	

	Package Type
44A	44 Lead, Thin Plastic Gull Wing Quad Flatpack (TQFP)
44J	44 Lead, Plastic J-Leaded Chip Carrier (PLCC)
40P6	40 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
44Q	44 Lead, Plastic Gull Wing Quad Flatpack (PQFP)

19-0381; Rev 2; 9/01

EVALUATION KIT MANUAL AVAILABLE

MAXIM

Multi-Range (±10V, ±5V, +10V, +5V), Single +5V, 12-Bit DAS with 8+4 Bus Interface

General Description

The MAX197 multi-range, 12-bit data-acquisition system (DAS) requires only a single +5V supply for operation, yet accepts signals at its analog inputs that may span both above the power-supply rail and below ground. This system provides 8 analog input channels that are independently software programmable for a variety of ranges: ±10V, ±5V, 0V to +10V, or 0V to +5V. This increases effective dynamic range to 14 bits, and provides the user flexibility to interface 4mA-to-20mA, ±12V, and ±15V powered sensors to a single +5V system. In addition, the converter is overvoltage tolerant to ±16.5V; a fault condition on any channel does **not** affect the conversion result of the selected channel. Other features include a 5MHz bandwidth track/hold, a 100ksps throughput rate, software-selectable internal or external clock and acquisition, 8+4 parallel interface, and an internal 4.096V or an external reference.

A hardware $\overline{SHDN}$ pin and two programmable power-down modes (STBYPD, FULLPD) are provided for low-current shutdown between conversions. In STBYPD mode, the reference buffer remains active, eliminating start-up delays.

The MAX197 employs a standard microprocessor (µP) interface. A three-state data I/O port is configured to operate with 8-bit data buses, and data-access and bus-release timing specifications are compatible with most popular µPs. All logic inputs and outputs are TTL/CMOS compatible.

The MAX197 is available in 28-pin DIP, wide SO, SSOP, and ceramic SB packages.

For a different combination of ranges (±4V, ±2V, 0V to 4V, 0V to 2V), refer to the MAX199 data sheet. For 12-bit bus interface, refer to the MAX196 and MAX198 data sheets.

Applications

Industrial-Control Systems
Robotics
Data-Acquisition Systems
Automatic Testing Systems
Medical Instruments
Telecommunications

Functional Diagram appears at end of data sheet.

Features

- **12-Bit Resolution, 1/2LSB Linearity**
- **Single +5V Operation**
- **Software-Selectable Input Ranges: ±10V, ±5V, 0V to 10V, 0V to 5V**
- **Fault-Protected Input Multiplexer (±16.5V)**
- **8 Analog Input Channels**
- **6µs Conversion Time, 100ksps Sampling Rate**
- **Internal or External Acquisition Control**
- **Internal 4.096V or External Reference**
- **Two Power-Down Modes**
- **Internal or External Clock**

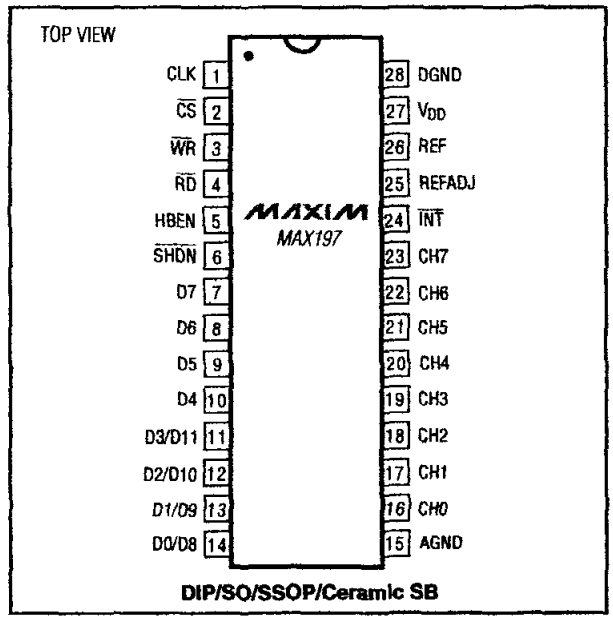
Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX197ACNI	0°C to +70°C	28 Narrow Plastic DIP
MAX197BCNI	0°C to +70°C	28 Narrow Plastic DIP
MAX197ACWI	0°C to +70°C	28 Wide SO
MAX197BCWI	0°C to +70°C	28 Wide SO
MAX197ACAI	0°C to +70°C	28 SSOP
MAX197BCAI	0°C to +70°C	28 SSOP
MAX197BC/D	0°C to +70°C	Dice*

Ordering Information continued at end of data sheet.

*Dice are specified at T_A = +25°C, DC parameters only.

Pin Configuration



DIP/SO/SSOP/Ceramic SB

Multi-Range (±10V, ±5V, +10V, +5V), Single +5V, 12-Bit DAS with 8+4 Bus Interface

ABSOLUTE MAXIMUM RATINGS

V_{DD} to AGND ..... -0.3V to +7V
AGND to DGND ..... -0.3V to +0.3V
REF to AGND ..... -0.3V to (V_{DD} + 0.3V)
REFADJ to AGND ..... -0.3V to (V_{DD} + 0.3V)
Digital Inputs to DGND ..... -0.3V to (V_{DD} + 0.3V)
Digital Outputs to DGND ..... -0.3V to (V_{DD} + 0.3V)
CH0–CH7 to AGND ..... ±16.5V
Continuous Power Dissipation (T_A = +70°C)
Narrow Plastic DIP (derate 14.29mW/°C above +70°C) 1143mW
Wide SO (derate 12.50mW/°C above +70°C) 1000mW
SSOP (derate 9.52mW/°C above +70°C) 762mW
Narrow Ceramic SB (derate 20.00mW/°C above +70°C)..1600mW

Operating Temperature Ranges
MAX197_C_ _ ..... 0°C to +70°C
MAX197_E_ _ ..... -40°C to +85°C
MAX197_M_ _ ..... -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (soldering, 10s) ..... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 5V ±5%; unipolar/bipolar range; external reference mode, V_{REF} = 4.096V; 4.7µF at REF pin; external clock, f_{CLK} = 2.0MHz with 50% duty cycle; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ACCURACY (Note 1)							
Resolution				12			Bits
Integral Nonlinearity	INL	MAX197A				±1/2	LSB
		MAX197B				±1	
Differential Nonlinearity	DNL					±1	LSB
Offset Error		Unipolar	MAX197A			±3	LSB
			MAX197B			±5	
		Bipolar	MAX197A			±5	
			MAX197B			±10	
Channel-to-Channel Offset Error Matching		Unipolar			±0.1		LSB
		Bipolar			±0.5		
Gain Error (Note 2)		Unipolar	MAX197A			±7	LSB
			MAX197B			±10	
		Bipolar	MAX197A			±7	
			MAX197B			±10	
Gain Temperature Coefficient (Note 2)		Unipolar			3		ppm/°C
		Bipolar			5		
DYNAMIC SPECIFICATIONS (10kHz sine-wave input, ±10Vp-p, f_{SAMPLE} = 100ksps)							
Signal-to-Noise + Distortion Ratio	SINAD		MAX197A	70			dB
			MAX197B	69			
Total Harmonic Distortion	*THD*	*Up to the 5th harmonic*			-85	-78	dB
Spurious-Free Dynamic Range	SFDR			80			dB
Channel-to-Channel Crosstalk		50kHz, V_{IN} = ±5V (Note 3)			-86		dB
Aperture Delay		External CLK mode/external acquisition control			15		ns
Aperture Jitter		External CLK mode/external acquisition control			<50		ps
		Internal CLK mode/internal acquisition control (Note 4)			10		ns

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 5V ±5%; unipolar/bipolar range; external reference mode, V_{REF} = 4.096V; 4.7µF at REF pin; external clock, f_{CLK} = 2.0MHz with 50% duty cycle; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ANALOG INPUT							
Track/Hold Acquisition Time		f_{CLK} = 2.0MHz				3	µs
Small-Signal Bandwidth		-3dB rolloff	±10V range		5		MHz
			±5V range		2.5		
			0V to 10V range		2.5		
			0V to 5V range		1.25		
Input Voltage Range (See Table 1)		Unipolar		0		10	V
				0		5	
		Bipolar		-10		10	
				-5		5	
Input Current		Unipolar	0V to 10V range			720	µA
			0V to 5V range			360	
		Bipolar	-10V to 10V range	-1200		720	
			-5V to 5V range	-600		360	
Input Dynamic Resistance		Unipolar			21		kΩ
		Bipolar			16		
Input Capacitance		(Note 5)				40	pF
INTERNAL REFERENCE							
REF Output Voltage	V_{REF}	T_A = +25°C		4.076	4.096	4.116	V
REF Output Tempco	TC V_{REF}				40		ppm/°C
Output Short-Circuit Current						30	mA
Load Regulation		0mA to 0.5mA output current (Note 6)				7.5	mV
Capacitive Bypass at REF				4.7			µF
REFADJ Output Voltage				2.465	2.500	2.535	V
REFADJ Adjustment Range		With recommended circuit (Figure 1)			±1.5		%
Buffer Voltage Gain					1.6384		V/V
REFERENCE INPUT (Buffer disabled, reference input applied to REF pin)							
Input Voltage Range				2.4		4.18	V
Input Current		V_{REF} = 4.18V	Normal or STANDBY power-down mode			400	µA
			FULL power-down mode			1	
Input Resistance		Normal or STANDBY power-down mode		10			kΩ
		FULL power-down mode		5			MΩ
REFADJ Threshold for Buffer Disable				V_{DD} - 50mV			V

Multi-Range (±10V, ±5V, +10V, +5V), Single +5V, 12-Bit DAS with 8+4 Bus Interface

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 5V ±5%; unipolar/bipolar range; external reference mode, V_{REF} = 4.096V; 4.7µF at REF pin; external clock, f_{CLK} = 2.0MHz with 50% duty cycle; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER REQUIREMENTS							
Supply Voltage	V_{DD}			4.75		5.25	V
Supply Current	I_{DD}	Normal mode, bipolar ranges				18	mA
		Normal mode, unipolar ranges			6	10	
		Standby power-down (STBYPD)			700	850	µA
		Full power-down mode (FULLPD) (Note 7)				120	
Power-Supply Rejection Ratio (Note 8)	PSRR	External reference = 4.096V				±1/2	LSB
		Internal reference			±1/2		
TIMING							
Internal Clock Frequency	f_{CLK}	C_{CLK} = 100pF		1.25	1.56	2.00	MHz
External Clock Frequency Range	f_{CLK}			0.1		2.0	MHz
Acquisition Time	t_{ACQI}	Internal acquisition	External CLK	3.0			µs
			Internal CLK	3.0		5.0	
	t_{ACQE}	External acquisition (Note 9)		3.0			
		After FULLPD or STBYPD			5		
Conversion Time	t_{CONV}	External CLK		6.0			µs
		Internal CLK, C_{CLK} = 100pF		6.0	7.7	10.0	
Throughput Rate		External CLK				100	ksps
		Internal CLK, C_{CLK} = 100pF		62			
Bandgap Reference Start-Up Time		Power-up (Note 10)			200		µs
Reference Buffer Settling		To 0.1mV REF bypass capacitor fully discharged	C_{REF} = 4.7µF		8		ms
			C_{REF} = 33µF		60		
DIGITAL INPUTS (D7–D0, CLK, $\overline{RD}$, $\overline{WR}$, $\overline{CS}$, HBEN, $\overline{SHDN}$) (Note 11)							
Input High Voltage	V_{INH}			2.4			V
Input Low Voltage	V_{INL}					0.8	V
Input Leakage Current	I_{IN}	V_{IN} = 0V or V_{DD}				±10	µA
Input Capacitance	C_{IN}	(Note 5)				15	pF
DIGITAL OUTPUTS (D7–D4, D3/D11, D2/D10, D1/D9, D0/D8, $\overline{INT}$)							
Output Low Voltage	V_{OL}	V_{DD} = 4.75V, I_{SINK} = 1.6mA				0.4	V
Output High Voltage	V_{OH}	V_{DD} = 4.75V, I_{SOURCE} = 1mA		V_{DD} - 1			V
Three-State Output Capacitance	C_{OUT}	(Note 5)				15	pF

TIMING CHARACTERISTICS

(V_{DD} = 5V ±5%; unipolar/bipolar range; external reference mode, V_{REF} = 4.096V; 4.7µF at REF pin; external clock, f_{CLK} = 2.0MHz with 50% duty cycle; T_A = T_{MIN} to T_{MAX}, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{CS}$ Pulse Width	t_{CS}		80			ns
$\overline{WR}$ Pulse Width	t_{WR}		80			ns
$\overline{CS}$ to $\overline{WR}$ Setup Time	t_{CSWS}		0			ns
$\overline{CS}$ to $\overline{WR}$ Hold Time	t_{CSWH}		0			ns
$\overline{CS}$ to $\overline{RD}$ Setup Time	t_{CSRS}		0			ns
$\overline{CS}$ to $\overline{RD}$ Hold Time	t_{CSRH}		0			ns
CLK to $\overline{WR}$ Setup Time	t_{CWS}				100	ns
CLK to $\overline{WR}$ Hold Time	t_{CWH}				50	ns
Data Valid to $\overline{WR}$ Setup	t_{DS}		60			ns
Data Valid to $\overline{WR}$ Hold	t_{DH}		0			ns
$\overline{RD}$ Low to Output Data Valid	t_{DO}	Figure 2, C_L = 100pF (Note 12)			120	ns
HBEN High or HBEN Low to Output Valid	t_{DO1}	Figure 2, C_L = 100pF (Note 12)			120	ns
$\overline{RD}$ High to Output Disable	t_{TR}	(Note 13)			70	ns
$\overline{RD}$ Low to $\overline{INT}$ High Delay	t_{INT1}				120	ns

Note 1: Accuracy specifications tested at V_{DD} = 5.0V. Performance at power-supply tolerance limits guaranteed by Power-Supply Rejection test. Tested for the ±10V input range.

Note 2: External reference: V_{REF} = 4.096V, offset error nulled, ideal last code transition = FS - 3/2LSB.

Note 3: Ground "on" channel; sine wave applied to all "off" channels.

Note 4: Maximum full-power input frequency for 1LSB error with 10ns jitter = 3kHz.

Note 5: Guaranteed by design. Not tested.

Note 6: *Use static loads only.*

Note 7: Tested using internal reference.

Note 8: PSRR measured at full-scale.

Note 9: External acquisition timing: starts at data valid at ACQMOD = low control byte; ends at rising edge of $\overline{WR}$ with ACQMOD = high control byte.

Note 10: Not subject to production testing. Provided for design guidance only.

Note 11: All input control signals specified with t_R = t_F = 5ns from a voltage level of 0.8V to 2.4V.

Note 12: t_{DO} and t_{DO1} are measured with the load circuits of Figure 2 and defined as the time required for an output to cross 0.8V or 2.4V.

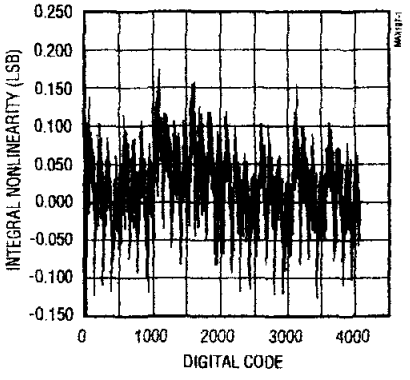
Note 13: t_{TR} is defined as the time required for the data lines to change by 0.5V.

Multi-Range (±10V, ±5V, +10V, +5V), Single +5V, 12-Bit DAS with 8+4 Bus Interface

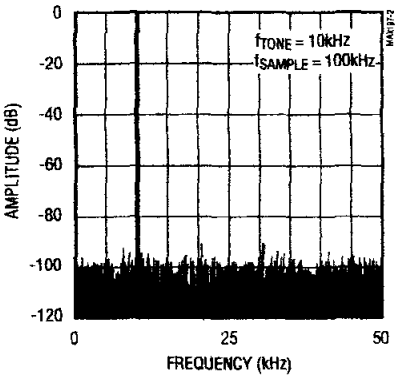
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

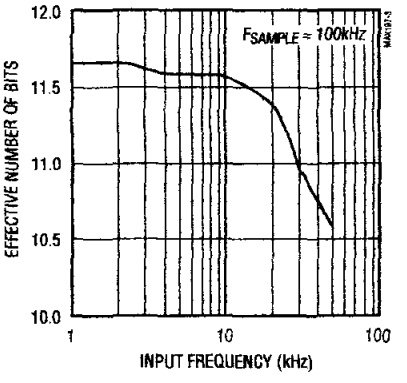
INTEGRAL NONLINEARITY vs. DIGITAL CODE



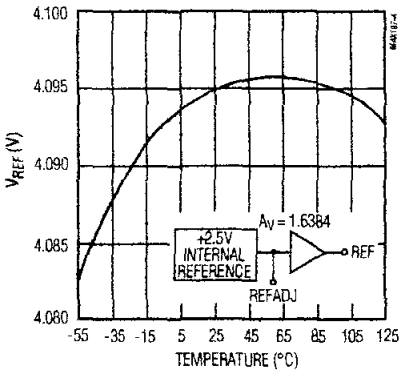
FFT PLOT



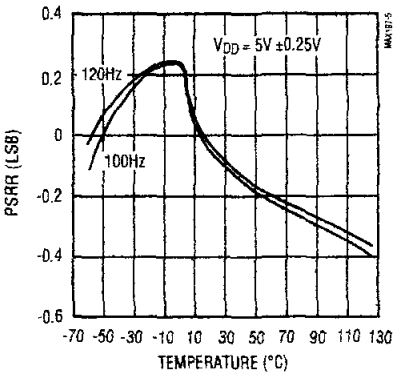
EFFECTIVE NUMBER OF BITS vs. INPUT FREQUENCY



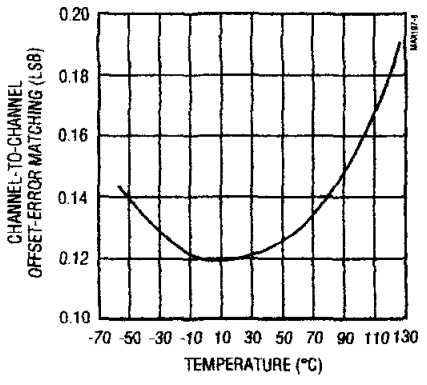
REFERENCE OUTPUT VOLTAGE (V_{REF}) vs. TEMPERATURE



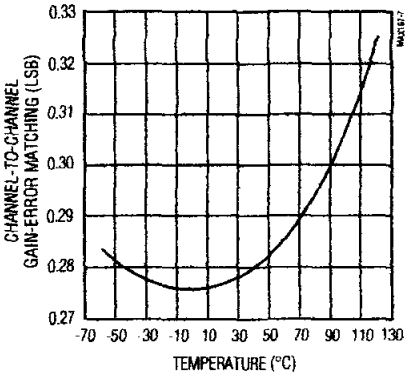
POWER-SUPPLY REJECTION RATIO vs. TEMPERATURE



CHANNEL-TO-CHANNEL OFFSET-ERROR MATCHING vs. TEMPERATURE



CHANNEL-TO-CHANNEL GAIN-ERROR MATCHING vs. TEMPERATURE



Pin Description

PIN	NAME	FUNCTION
1	CLK	Clock Input. In external clock mode, drive CLK with a TTL/CMOS compatible clock. In internal clock mode, place a capacitor from this pin to ground to set the internal clock frequency; f_{CLK} = 1.56MHz typical with C_{CLK} = 100pF.
2	$\overline{CS}$	Chip Select, active low.
3	$\overline{WR}$	When $\overline{CS}$ is low, in the internal acquisition mode, a rising edge on $\overline{WR}$ latches in configuration data and starts an acquisition plus a conversion cycle. When $\overline{CS}$ is low, in the external acquisition mode, the first rising edge on $\overline{WR}$ starts an acquisition and a second rising edge on $\overline{WR}$ ends acquisition and starts a conversion cycle.
4	$\overline{RD}$	If $\overline{CS}$ is low, a falling edge on $\overline{RD}$ will enable a read operation on the data bus.
5	HBEN	Used to multiplex the 12-bit conversion result. When high, the 4 MSBs are multiplexed on the data bus; when low, the 8 LSBs are available on the bus.
6	$\overline{SHDN}$	Shutdown. Puts the device into full power-down (FULLPD) mode when pulled low.
7–10	D7–D4	Three-State Digital I/O
11	D3/D11	Three-State Digital I/O. D3 output (HBEN = low), D11 output (HBEN = high).
12	D2/D10	Three-State Digital I/O. D2 output (HBEN = low), D10 output (HBEN = high).
13	D1/D9	Three-State Digital I/O. D1 output (HBEN = low), D9 output (HBEN = high).
14	D0/D8	Three-State Digital I/O. D0 output (HBEN = low), D8 output (HBEN = high). D0 = LSB.
15	AGND	Analog Ground
16–23	CH0–CH7	Analog Input Channels
24	$\overline{INT}$	$\overline{INT}$ goes low when conversion is complete and output data is ready.
25	REFADJ	Bandgap Voltage-Reference Output/External Adjust Pin. Bypass with a 0.01µF capacitor to AGND. Connect to V_{DD} when using an external reference at the REF pin.
26	REF	Reference Buffer Output/ADC Reference Input. In internal reference mode, the reference buffer provides a 4.096V nominal output, externally adjustable at REFADJ. In external reference mode, disable the internal buffer by pulling REFADJ to V_{DD}.
27	V_{DD}	+5V Supply. Bypass with 0.1µF capacitor to AGND.
28	DGND	Digital Ground

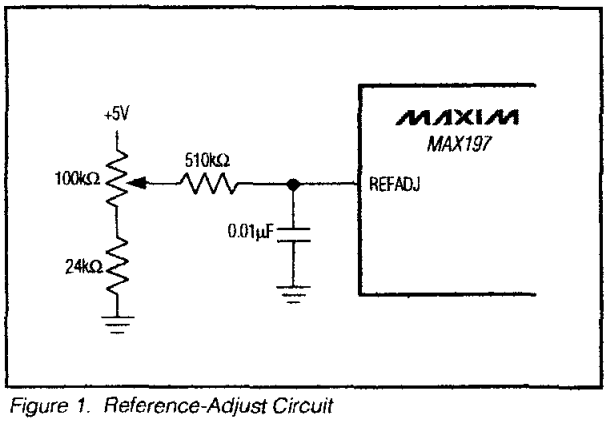


Figure 1. Reference-Adjust Circuit

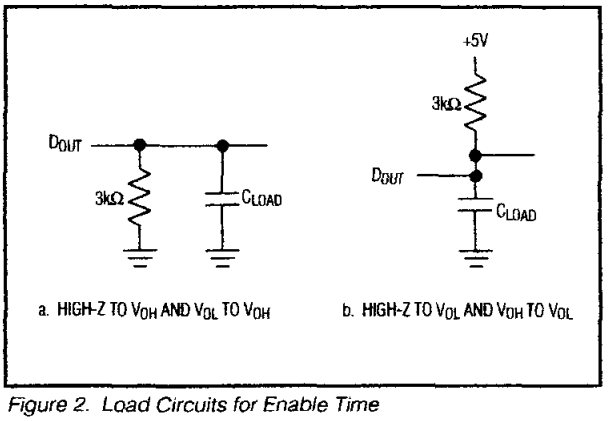


Figure 2. Load Circuits for Enable Time

Multi-Range (±10V, ±5V, +10V, +5V), Single +5V, 12-Bit DAS with 8+4 Bus Interface

Detailed Description

Converter Operation

The MAX197, a multi-range, fault-tolerant ADC, uses successive approximation and internal input track/hold (T/H) circuitry to convert an analog signal to a 12-bit digital output. The parallel-output format provides easy interface to microprocessors (µPs). Figure 3 shows the MAX197 in its simplest operational configuration.

Analog-Input Track/Hold

In the internal acquisition control mode (control bit D5 set to 0), the T/H enters its tracking mode on $\overline{WR}$'s rising edge, and enters its hold mode when the internally timed (6 clock cycles) acquisition interval ends. A low impedance input source, which settles in less than 1.5µs, is required to maintain conversion accuracy at the maximum conversion rate.

In the external acquisition control mode (D5 = 1), the T/H enters its tracking mode on the first $\overline{WR}$ rising edge and enters its hold mode when it detects the second $\overline{WR}$ rising edge with D5 = 0. See the *External Acquisition* section.

Input Bandwidth

The ADC's input tracking circuitry has a 5MHz small-signal bandwidth. When using the internal acquisition mode with an external clock frequency of 2MHz, a 100ksps throughput rate can be achieved. It is possible to digitize high-speed transient events and measure periodic signals with bandwidths exceeding the ADC's sampling rate by using undersampling techniques. To avoid high-frequency signals being aliased into the frequency band of interest, anti-alias filtering is recommended (MAX274/MAX275 continuous-time filters).

Input Range and Protection

Figure 4 shows the equivalent input circuit. With V_{REF} = 4.096V, the MAX197 can be programmed for input ranges of ±10V, ±5V, 0V to 10V, or 0V to 5V by setting the appropriate control bits (D3, D4) in the control byte (see Tables 2 and 3). The full-scale input voltage depends on the voltage at REF (Table 1). When an external reference is applied at REFADJ, the voltage at REF is given by $V_{REF} = 1.6384 \times V_{REFADJ}$ (2.4V < V_{REF} < 4.18V).

Table 1. Full Scale and Zero Scale

RANGE (V)	ZERO SCALE (V)	-FULL SCALE	+FULL SCALE
0 to 5	0	—	V_{REF} x 1.2207
0 to 10	0	—	V_{REF} x 2.4414
±5	—	-V_{REF} x 1.2207	V_{REF} x 1.2207
±10	—	-V_{REF} x 2.4414	V_{REF} x 2.4414

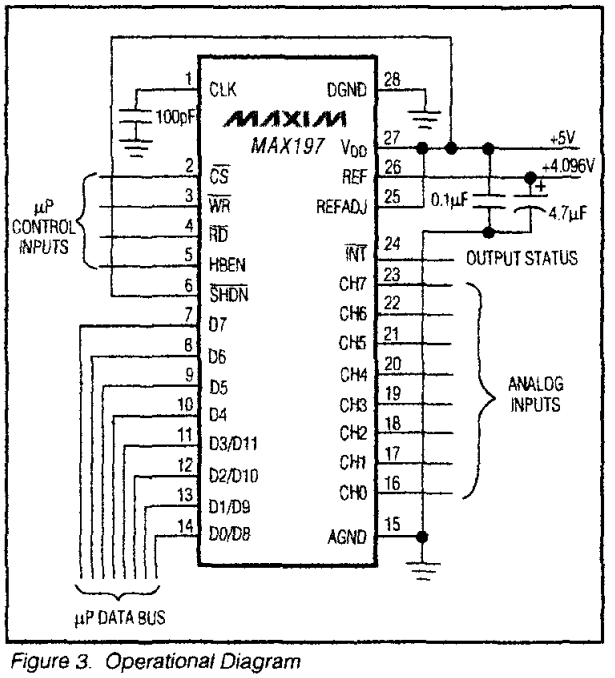


Figure 3. Operational Diagram

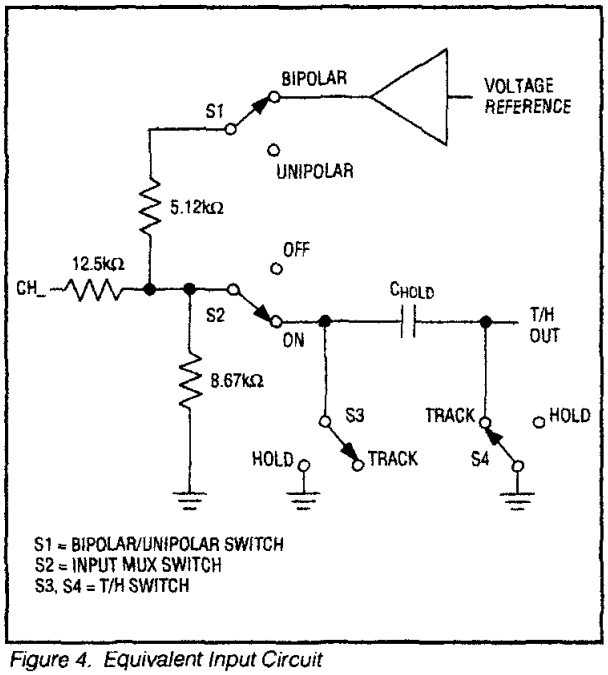


Figure 4. Equivalent Input Circuit

Multi-Range (±10V, ±5V, +10V, +5V), Single +5V, 12-Bit DAS with 8+4 Bus Interface

The input channels are overvoltage protected to ±16.5V. This protection is active even if the device is in power-down mode.

Even with V_{DD} = 0V, the input resistive network provides current-limiting that adequately protects the device.

Digital Interface

Input data (control byte) and output data are multiplexed on a three-state parallel interface. This parallel I/O can easily be interfaced with a µP. $\overline{CS}$, $\overline{WR}$, and $\overline{RD}$ control the write and read operations. $\overline{CS}$ is the standard chip-select signal, which enables a µP to address the MAX197 as an I/O port. When high, it disables the $\overline{WR}$ and $\overline{RD}$ inputs and forces the interface into a high-Z state.

Input Format

The control byte is latched into the device, on pins D7–D0, during a write cycle. Table 2 shows the control-byte format.

Output Data Format

The output data format is binary in unipolar mode and twos-complement binary in bipolar mode. When reading the output data, $\overline{CS}$, and $\overline{RD}$ must be low. When HBEN is low, the lower eight bits are read. When HBEN is high, the upper four MSBs are available and the output data bits D4–D7 are either set low (in unipolar mode) or set to the value of the MSB (in bipolar mode) (Table 6).

Table 2. Control-Byte Format

D7 (MSB)	D6	D5	D4	D3	D2	D1	D0 (LSB)
PD1	PD0	ACQMOD	RNG	BIP	A2	A1	A0

BIT	NAME	DESCRIPTION
7, 6	PD1, PD0	These two bits select the clock and power-down modes (Table 4).
5	ACQMOD	0 = internally controlled acquisition (6 clock cycles), 1 = externally controlled acquisition
4	RNG	Selects the full-scale voltage magnitude at the input (Table 3).
3	BIP	Selects unipolar or bipolar conversion mode (Table 3).
2, 1, 0	A2, A1, A0	These are address bits for the input mux to select the "on" channel (Table 5).

Table 3. Range and Polarity Selection

BIP	RNG	INPUT RANGE (V)
0	0	0 to 5
0	1	0 to 10
1	0	±5
1	1	±10

Table 4. Clock and Power-Down Selection

PD1	PD0	DEVICE MODE
0	0	Normal Operation / External Clock Mode
0	1	Normal Operation / Internal Clock Mode
1	0	Standby Power-Down (STBYPD); clock mode is unaffected
1	1	Full Power-Down (FULLPD); clock mode is unaffected

Table 5. Channel Selection

A2	A1	A0	CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7
0	0	0	—							
0	0	1		—						
0	1	0			—					
0	1	1				—				
1	0	0					—			
1	0	1						—		
1	1	0							—	
1	1	1								—

Multi-Range (±10V, ±5V, +10V, +5V), Single +5V, 12-Bit DAS with 8+4 Bus Interface

Table 6. Data-Bus Output

PIN	HBEN = LOW	HBEN = HIGH
D0	B0 (LSB)	B8
D1	B1	B9
D2	B2	B10
D3	B3	B11 (MSB)
D4	B4	B11 (BIP = 1) / 0 (BIP = 0)
D5	B5	B11 (BIP = 1) / 0 (BIP = 0)
D6	B6	B11 (BIP = 1) / 0 (BIP = 0)
D7	B7	B11 (BIP = 1) / 0 (BIP = 0)

How to Start a Conversion

Conversions are initiated with a write operation, which selects the mux channel and configures the MAX197 for either unipolar or bipolar input range. A write pulse ($\overline{WR}$ + CS) can either start an acquisition interval or initiate a combined acquisition plus conversion. The sampling interval occurs at the end of the acquisition interval. The ACQMOD bit in the input control byte offers two options for acquiring the signal: internal or external. The conversion period lasts for 12 clock cycles in either internal or external clock or acquisition mode.

Writing a new control byte during conversion cycle will abort conversion and start a new acquisition interval.

Internal Acquisition

Select internal acquisition by writing the control byte with the ACQMOD bit cleared (ACQMOD = 0). This causes the write pulse to initiate an acquisition interval whose duration is internally timed. Conversion starts when this six-clock-cycle acquisition interval (3µs with f_{CLK} = 2MHz) ends. See Figure 5.

External Acquisition

Use the external acquisition timing mode for precise control of the sampling aperture and/or independent control of acquisition and conversion times. The user controls acquisition and start-of-conversion with two separate write pulses. The first pulse, written with ACQMOD = 1, starts an acquisition interval of indeterminate length. The second write pulse, written with ACQMOD = 0, terminates acquisition and starts conversion on $\overline{WR}$'s rising edge (Figure 6). However, if the second control byte contains ACQMOD = 1, an indefinite acquisition interval is restarted.

The address bits for the input mux must have the same values on the first and second write pulses. Power-down mode bits (PD0, PD1) can assume new values on the second write pulse (see *Power-Down Mode*).

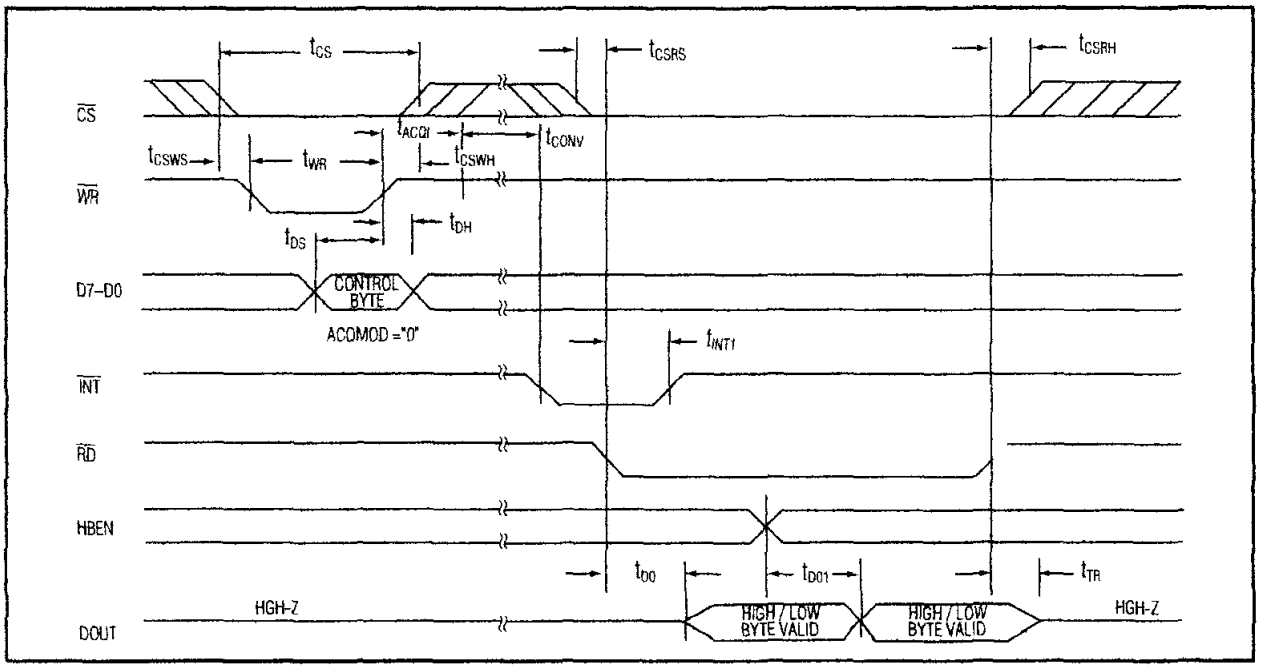


Figure 5. Conversion Timing Using Internal Acquisition Mode

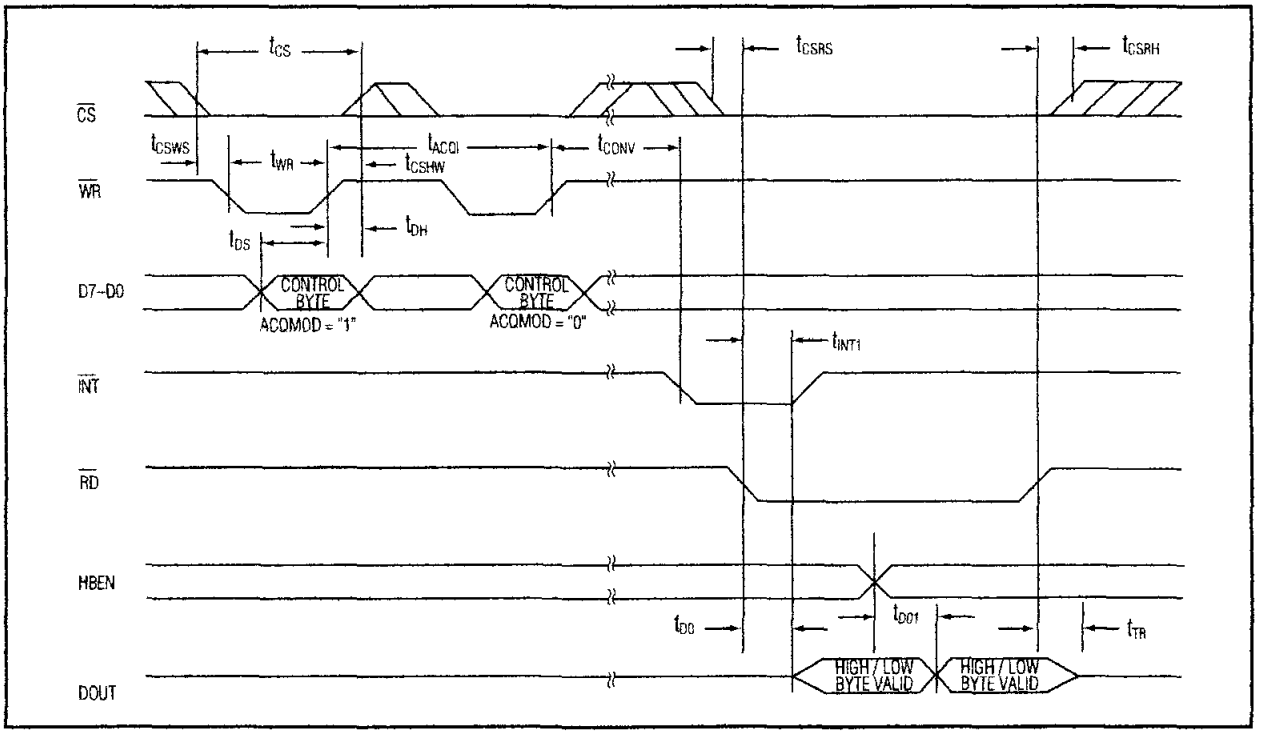


Figure 6. Conversion Timing Using External Acquisition Mode

How to Read a Conversion

A standard interruot signal, INT, is provided to allow the device to flag the µP when the conversion has ended and a valid result is available. INT goes low when conversion is complete and the output data is ready (Figures 5 and 6). It returns high on the first read cycle or if a new control byte is written.

Clock Modes

The MAX197 operates with either an internal or an external clock. Control bits (D6, D7) select either internal or external clock mode. Once the desired clock mode is selected, changing these bits to program power-down will not affect the clock mode. In each mode, internal or external acquisition can be used. At power-up, external clock mode is selected.

Internal Clock Mode

Select internal clock mode to free the µP from the burden of running the SAR conversion clock. To select this mode, write the control byte with D7 = 0 and D6 = 1. A 100pF capacitor between the CLK pin and ground sets this frequency to 1.56MHz nominal. Figure 7 shows a linear relationship between the internal clock period and the value of the external capacitor used.

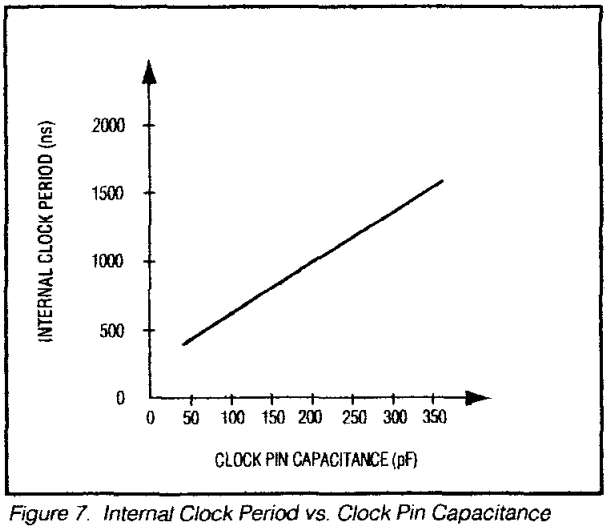


Figure 7. Internal Clock Period vs. Clock Pin Capacitance

Multi-Range (±10V, ±5V, +10V, +5V), Single +5V, 12-Bit DAS with 8+4 Bus Interface

External Clock Mode

Select external clock mode by writing the control byte with D7 = 0 and D6 = 0. Figure 8 shows CLK and $\overline{WR}$ timing relationships in internal and external acquisition modes, with an external clock. A 100kHz to 2.0MHz external clock with 45% to 55% duty cycle is required for proper operation. Operating at clock frequencies lower than 100kHz will cause a voltage droop across the hold capacitor, and subsequently degrade performance.

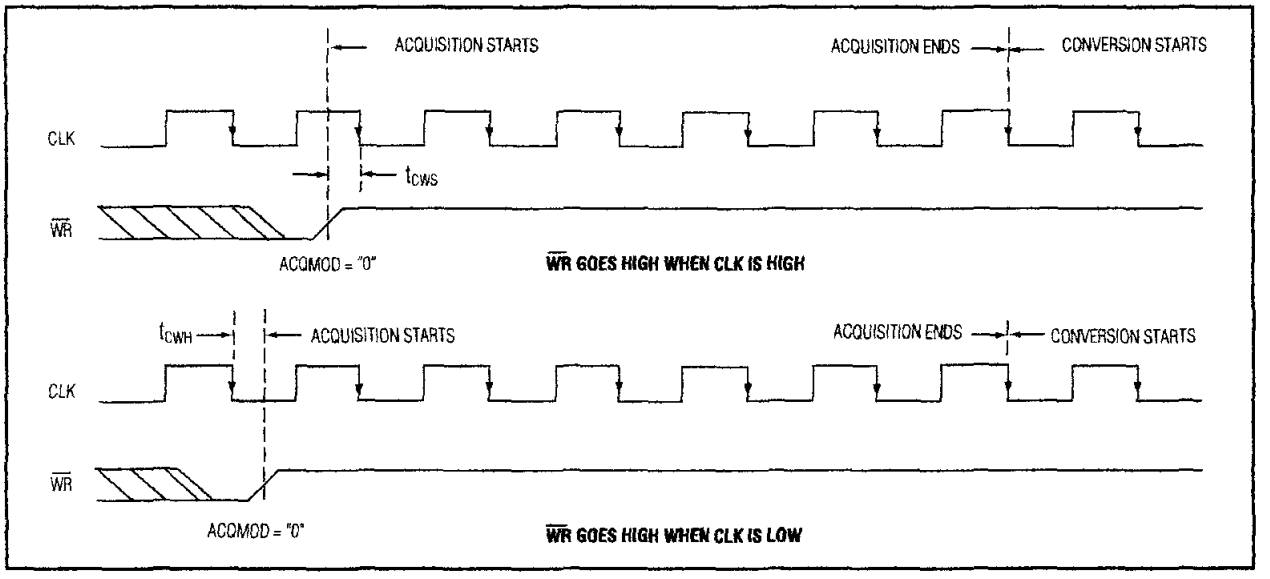


Figure 8a. External Clock and WR Timing (Internal Acquisition Mode)

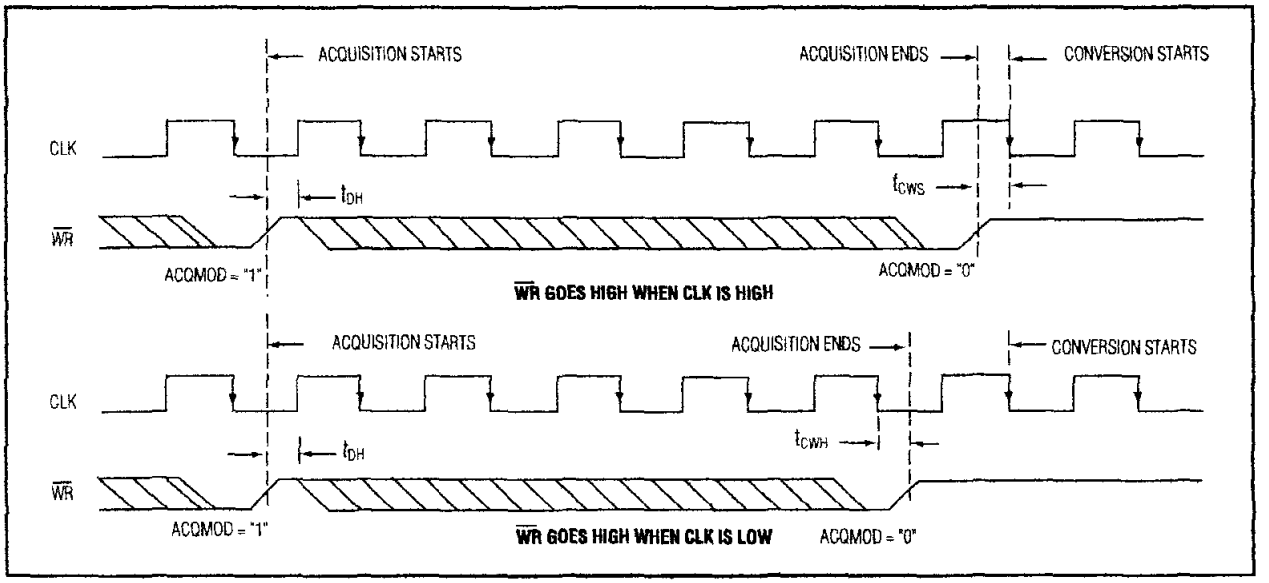


Figure 8b. External Clock and WR Timing (External Acquisition Mode)

Applications Information

Power-On Reset

At power-up, the internal power-supply circuitry sets INT high and puts the device in normal operation/external clock mode. This state is selected to keep the internal clock from loading the external clock driver when the part is used in external clock mode.

Internal or External Reference

The MAX197 can operate with either an internal or an external reference. An external reference can be connected to either the REF pin or to the REFADJ pin (Figure 9).

To use the REF input directly, disable the internal buffer by tying REFADJ to VDD. Using the REFADJ input eliminates the need to buffer the reference externally. When the reference is applied at REFADJ, bypass REFADJ with a 0.01µF capacitor to AGND.

The REFADJ internal buffer gain is trimmed to 1.6384 to provide 4.096V at the REF pin from a 2.5V reference.

Internal Reference

The internally trimmed 2.50V reference is gained through the REFADJ buffer to provide 4.096V at REF. Bypass the REF pin with a 4.7µF capacitor to AGND and the REFADJ pin with a 0.01µF capacitor to AGND. The internal reference voltage is adjustable to ±1.5% (±65 LSBs) with the reference-adjust circuit of Figure 1.

External Reference

At REF and REFADJ, the input impedance is a minimum of 10kΩ for DC currents. During conversions, an external reference at REF must be able to deliver 400µA DC load currents, and must have an output impedance of 10Ω or less. If the reference has higher input impedance or is noisy, bypass it close to the REF pin with a 4.7µF capacitor to AGND.

With an external reference voltage of less than 4.096V at the REF pin or less than 2.5V at the REFADJ pin, the increase in the ratio of the RMS noise to the LSB value (FS / 4096) results in performance degradation (loss of effective bits).

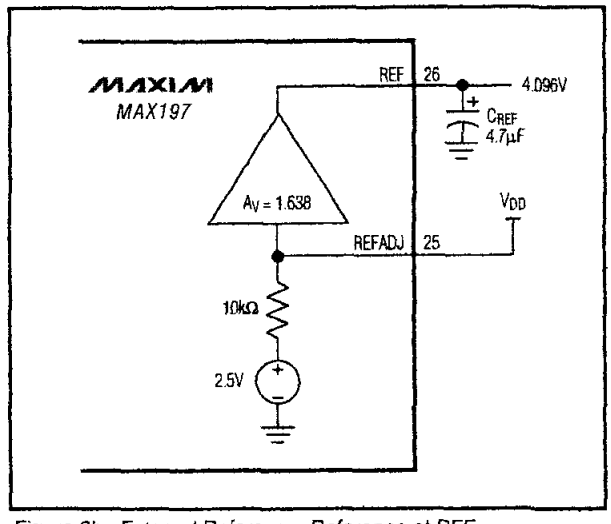


Figure 9b. External Reference, Reference at REF

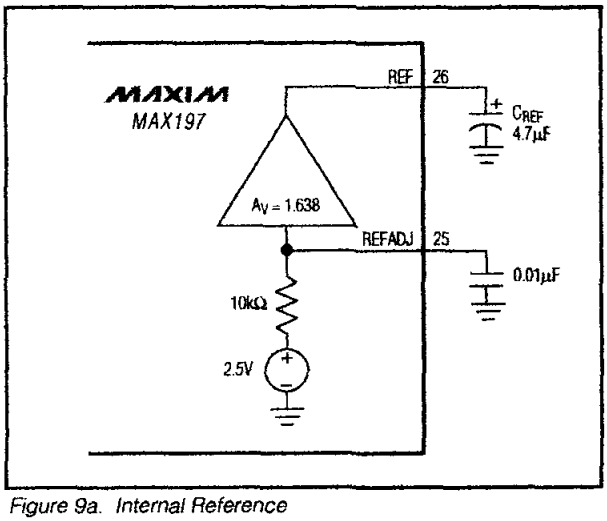


Figure 9a. Internal Reference

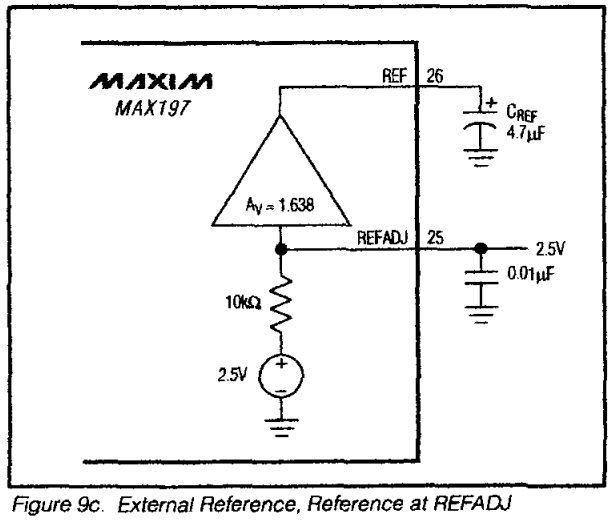


Figure 9c. External Reference, Reference at REFADJ

Multi-Range (±10V, ±5V, +10V, +5V), Single +5V, 12-Bit DAS with 8+4 Bus Interface

Power-Down Mode

To save power, you can put the converter into low-current shutdown mode between conversions. Two programmable power-down modes are available, in addition to a hardware shutdown. Select STBYPD or FULLPD by programming PD0 and PD1 in the input control byte. When software power-down is asserted, it becomes effective only after the end of conversion. In all power-down modes, the interface remains active and conversion results may be read. Input overvoltage protection is active in all power-down modes. The device returns to normal operation on the first WR falling edge during write operation.

For hardware-controlled (FULLPD) power-down, pull the $\overline{SHDN}$ pin low. When hardware shutdown is asserted, it becomes effective immediately and the conversion is aborted.

Choosing Power-Down Modes

The bandgap reference and reference buffer remain active in STBYPD mode, maintaining the voltage on the 4.7µF capacitor at the REF pin. This is a "DC" state that does not degrade after power-down of any duration. Therefore, you can use any sampling rate with this mode, without regard to start-up delays.

However, in FULLPD mode, only the bandgap reference is active. Connect a 33µF capacitor between REF and AGND to maintain the reference voltage between conversion and to reduce transients when the buffer is enabled and disabled. Throughput rates down to 1ksps can be achieved without allotting extra acquisition time for reference recovery prior to conversion. This allows conversion to begin immediately after power-down ends. If the discharge of the REF capacitor during FULLPD exceeds the desired limits for accuracy (less than a fraction of an LSB), run a STBYPD power-down cycle prior to starting conversions. Take into account that the reference buffer recharges the bypass capacitor at an 80mV/ms slew rate and add 50µs for settling time. Throughput rates of 10ksps offer typical supply currents of 470µA, using the recommended 33µF capacitor value.

Auto-Shutdown

Selecting STBYPD on every conversion automatically shuts the MAX197 down after each conversion without requiring any start-up time on the next conversion.

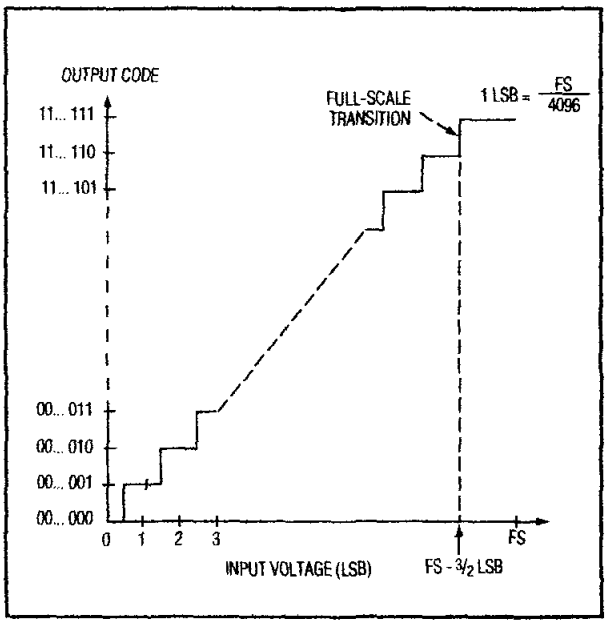


Figure 10. Unipolar Transfer Function

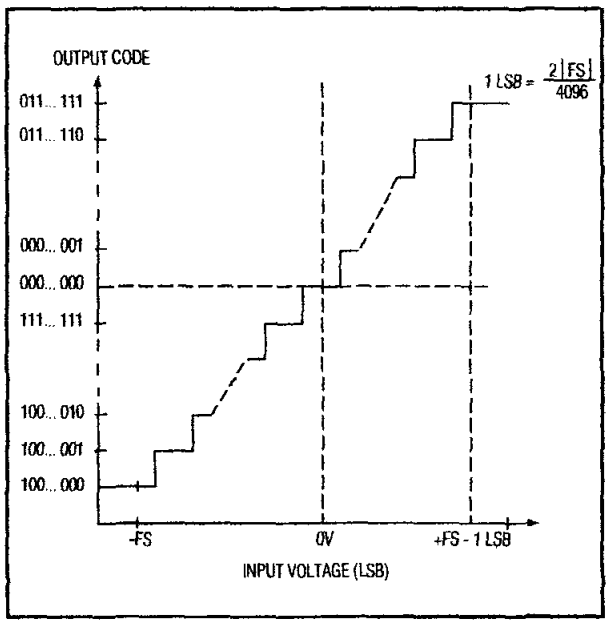


Figure 11. Bipolar Transfer Function

Multi-Range (±10V, ±5V, +10V, +5V), Single +5V, 12-Bit DAS with 8+4 Bus Interface

Transfer Function

Output data coding for the MAX197 is binary in unipolar mode with 1LSB = (FS / 4096) and two's-complement binary in bipolar mode with 1LSB = ((2 x |FS|) / 4096). Code transitions occur halfway between successive-integer LSB values. Figures 10 and 11 show the input/output (I/O) transfer functions for unipolar and bipolar operations, respectively. For full-scale (FS) values, see Table 1.

Layout, Grounding, and Bypassing

Careful printed circuit board layout is essential for best system performance. For best performance, use a ground plane. To reduce crosstalk and noise injection, keep analog and digital signals separate. Digital ground lines can run between digital signal lines to minimize interference. Connect analog grounds and DGND in a star configuration to AGND. For noise-free operation, ensure the ground return from AGND to the supply ground is low impedance and as short as possible. Connect the logic grounds directly to the supply ground. Bypass V_{DD} with 0.1µF and 4.7µF capacitors to AGND to minimize high- and low-frequency fluctuations. If the supply is excessively noisy, connect a 5Ω resistor between the supply and V_{DD}, as shown in Figure 12.

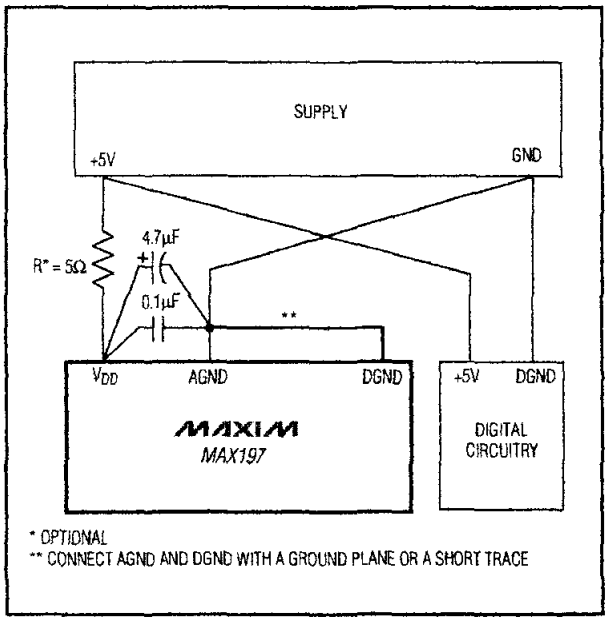


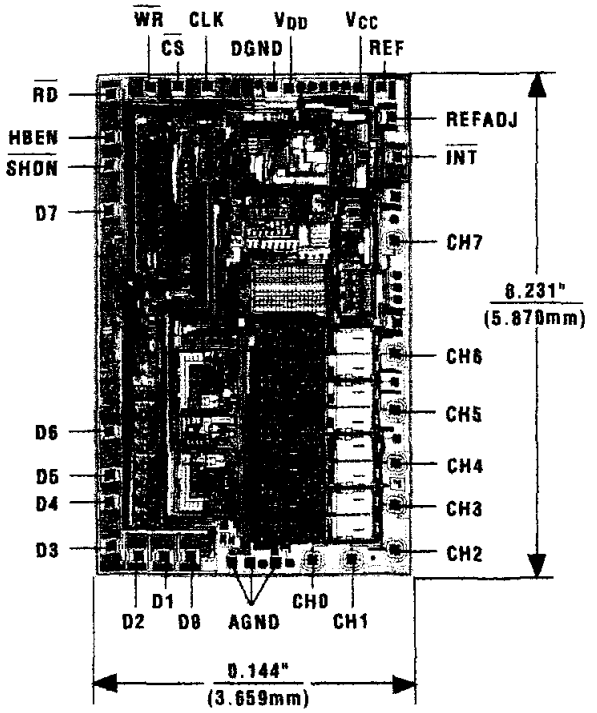
Figure 12. Power-Supply Grounding Connection

Ordering Information (continued)

PART	TEMP RANGE	PIN-PACKAGE
MAX197AENI	-40°C to +85°C	28 Narrow Plastic DIP
MAX197BENI	-40°C to +85°C	28 Narrow Plastic DIP
MAX197AEWI	-40°C to +85°C	28 Wide SO
MAX197BEWI	-40°C to +85°C	28 Wide SO
MAX197AEAI	-40°C to +85°C	28 SSOP
MAX197BEAI	-40°C to +85°C	28 SSOP
MAX197AMYI	-55°C to +125°C	28 Narrow Ceramic SB**
MAX197BMYI	-55°C to +125°C	28 Narrow Ceramic SB**

*** Contact factory for availability and processing to MIL-STD-883.*

Chip Topography

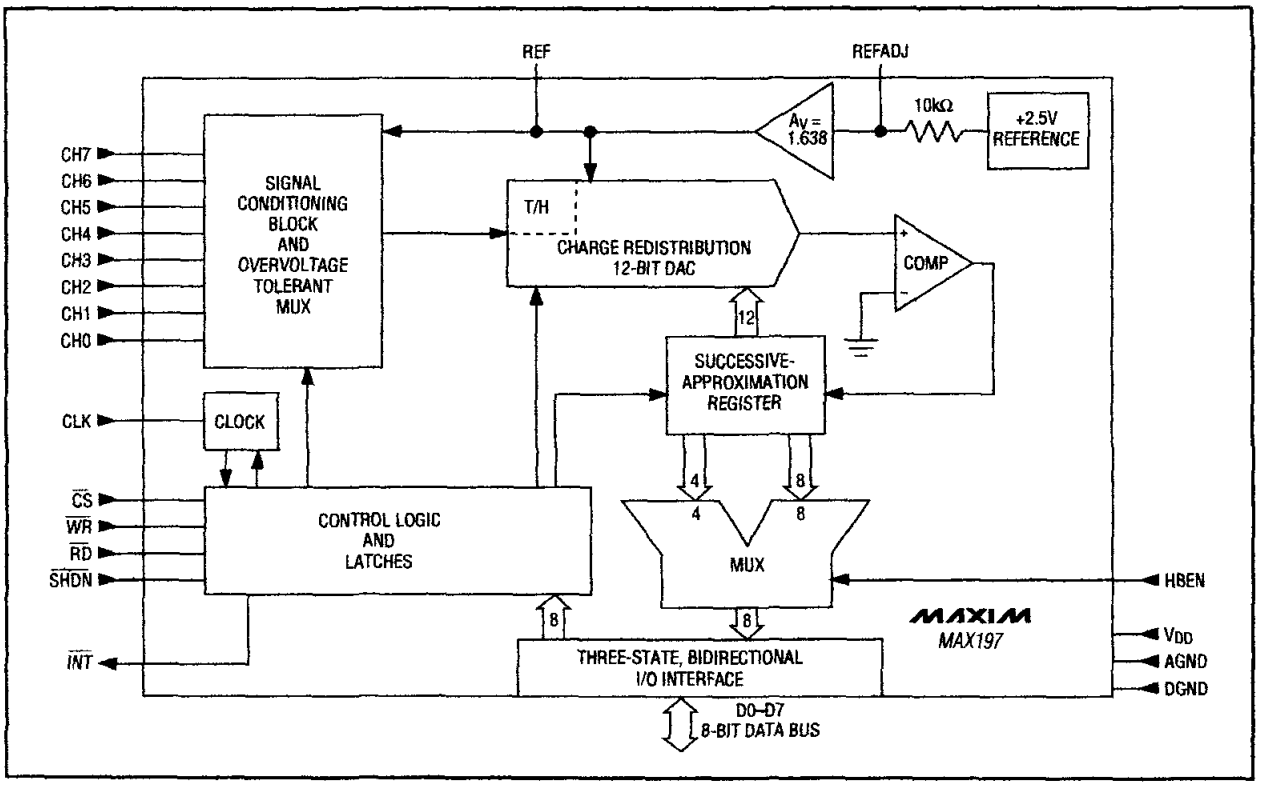


TRANSISTOR COUNT: 2956

SUBSTRATE CONNECTED TO GND

Multi-Range (±10V, ±5V, +10V, +5V), Single +5V, 12-Bit DAS with 8+4 Bus Interface

Functional Diagram



Low-Noise, Precision Operational Amplifier

OP27

FEATURES

Low Noise: 80 nV p-p (0.1 Hz to 10 Hz), 3 nV/$\sqrt{Hz}$
Low Drift: 0.2 μV/°C
High Speed: 2.8 V/μs Slew Rate, 8 MHz Gain Bandwidth
Low V_{OS}: 10 μV
Excellent CMRR: 126 dB at V_{CM} of ±11 V
High Open-Loop Gain: 1.8 Million
Fits 725, OP07, 5534A Sockets
Available in Die Form

GENERAL DESCRIPTION

The OP27 precision operational amplifier combines the low offset and drift of the OP07 with both high speed and low noise. Offsets down to 25 μV and maximum drift of 0.6 μV/°C, makes the OP27 ideal for precision instrumentation applications. Exceptionally low noise, e_n = 3.5 nV/$\sqrt{Hz}$, at 10 Hz, a low 1/f noise corner frequency of 2.7 Hz, and high gain (1.8 million), allow accurate high-gain amplification of low-level signals. A gain-bandwidth product of 8 MHz and a 2.8 V/μsec slew rate provides excellent dynamic accuracy in high-speed, data-acquisition systems.

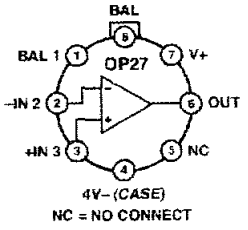
A low input bias current of ±10 nA is achieved by use of a bias-current-cancellation circuit. Over the military temperature range, this circuit typically holds I_B and I_{OS} to ±20 nA and 15 nA, respectively.

The output stage has good load driving capability. A guaranteed swing of ±10 V into 600 Ω and low output distortion make the OP27 an excellent choice for professional audio applications.

(Continued on page 7)

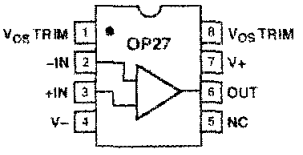
PIN CONNECTIONS

TO-99
(J-Suffix)



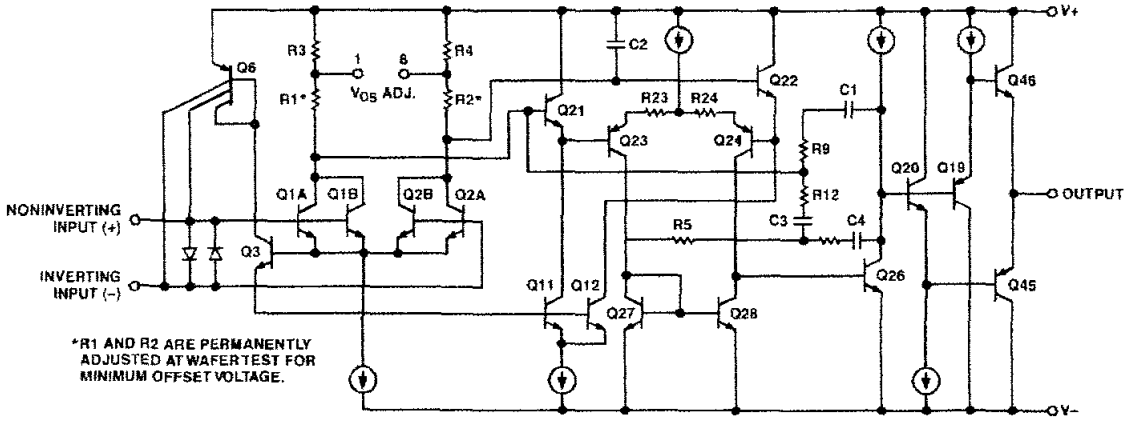
NC = NO CONNECT

8-Pin Hermetic DIP
(Z-Suffix)
Epoxy Mini-DIP
(P-Suffix)
8-Pin SO
(S-Suffix)



NC = NO CONNECT

SIMPLIFIED SCHEMATIC



REV. C

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781/329-4700 www.analog.com
Fax: 781/326-8703

OP27–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (@ V_S = ±15 V, T_A = 25°C, unless otherwise noted.)

Parameter	Symbol	Conditions	OP27A/E Min	OP27A/E Typ	OP27A/E Max	OP27F Min	OP27F Typ	OP27F Max	OP27C/G Min	OP27C/G Typ	OP27C/G Max	Unit
INPUT OFFSET VOLTAGE[1]	V_{OS}			10	25		20	60		30	100	µV
LONG-TERM V_{OS} STABILITY[2, 3]	V_{OS}/Time			0.2	1.0		0.3	1.5		0.4	2.0	µV/M_O
INPUT OFFSET CURRENT	I_{OS}			7	35		9	50		12	75	nA
INPUT BIAS CURRENT	I_B			±10	±40		±12	±55		±15	±80	nA
INPUT NOISE VOLTAGE[3, 4]	$e_{n\ p\text{-}p}$	0.1 Hz to 10 Hz		0.08	0.18		0.08	0.18		0.09	0.25	µV p-p
INPUT NOISE Voltage Density[3]	e_n	f_O = 10 Hz		3.5	5.5		3.5	5.5		3.8	8.0	nV/√Hz
		f_O = 30 Hz		3.1	4.5		3.1	4.5		3.3	5.6	nV/√Hz
		f_O = 1000 Hz		3.0	3.8		3.0	3.8		3.2	4.5	nV/√Hz
INPUT NOISE Current Density[3, 5]	i_n	f_O = 10 Hz		1.7	4.0		1.7	4.0		1.7		pA/√Hz
		f_O = 30 Hz		1.0	2.3		1.0	2.3		1.0		pA/√Hz
		f_O = 1000 Hz		0.4	0.6		0.4	0.6		0.4	0.6	pA/√Hz
INPUT RESISTANCE												
Differential-Mode[6]	R_{IN}		1.3	6		0.94	5		0.7	4		MΩ
Common-Mode	R_{INCM}			3			2.5			2		GΩ
INPUT VOLTAGE RANGE	IVR		±11.0	±12.3		±11.0	±12.3		±11.0	±12.3		V
COMMON-MODE REJECTION RATIO	CMRR	V_{CM} = ±11 V	114	126		106	123		100	120		dB
POWER SUPPLY REJECTION RATIO	PSRR	V_S = ±4 V to ±18 V		1	10		1	10		2	20	µV/V
LARGE-SIGNAL VOLTAGE GAIN	A_{VO}	R_L ≥ 2 kΩ, V_O = ±10 V	1000	1800		1000	1800		700	1500		V/mV
		R_L ≥ 600 Ω, V_O = ±10 V	800	1500		800	1500		600	1500		V/mV
OUTPUT VOLTAGE SWING	V_O	R_L ≥ 2 kΩ	±12.0	±13.8		±12.0	±13.8		±11.5	±13.5		V
		R_L ≥ 600 Ω	±10.0	±11.5		±10.0	±11.5		±10.0	±11.5		V
SLEW RATE[7]	SR	R_L ≥ 2 kΩ	1.7	2.8		1.7	2.8		1.7	2.8		V/µs
GAIN BANDWIDTH PRODUCT[7]	GBW		5.0	8.0		5.0	8.0		5.0	8.0		MHz
OPEN-LOOP OUTPUT RESISTANCE	R_O	V_O = 0, I_O = 0		70			70			70		Ω
POWER CONSUMPTION	P_d	V_O		90	140		90	140		100	170	mW
OFFSET ADJUSTMENT RANGE		R_P = 10 kΩ		±4.0			±4.0			±4.0		mV

NOTES

[1]Input offset voltage measurements are performed ~ 0.5 seconds after application of power. A/E grades guaranteed fully warmed up.

[2]Long-term input offset voltage stability refers to the average trend line of V_{OS} versus. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 days are typically 2.5 µV. Refer to typical performance curve.

[3]Sample tested.

[4]See test circuit and frequency response curve for 0.1 Hz to 10 Hz tester.

[5]See test circuit for current noise measurement.

[6]Guaranteed by input bias current.

[7]Guaranteed by design.

ELECTRICAL CHARACTERISTICS (@ $V_S = \pm 15$ V, $-55°C \le T_A \le 125°C$, unless otherwise noted.)

Parameter	Symbol	Conditions	OP27A Min	OP27A Typ	OP27A Max	OP27C Min	OP27C Typ	OP27C Max	Unit
INPUT OFFSET VOLTAGE[1]	V_{OS}			30	60		70	300	μV
AVERAGE INPUT OFFSET DRIFT	TCV_{OS}[2] TCV_{OSn}[3]			0.2	0.6		4	1.8	μV/°C
INPUT OFFSET CURRENT	I_{OS}			15	50		30	135	nA
INPUT BIAS CURRENT	I_B			±20	±60		±35	±150	nA
INPUT VOLTAGE RANGE	IVR		±10.3	±11.5		±10.2	±11.5		V
COMMON-MODE REJECTION RATIO	CMRR	$V_{CM} = \pm 10$ V	108	122		94	118		dB
POWER SUPPLY REJECTION RATIO	PSRR	$V_S = \pm 4.5$ V to ±18 V		2	16		4	51	μV/V
LARGE-SIGNAL VOLTAGE GAIN	A_{VO}	$R_L \ge 2$ kΩ, $V_O = \pm 10$ V	600	1200		300	800		V/mV
OUTPUT VOLTAGE SWING	V_O	$R_L \ge 2$ kΩ	±11.5	±13.5		±10.5	±13.0		V

NOTES

[1]Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power. A/E grades guaranteed fully warmed up.

[2]The TCV_{OS} performance is within the specifications unnulled or when nulled with R_P = 8 kΩ to 20 kΩ. TCV_{OS} is 100% tested for A/E grades, sample tested for C/F/G grades.

[3]Guaranteed by design.

ELECTRICAL CHARACTERISTICS

(@ $V_S = \pm 15$ V, $-25°C \le T_A \le 85°C$ for OP27J, OP27Z, $0°C \le T_A \le 70°C$ for OP27EP, OP27FP, and $-40°C \le T_A \le 85°C$ for OP27GP, OP27GS, unless otherwise noted.)

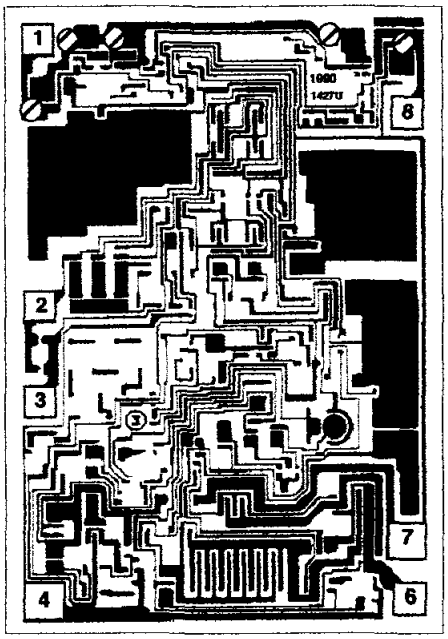
Parameter	Symbol	Conditions	OP27E Min	OP27E Typ	OP27E Max	OP27F Min	OP27F Typ	OP27F Max	OP27G Min	OP27G Typ	OP27G Max	Unit
INPUT ONSET VOLTAGE	V_{OS}			20	50		40	140		55	220	μV
AVERAGE INPUT OFFSET DRIFT	TCV_{OS}[1] TCV_{OSn}[2]			0.2 0.2	0.6 0.6		0.3 0.3	1.3 1.3		0 4 0 4	1.8 1.8	μV/°C μV/°C
INPUT OFFSET CURRENT	I_{OS}			10	50		14	85		20	135	nA
INPUT BIAS CURRENT	I_B			±14	±60		±18	±95		±25	±150	nA
INPUT VOLTAGE RANGE	IVR		±10.5	±11.8		±10.5	±11.8		±10.5	±11.8		V
COMMON-MODE REJECTION RATIO	CMRR	$V_{CM} = \pm 10$ V	110	124		102	121		96	118		dB
POWER SUPPLY REJECTION RATIO	PSRR	$V_S = \pm 4.5$ V to ±18 V		2	15		2	16		2	32	μV/V
LARGE-SIGNAL VOLTAGE GAIN	A_{VO}	$R_L \ge 2$ kΩ, $V_O = \pm 10$ V	750	1500		700	1300		450	1000		V/mV
OUTPUT VOLTAGE SWING	V_O	$R_L \ge 2$ kΩ	±11.7	±13.6		±11.4	±13.5		±11.0	±13.3		V

NOTES

[1]The TCV_{OS} performance is within the specifications unnulled or when nulled with R_P = 8 kΩ to 20 kΩ. TCV_{OS} is 100% tested for A/E grades, sample tested for C/F/G grades.

[2]Guaranteed by design.

DIE CHARACTERISTICS



1. NULL
2. (–) INPUT
3. (+) INPUT
4. V–
6. OUTPUT
7. V+
8. NULL

WAFER TEST LIMITS (@ $V_S = \pm 15$ V, $T_A = 25°C$ unless otherwise noted.)

Parameter	Symbol	Conditions	OP27N Limit	OP27G Limit	OP27GR Limit	Unit
INPUT OFFSET VOLTAGE*	V_{OS}		35	60	100	µV Max
INPUT OFFSET CURRENT	I_{OS}		35	50	75	nA Max
INPUT BIAS CURRENT	IB		±40	±55	±80	nA Max
INPUT VOLTAGE RANGE	IVR		±11	±11	±11	V Min
COMMON-MODE REJECTION RATIO	CMRR	V_{CM} = IVR	114	106	100	dB Min
POWER SUPPLY	PSRR	$V_S = \pm 4$ V to ±18 V	10	10	20	µV/V Max
LARGE-SIGNAL VOLTAGE GAIN	A_{VO} A_{VO}	$R_L \geq 2$ kΩ, $V_O = \pm 10$ V $R_L \geq 600$ Ω, $V_O = \pm 10$ V	1000 800	1000 800	700 600	V/mV Min V/mV Min
OUTPUT VOLTAGE SWING	V_O V_O	$R_L \geq 2$ kΩ RL2600n	±12.0 ±10.0	±12.0 ±10.0	+11.5 ±10.0	V Min V Min
POWER CONSUMPTION	P_d	$V_O = 0$	140	140	170	mW Max

NOTE

*Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS (@ $V_S = \pm 15$ V, $T_A = 25°C$ unless otherwise noted.)

Parameter	Symbol	Conditions	OP27N Typical	OP27G Typical	OP27GR Typical	Unit
AVERAGE INPUT OFFSET VOLTAGE DRIFT*	TCV_{OS} or TCV_{OSn}	Nulled or Unnulled R_P = 8 kΩ to 20 kΩ	0.2	0.3	0.4	μV/°C
AVERAGE INPUT OFFSET CURRENT DRIFT	TCI_{OS}		80	130	180	pA/°C
AVERAGE INPUT BIAS CURRENT DRIFT	TCI_B		100	160	200	pA/°C
INPUT NOISE VOLTAGE DENSITY	e_n	f_O = 10 Hz	3.5	3.5	3.8	nV/$\sqrt{Hz}$
	e_n	f_O = 30 Hz	3.1	3.1	3.3	nV/$\sqrt{Hz}$
	e_n	f_O = 1000 Hz	3.0	3.0	3.2	nV/$\sqrt{Hz}$
INPUT NOISE CURRENT DENSITY	i_n	f_O = 10 Hz	1.7	1.7	1.7	pA/$\sqrt{Hz}$
	i_n	f_O = 30 Hz	1.0	1.0	1.0	pA/$\sqrt{Hz}$
	i_n	f_O = 1000 Hz	0.4	0.4	0.4	pA/$\sqrt{Hz}$
INPUT NOISE VOLTAGE	e_{np-p}	0.1 Hz to 10 Hz	0.08	0.08	0.09	μV p-p
SLEW RATE	SR	$R_L \geq 2$ kΩ	2.8	2.8	2.8	V/μs
GAIN BANDWIDTH PRODUCT	GBW		8	8	8	MHz

NOTE
*Input offset voltage measurements are performed by automated test equipment approximately 0.5 seconds after application of power.

(Continued from page 1)

PSRR and CMRR exceed 120 dB. These characteristics, coupled with long-term drift of 0.2 µV/month, allow the circuit designer to achieve performance levels previously attained only by discrete designs.

Low-cost, high-volume production of OP27 is achieved by using an on-chip Zener zap-trimming network. This reliable and stable offset trimming scheme has proved its effectiveness over many years of production history.

The OP27 provides excellent performance in low-noise, high-accuracy amplification of low-level signals. Applications include stable integrators, precision summing amplifiers, precision voltage-threshold detectors, comparators, and professional audio circuits such as tape-head and microphone preamplifiers.

The OP27 is a direct replacement for 725, OP06, OP07, and OP45 amplifiers; 741 types may be directly replaced by removing the 741's nulling potentiometer.

ABSOLUTE MAXIMUM RATINGS[4]

Supply Voltage	±22 V
Input Voltage[1]	±22 V
Output Short-Circuit Duration	Indefinite
Differential Input Voltage[2]	±0.7 V
Differential Input Current[2]	±25 mA
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
OP27A, OP27C (J, Z)	-55°C to +125°C
OP27E, OP27F (J, Z)	-25°C to +85°C
OP27E, OP27F (P)	0°C to 70°C
OP27G (P, S, J, Z)	-40°C to +85°C
Lead Temperature Range (Soldering, 60 sec)	300°C
Junction Temperature	-65°C to +150°C

Package Type	θ_{JA}[3]	θ_{JC}	Unit
TO 99 (J)	150	18	°C/W
8-Lead Hermetic DIP (Z)	148	16	°C/W
8-Lead Plastic DIP (P)	103	43	°C/W
20-Contact LCC (RC)	98	38	°C/W
8-Lead SO (S)	158	43	°C/W

NOTES
[1]For supply voltages less than ±22 V, the absolute maximum input voltage is equal to the supply voltage.
[2]The OP27's inputs are protected by back-to-back diodes. Current limiting resistors are not used in order to achieve low noise. If differential input voltage exceeds ±0.7 V, the input current should be limited to 25 mA.
[3]θ_{JA} is specified for worst-case mounting conditions, i.e., θ_{JA} is specified for device in socket for TO, CERDIP, and P-DIP packages; θ_{JA} is specified for device soldered to printed circuit board for SO package.
[4]Absolute Maximum Ratings apply to both DICE and packaged parts, unless otherwise noted.

ORDERING INFORMATION[1]

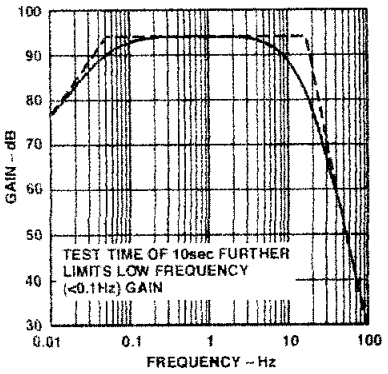
	Package			
T_A = 25°C V_{OS} Max (µV)	TO-99	CERDIP 8-Lead	Plastic 8-Lead	Operating Temperature Range
25	OP27AJ[2,3]	OP27AZ[2]		MIL
25	OP27EJ[2,3]	OP27EZ	OP27EP	IND/COM
60			OP27FP[3]	IND/COM
100		OP27CZ[3]		MIL
100	OP27GJ	OP27GZ	OP27GP	XIND
100			OP27GS[4]	XIND

NOTES
[1]Burn-in is available on commercial and industrial temperature range parts in CERDIP, plastic DIP, and TO-can packages.
[2]For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.
[3]Not for new design; obsolete April 2002.
[4]For availability and burn-in information on SO and PLCC packages, contact your local sales office.

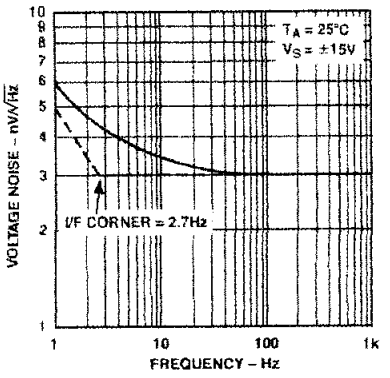
CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the OP27 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

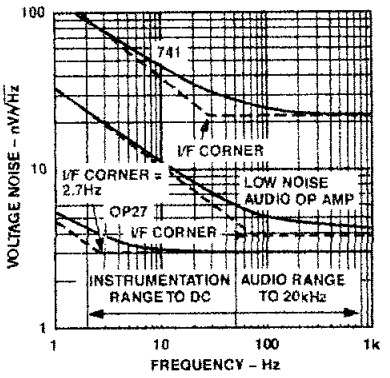
OP27–Typical Performance Characteristics



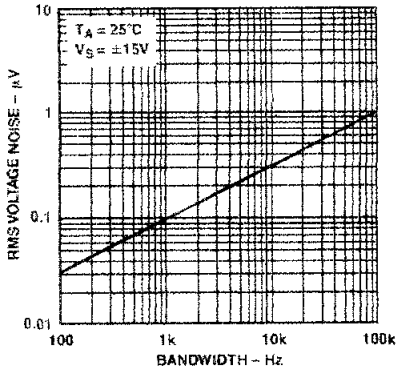
TPC 1. 0.1 Hz to 10 Hz_{p-p} Noise Tester Frequency Response



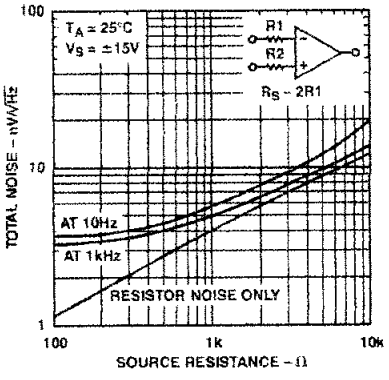
TPC 2. Voltage Noise Density vs. Frequency



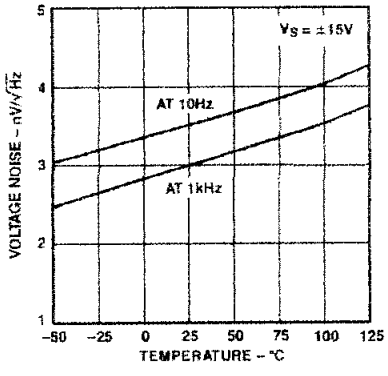
TPC 3. A Comparison of Op Amp Voltage Noise Spectra



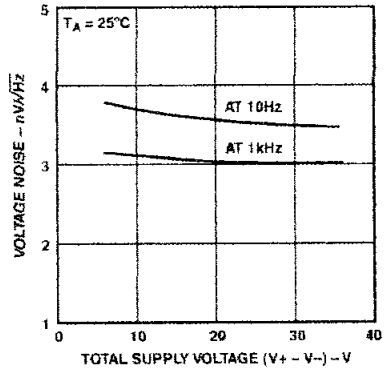
TPC 4. Input Wideband Voltage Noise vs. Bandwidth (0.1 Hz to Frequency Indicated)



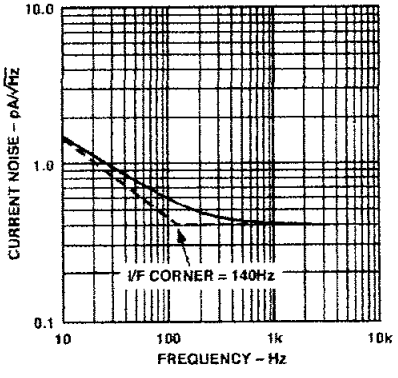
TPC 5. Total Noise vs. Sourced Resistance



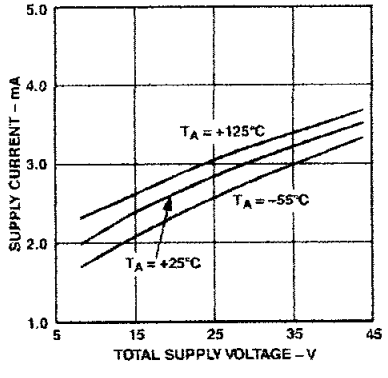
TPC 6. Voltage Noise Density vs. Temperature



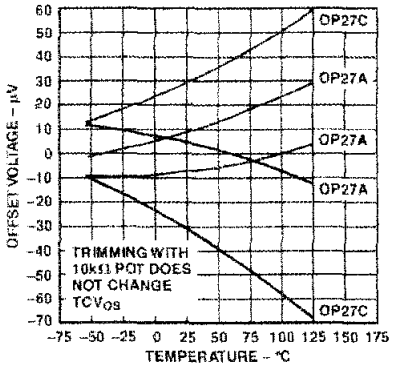
TPC 7. Voltage Noise Density vs. Supply Voltage



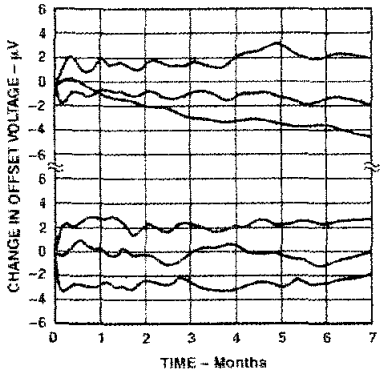
TPC 8. Current Noise Density vs. Frequency



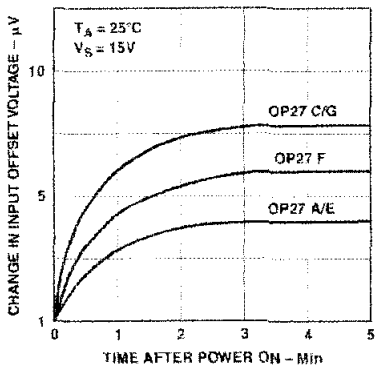
TPC 9. Supply Current vs. Supply Voltage



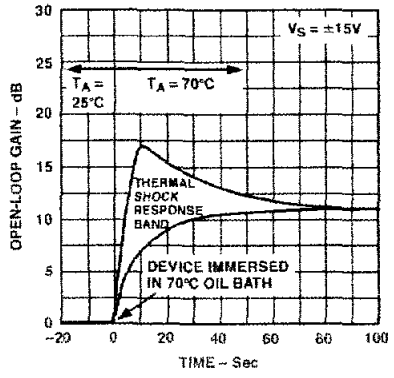
TPC 10. Offset Voltage Drift of Five Representative Units vs. Temperature



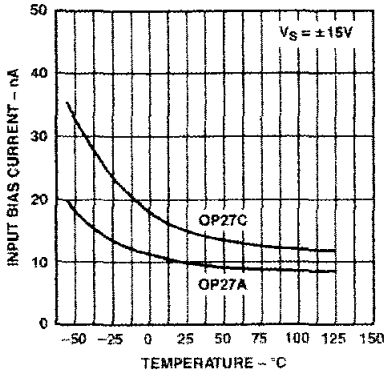
TPC 11. Long-Term Offset Voltage Drift of Six Representative Units



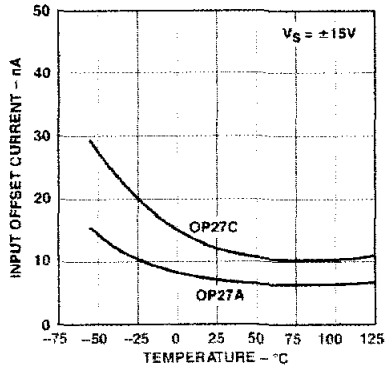
TPC 12. Warm-Up Offset Voltage Drift



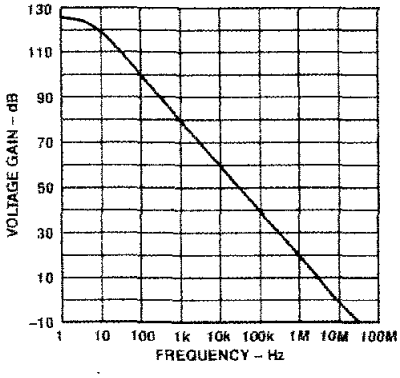
TPC 13. Offset Voltage Change Due to Thermal Shock



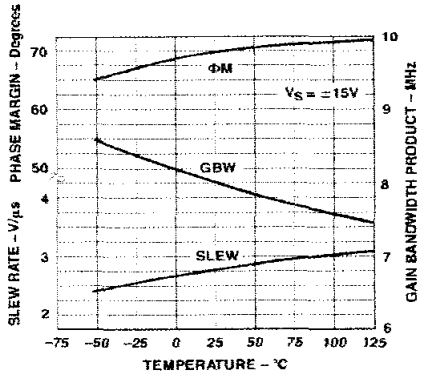
TPC 14. Input Bias Current vs. Temperature



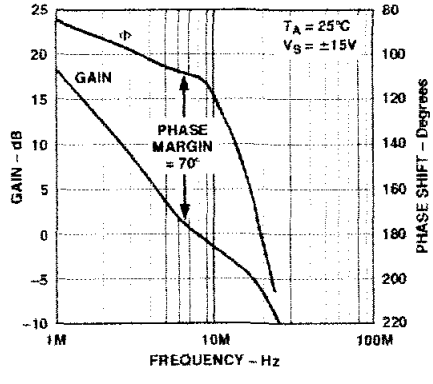
TPC 15. Input Offset Current vs. Temperature



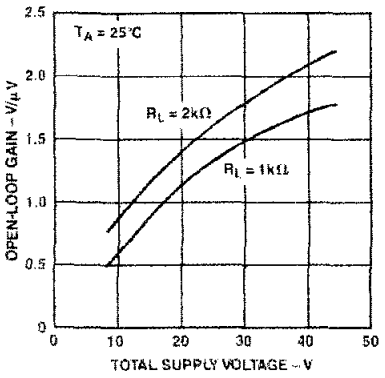
TPC 16. Open-Loop Gain vs. Frequency



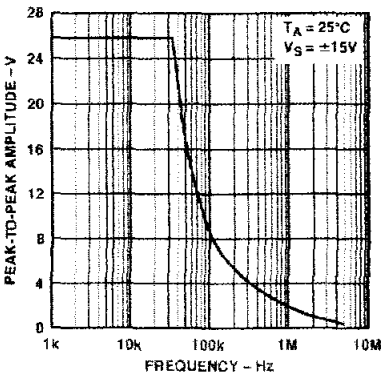
TPC 17. Slew Rate, Gain-Bandwidth Product, Phase Margin vs. Temperature



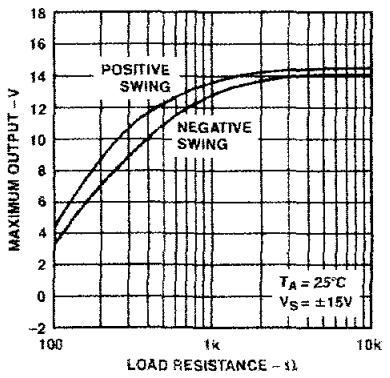
TPC 18. Gain, Phase Shift vs. Frequency



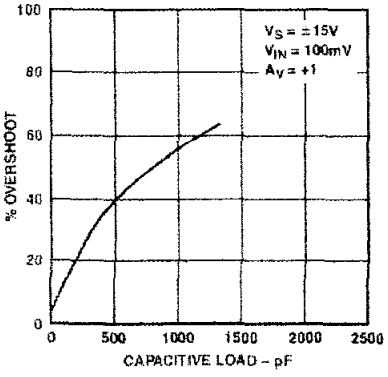
TPC 19. Open-Loop Voltage Gain vs. Supply Voltage



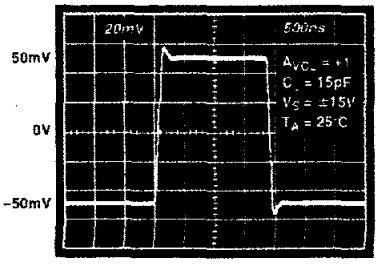
TPC 20. Maximum Output Swing vs. Frequency



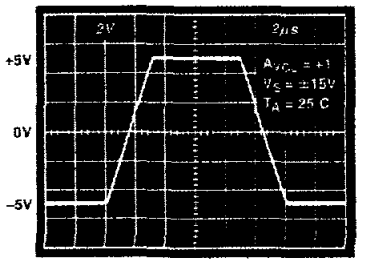
TPC 21. Maximum Output Voltage vs. Load Resistance



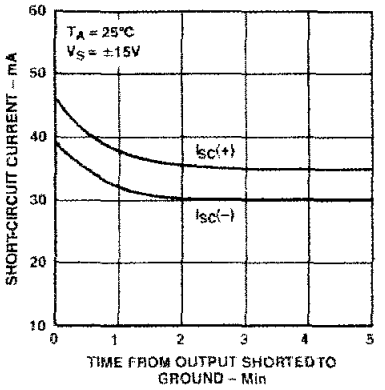
TPC 22. Small-Signal Overshoot vs. Capacitive Load



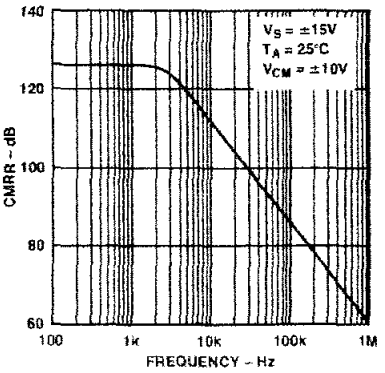
TPC 23. Small-Signal Transient Response



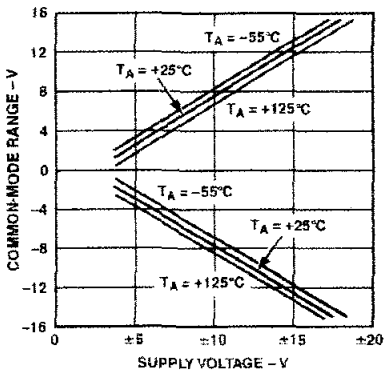
TPC 24. Large-Signal Transient Response



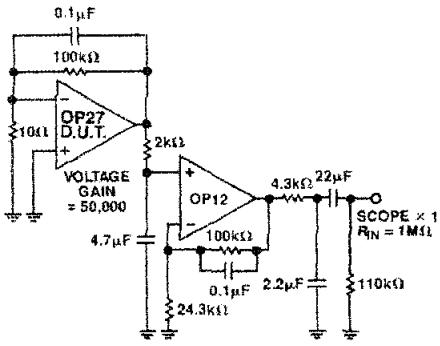
TPC 25. Short-Circuit Current vs. Time



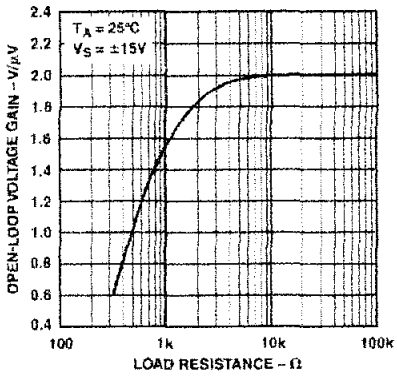
TPC 26. CMRR vs. Frequency



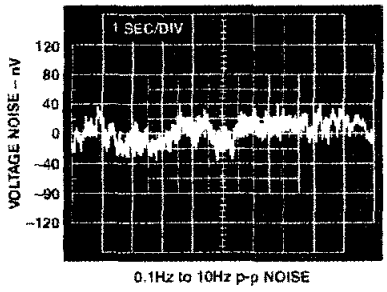
TPC 27. Common-Mode Input Range vs. Supply Voltage



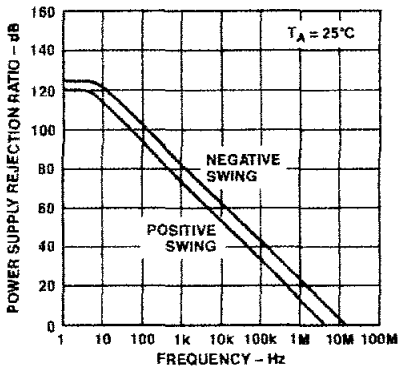
TPC 28. Voltage Noise Test Circuit (0.1 Hz to 10 Hz)



TPC 29. Open-Loop Voltage Gain vs. Load Resistance



TPC 30. Low-Frequency Noise



TPC 31. PSRR vs. Frequency

APPLICATION INFORMATION

OP27 series units may be inserted directly into 725 and OP07 sockets with or without removal of external compensation or nulling components. Additionally, the OP27 may be fitted to unnulled 741-type sockets; however, if conventional 741 nulling circuitry is in use, it should be modified or removed to ensure correct OP27 operation. OP27 offset voltage may be nulled to zero (or another desired setting) using a potentiometer (see Figure 1).

The OP27 provides stable operation with load capacitances of up to 2000 pF and ±10 V swings; larger capacitances should be decoupled with a 50 Ω resistor inside the feedback loop. The OP27 is unity-gain stable.

Thermoelectric voltages generated by dissimilar metals at the input terminal contacts can degrade the drift performance. Best operation will be obtained when both input contacts are maintained at the same temperature.

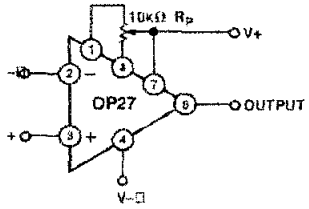


Figure 1. Offset Nulling Circuit

OFFSET VOLTAGE ADJUSTMENT

The input offset voltage of the OP27 is trimmed at wafer level. However, if further adjustment of V_{OS} is necessary, a 10 kΩ trim potentiometer can be used. TCV_{OS} is not degraded (see Offset Nulling Circuit). Other potentiometer values from 1 kΩ to 1 MΩ can be used with a slight degradation (0.1 μV/°C to 0.2 μV/°C) of TCV_{OS}. Trimming to a value other than zero creates a drift of approximately (V_{OS}/300) μV/°C. For example, the change in TCV_{OS} will be 0.33 μV/°C if V_{OS} is adjusted to 100 μV. The offset voltage adjustment range with a 10 kΩ potentiometer is ±4 mV. If smaller adjustment range is required, the nulling sensitivity can be reduced by using a smaller pot in conjuction with fixed resistors. For example, Figure 2 shows a network that will have a ±280 μV adjustment range.

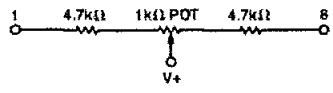


Figure 2. Offset Voltage Adjustment

NOISE MEASUREMENTS

To measure the 80 nV peak-to-peak noise specification of the OP27 in the 0.1 Hz to 10 Hz range, the following precautions must be observed:

1. The device must be warmed up for at least five minutes. As shown in the warm-up drift curve, the offset voltage typically changes 4 μV due to increasing chip temperature after power-up. In the 10-second measurement interval, these temperature-induced effects can exceed tens-of-nanovolts.
2. For similar reasons, the device has to be well-shielded from air currents. Shielding minimizes thermocouple effects.
3. Sudden motion in the vicinity of the device can also "feedthrough" to increase the observed noise.
4. The test time to measure 0.1 Hz to 10 Hz noise should not exceed 10 seconds. As shown in the noise-tester frequency response curve, the 0.1 Hz corner is defined by only one zero. The test time of 10 seconds acts as an additional zero to eliminate noise contributions from the frequency band below 0.1 Hz.
5. A noise-voltage-density test is recommended when measuring noise on a large number of units. A 10 Hz noise-voltage-density measurement will correlate well with a 0.1 Hz to 10 Hz peak-to-peak noise reading, since both results are determined by the white noise and the location of the 1/f corner frequency.

UNITY-GAIN BUFFER APPLICATIONS

When $R_f \leq 100\ \Omega$ and the input is driven with a fast, large signal pulse (>1 V), the output waveform will look as shown in the pulsed operation diagram (Figure 3).

During the fast feedthrough-like portion of the output, the input protection diodes effectively short the output to the input and a current, limited only by the output short-circuit protection, will be drawn by the signal generator. With $R_f \geq 500\ \Omega$, the output is capable of handling the current requirements ($I_L \leq 20$ mA at 10 V); the amplifier will stay in its active mode and a smooth transition will occur.

When $R_f > 2$ kΩ, a pole will be created with R_f and the amplifier's input capacitance (8 pF) that creates additional phase shift and reduces phase margin. A small capacitor (20 pF to 50 pF) in parallel with R_f will eliminate this problem.

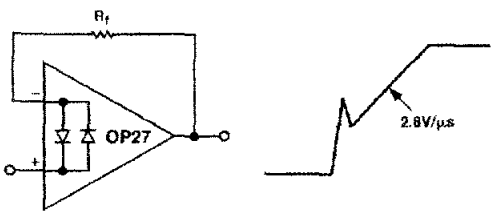


Figure 3. Pulsed Operation

COMMENTS ON NOISE

The OP27 is a very low-noise monolithic op amp. The outstanding input voltage noise characteristics of the OP27 are achieved mainly by operating the input stage at a high quiescent current. The input bias and offset currents, which would normally increase, are held to reasonable values by the input bias-current cancellation circuit. The OP27A/E has I_B and I_{OS} of only ±40 nA and 35 nA at 25°C respectively. This is particularly important when the input has a high source resistance. In addition, many audio amplifier designers prefer to use direct coupling. The high I_B, V_{OS}, and TCV_{OS} of previous designs have made direct coupling difficult, if not impossible, to use.

Voltage noise is inversely proportional to the square root of bias current, but current noise is proportional to the square root of bias current. The OP27's noise advantage disappears when high source-resistors are used. Figures 4, 5, and 6 compare OP27's observed total noise with the noise performance of other devices in different circuit applications.

$$Total\ Noise = \left[\begin{array}{l}(Voltage\ Noise)^2 + \\ (Current\ Noise \times R_S)^2 + \\ (Resistor\ Noise)^2\end{array}\right]^{1/2}$$

Figure 4 shows noise versus source-resistance at 1000 Hz. The same plot applies to wideband noise. To use this plot, multiply the vertical scale by the square root of the bandwidth.

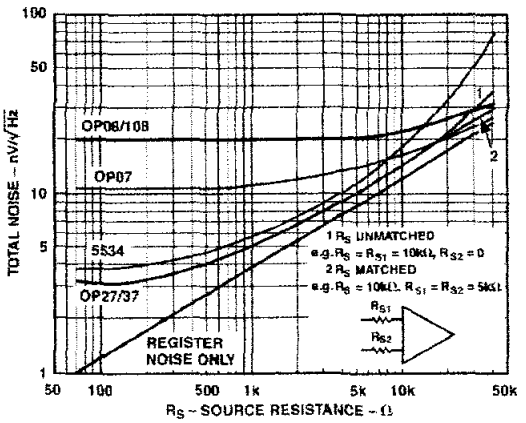


Figure 4. Noise vs. Source Resistance (Including Resistor Noise) at 1000 Hz

At R_S <1 kΩ, the OP27's low voltage noise is maintained. With R_S <1 kΩ, total noise increases, but is dominated by the resistor noise rather than current or voltage noise. It is only beyond R_S of 20 kΩ that current noise starts to dominate. The argument can be made that current noise is not important for applications with low to moderate source resistances. The crossover between the OP27, OP07, and OP08 noise occurs in the 15 kΩ to 40 kΩ region.

Figure 5 shows the 0.1 Hz to 10 Hz peak-to-peak noise. Here the picture is less favorable; resistor noise is negligible and current noise becomes important because it is inversely proportional to the square root of frequency. The crossover with the OP07 occurs in the 3 kΩ to 5 kΩ range depending on whether balanced or unbalanced source resistors are used (at 3 kΩ the I_B and I_{OS} error also can be three times the V_{OS} spec.).

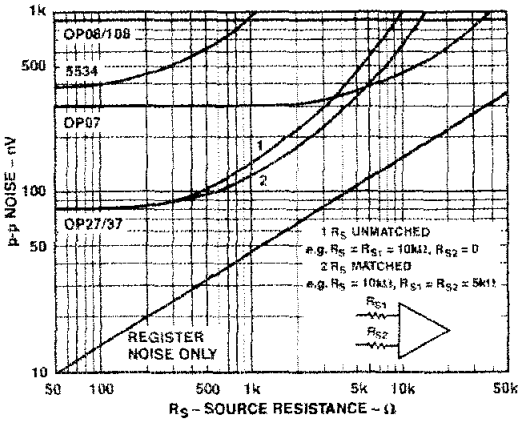


Figure 5. Peak-to-Peak Noise (0.1 Hz to 10 Hz) as Source Resistance (Includes Resistor Noise)

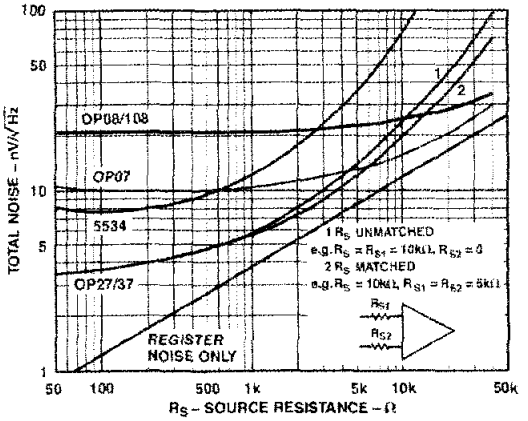


Figure 6. 10 Hz Noise vs. Source Resistance (Includes Resistor Noise)

Therefore, for low-frequency applications, the OP07 is better than the OP27/OP37 when $R_S > 3\ k\Omega$. The only exception is when gain error is important. Figure 6 illustrates the 10 Hz noise. As expected, the results are between the previous two figures.

For reference, typical source resistances of some signal sources are listed in Table I.

Table I.

Device	Source Impedance	Comments
Strain Gauge	<500 Ω	Typically used in low-frequency applications.
Magnetic Tapehead	<1500 Ω	Low is very important to reduce self-magnetization problems when direct coupling is used. OP27 I_B can be neglected.
Magnetic Phonograph Cartridges	<1500 Ω	Similar need for low I_B in direct coupled applications. OP27 will not introduce any self-magnetization problem.
Linear Variable Differential Transformer	<1500 Ω	Used in rugged servo-feedback applications. Bandwidth of interest is 400 Hz to 5 kHz.

Open-Loop Gain

Frequency at	OP07	OP27	OP37
3 Hz	100 dB	124 dB	125 dB
10 Hz	100 dB	120 dB	125 dB
30 Hz	90 dB	110 dB	124 dB

For further information regarding noise calculations, see "Minimization of Noise in Op Amp Applications," Application Note AN-15.

AUDIO APPLICATIONS

The following applications information has been abstracted from a PMI article in the 12/20/80 issue of Electronic Design magazine and updated.

Figure 7 is an example of a phono pre-amplifier circuit using the OP27 for A1; R1-R2-C1-C2 form a very accurate RIAA network with standard component values. The popular method to accomplish RIAA phono equalization is to employ frequency-dependent feedback around a high-quality gain block. Properly chosen, an RC network can provide the three necessary time constants of 3180, 318, and 75 µs.[1]

For initial equalization accuracy and stability, precision metal film resistors and film capacitors of polystyrene or polypropylene are recommended since they have low voltage coefficients, dissipation factors, and dielectric absorption.[4] (High-K ceramic capacitors should be avoided here, though low-K ceramics—such as NPO types, which have excellent dissipation factors and somewhat lower dielectric absorption—can be considered for small values.)

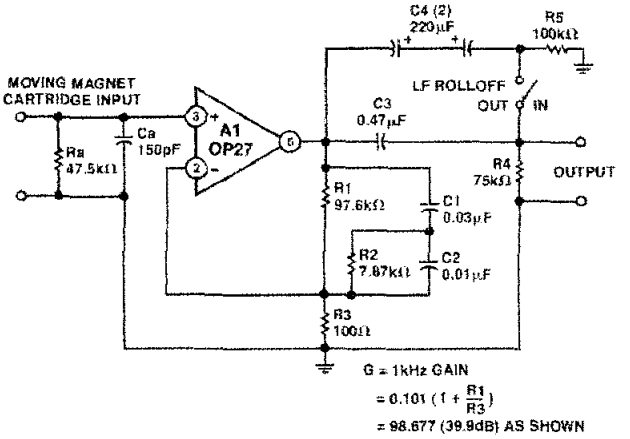


Figure 7. Phono Preamplifier Circuit

The OP27 brings a 3.2 nV/√Hz voltage noise and 0.45 pA/√Hz current noise to this circuit. To minimize noise from other sources, R3 is set to a value of 100 Ω, which generates a voltage noise of 1.3 nV/√Hz. The noise increases the 3.2 nV/√Hz of the amplifier by only 0.7 dB. With a 1 kΩ source, the circuit noise measures 63 dB below a 1 mV reference level, unweighted, in a 20 kHz noise bandwidth.

Gain (G) of the circuit at 1 kHz can be calculated by the expression:

$$G = 0.101\left(1 + \frac{R1}{R3}\right)$$

For the values shown, the gain is just under 100 (or 40 dB). Lower gains can be accommodated by increasing R3, but gains higher than 40 dB will show more equalization errors because of the 8 MHz gain-bandwidth of the OP27.

This circuit is capable of very low distortion over its entire range, generally below 0.01% at levels up to 7 V rms. At 3 V output levels, it will produce less than 0.03% total harmonic distortion at frequencies up to 20 kHz.

Capacitor C3 and resistor R4 form a simple –6 dB-per-octave rumble filter, with a corner at 22 Hz. As an option, the switch-selected shunt capacitor C4, a nonpolarized electrolytic, bypasses the low-frequency rolloff. Placing the rumble filter's high-pass action after the preamp has the desirable result of discriminating against the RIAA-amplified low-frequency noise components and pickup-produced low-frequency disturbances.

A preamplifier for NAB tape playback is similar to an RIAA phono preamp, though more gain is typically demanded, along with equalization requiring a heavy low-frequency boost. The circuit in Figure 7 can be readily modified for tape use, as shown by Figure 8.

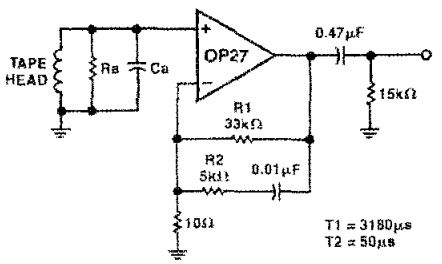


Figure 8. Tape-Head Preamplifier

While the tape-equalization requirement has a flat high-frequency gain above 3 kHz (T_2 = 50 μs), the amplifier need not be stabilized for unity gain. The decompensated OP37 provides a greater bandwidth and slew rate. For many applications, the idealized time constants shown may require trimming of R1 and R2 to optimize frequency response for nonideal tapehead performance and other factors.[5]

The network values of the configuration yield a 50 dB gain at 1 kHz, and the dc gain is greater than 70 dB. Thus, the worst-case output offset is just over 500 mV. A single 0.47 μF output capacitor can block this level without affecting the dynamic range.

The tapehead can be coupled directly to the amplifier input, since the worst-case bias current of 80 nA with a 400 mH, 100 μ inch head (such as the PRB2H7K) will not be troublesome.

One potential tapehead problem is presented by amplifier bias-current transients which can magnetize a head. The OP27 and OP37 are free of bias-current transients upon power-up or power-down. However, it is always advantageous to control the speed of power supply rise and fall, to eliminate transients.

In addition, the dc resistance of the head should be carefully controlled, and preferably below 1 kΩ. For this configuration, the bias-current-induced offset voltage can be greater than the 100pV maximum offset if the head resistance is not sufficiently controlled.

A simple, but effective, fixed-gain transformerless microphone preamp (Figure 9) amplifies differential signals from low impedance microphones by 50 dB, and has an input impedance of 2 kΩ. Because of the high working gain of the circuit, an OP37 helps to preserve bandwidth, which will be 110 kHz. As the OP37 is a decompensated device (minimum stable gain of 5), a dummy resistor, Rp, may be necessary, if the microphone is to be unplugged. Otherwise the 100% feedback from the open input may cause the amplifier to oscillate.

Common-mode input-noise rejection will depend upon the match of the bridge-resistor ratios. Either close-tolerance (0.1%) types should be used, or R4 should be trimmed for best CMRR. All resistors should be metal film types for best stability and low noise.

Noise performance of this circuit is limited more by the input resistors R1 and R2 than by the op amp, as R1 and R2 each generate a 4 nV/√Hz noise, while the op amp generates a 3.2 nV/√Hz noise. The rms sum of these predominant noise sources will be about 6 nV/√Hz, equivalent to 0.9 μV in a 20 kHz noise bandwidth, or nearly 61 dB below a 1 mV input signal. Measurements confirm this predicted performance.

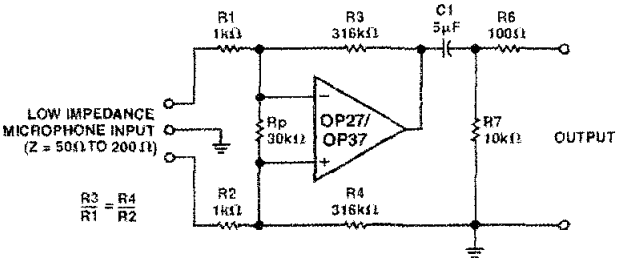


Figure 9. Fixed Gain Transformerless Microphone Preamplifier

For applications demanding appreciably lower noise, a high quality microphone transformer-coupled preamp (Figure 10) incorporates the internally compensated OP27. T1 is a JE-115K-E 150 Ω/15 kΩ transformer which provides an optimum source resistance for the OP27 device. The circuit has an overall gain of 40 dB, the product of the transformer's voltage setup and the op amp's voltage gain.

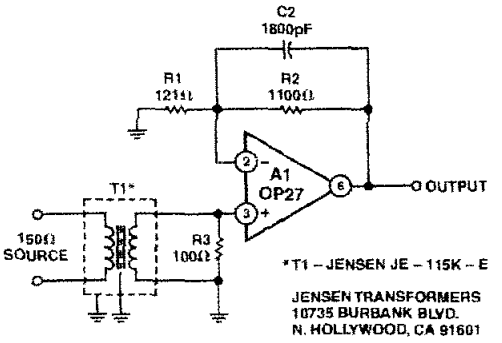


Figure 10. High Quality Microphone Transformer-Coupled Preamplifier

Gain may be trimmed to other levels, if desired, by adjusting R2 or R1. Because of the low offset voltage of the OP27, the output offset of this circuit will be very low, 1.7 mV or less, for a 40 dB gain. The typical output blocking capacitor can be eliminated in such cases, but is desirable for higher gains to eliminate switching transients.

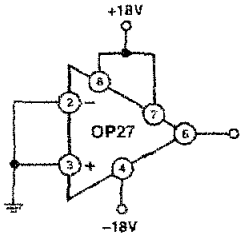


Figure 11. Burn-In Circuit

Capacitor C2 and resistor R2 form a 2 μs time constant in this circuit, as recommended for optimum transient response by the transformer manufacturer. With C2 in use, A1 must have unity-gain stability. For situations where the 2 μs time constant is not necessary, C2 can be deleted, allowing the faster OP37 to be employed.

Some comment on noise is appropriate to understand the capability of this circuit. A 150 Ω resistor and R1 and R2 gain resistors connected to a noiseless amplifier will generate 220 nV of noise in a 20 kHz bandwidth, or 73 dB below a 1 mV reference level. Any practical amplifier can only approach this noise level; it can never exceed it. With the OP27 and T1 specified, the additional noise degradation will be close to 3.6 dB (or –69.5 referenced to 1 mV).

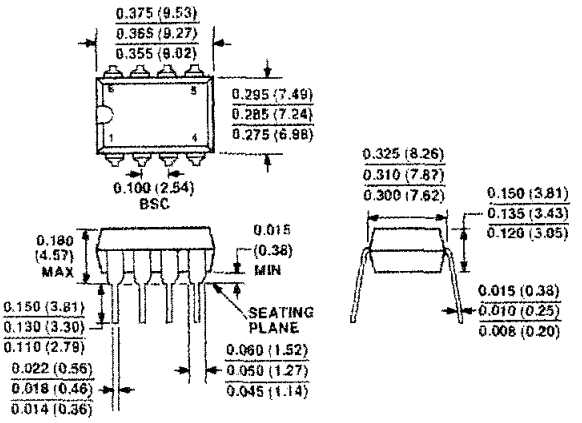
References

1. Lipshitz, S.R, "On RIAA Equalization Networks," JAES, Vol. 27, June 1979, p. 458–481.
2. Jung, W.G., *IC Op Amp Cookbook*, 2nd. Ed., H.W. Sams and Company, 1980.
3. Jung, W.G., *Audio IC Op Amp Applications*, 2nd. Ed., H.W. Sams and Company, 1978.
4. Jung, W.G., and Marsh, R.M., "Picking Capacitors," *Audio*, February and March, 1980.
5. Otala, M., "Feedback-Generated Phase Nonlinearity in Audio Amplifiers," London AES Convention, March 1980, preprint 1976.
6. Stout, D.F., and Kaufman, M., *Handbook of Operational Amplifier Circuit Design*, New York, McGraw-Hill, 1976.

OUTLINE DIMENSIONS

8-Lead Plastic Dual-in-Line Package [PDIP]
(N-8)

Dimensions shown in inches and (millimeters)

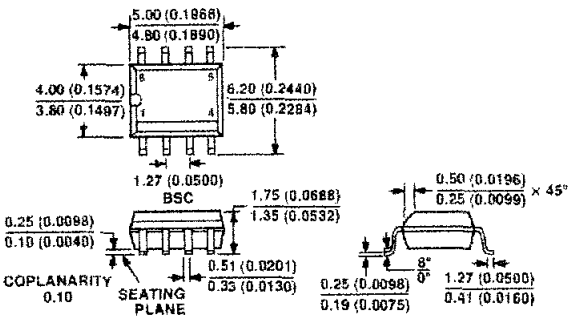


COMPLIANT TO JEDEC STANDARDS MO-095AA

CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETERS DIMENSIONS (IN PARENTHESES)

8-Lead Standard Small Outline Package [SOIC]
Narrow Body
(R-8)

Dimensions shown in millimeters and (inches)

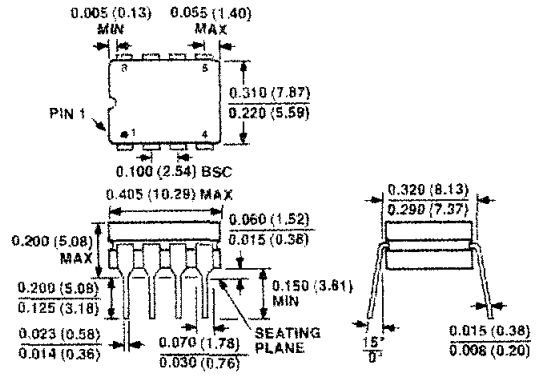


COMPLIANT TO JEDEC STANDARDS MS-012AA

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

8-Lead Ceramic DIP – Glass Hermetic Seal [CERDIP]
(Q-8)

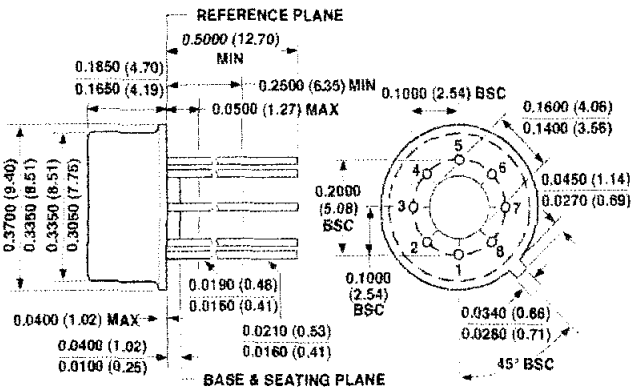
Dimensions shown in inches and (millimeters)



CONTROLLING DIMENSIONS ARE IN INCH; MILLIMETERS DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

8-Lead Metal Can [TO-99]
(H-08)

Dimensions shown in inches and (millimeters)



COMPLIANT TO JEDEC STANDARDS MO-002AK

CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETERS DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Revision History

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1/03—Data Sheet changed from REV. B to REV. C.	
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Edits to ABSOLUTE MAXIMUM RATINGS	7
Updated OUTLINE DIMENSIONS	16
9/02—Data Sheet changed from REV. A to REV. B.	
Edits to Figure 8	14
Edits to OUTLINE DIMENSIONS	16
9/01—Data Sheet changed from REV. 0 to REV. A.	
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Edits to PACKAGE TYPE	2
Edits to ELECTRICAL CHARACTERISTICS	2, 3
Edits to WAFER TEST LIMITS	4
Deleted TYPICAL ELECTRICAL CHARACTERISTICS	4
Edits to BURN-IN CIRCUIT figure	7
Edits to APPLICATION INFORMATION	8

LAMPIRAN C

Turbidity

What is Turbidity?

Turbidity, or cloudiness, in water is caused by a variety of suspended materials. The material can be both organic (plankton, sewage) and inorganic (silt, clay). The suspended material will scatter and absorb light passing through the water. The light scattered back to the observer can be affected so that the water will have a color dependent upon the type and amount of suspended matter. The cloudiness and color can be observed also if a sample of water in a transparent container is held between the observer's eye and a light source. It is this fact that is used in the turbidity meter.

What is a Turbidity Meter?

The turbidity meter measures the clarity of a water sample. A beam of light is shown through the water sample. The turbidity, o its converse clarity, is read on a numerical scale.

The turbidity meter contains a source of light, a photocell, and a meter. The path of the light is 90 degrees to the direction in whic the photocell points. When a sample is placed in the light beam, light scattered by the suspended material in the sample is detec by the photocell. The photocell converts the scattered light into a electrical current that is sent through the meter. The position of t needle on the meter or a digital read-out gives an indication of th turbidity of the water sample.

Turbidity determined by the technique described above is referre to as the nephelometric method from the root meaning "cloudiness". This word is used to form the name of the unit of turbidity, the NTU. This acronym stands for Nephelometric Turbidity Unit.

The meter reading cannot be used to compare the turbidity of different water samples unless the instrument is calibrated. The aquatic science instructors calibrate the meter regularly. Calibration consists of adjusting the meter reading to a known value when a standard sample is placed in the lig beam. A standard suspension is often made from a polymer called Formazin which has greater reproducibility.

What is the significance of turbidity?

Turbidity relates to the effect that suspended particles have on water clarit High turbidity readings (low clarity) can indicate erosion and sedimentatior problems. Rainfall and runoff can increase the suspended solid load in a river and make the river appear cloudy or muddy. High biological productiv related to increases in nutrients and temperature can result in increases o diatoms and other algae that contribute to turbidity. Turbidity meters can b used to estimate plankton density.

River plumes that are rich in organic matter and suspended solids are clea differentiated from the Lake Michigan water as they enter they lake. Turbic readings in Lake Michigan are likely to range from 0.1 to 2.5 NTU. The

Grand River often ranges from 2 to 9 NTU. Spring Lake and Muskegon La have typical readings ranging between 0.1 and 4 NTU.

Elevated turbidity can cause an increase in temperature since suspended particles absorb heat. Reduction of light penetrating the water column due to turbidity can decrease the rate of photosynthesis. This, in turn, can decrease the amount of dissolved oxygen in the water. As suspended particles settle, they can impair the habitat needed for fish spawning and aquatic macroinvertebrates. They can also clog the gills of fish and the breathing apparatus of invertebrates Particles serve as places of attachment for harmful microorganisms and toxic materials. Turbidity in drinking water is decreased through the process of flocculation, which involves addition of alum or a mixture of iron, lime, and chloride to cause solids to settle out.

Instructions for use of a Turbidity Meter:

1. Using specially marked beakers found in the main cabin, obtain samples of water from the water sampling devices (Van Dorn Bottles) located on the rear deck. Use the beaker marked **TURB T** to obtain 50 mL of the top water sample from the Van Dorn bottle marked "T". Use t beaker marked **TURB B** to obtain 50 mL of the bottom water sample from the Van Dorn bottl marked "B". Be sure to match the symbols on the beakers with the same symbol on the Van Dorn bottle (the symbol "T" for top and "B" for bottom).
2. Bring the beakers containing the water samples back to the turbidity lab station in the main cabin. Measure the top water sample first then measure the bottom water sample.
3. Select the empty SAMPLE cell (cuvette). Rinse the cell two times with the water sample and the cell to the line (about 15 mL) with the top "T" sample, taking care to handle the sample c by the top only. Put the cap on the cell and wipe the cell with a soft, lint-free cloth to remove water spots and fingerprints.
4. Press the ON/OFF (I/O) key to turn on the turbidity meter. Gently invert the sample cell 2-3 times and place the sample cell in the instrument cell compartment. Be sure the cell is lined at the marks.
5. Close the lid. Press READ. Record the turbidity reading after the lamp symbol turns off. The display will show the turbidity reading in NTUs.
6. Record the meter reading in NTU units for the top sample in the appropriate place (TURB T) the data board then empty and rinse the sample cell with deionized water.
7. Repeat steps 3 through 6 with the bottom "B" water sample. Record the meter reading in NT units for the bottom sample in the appropriate place (TURB B) on the data board then empty and rinse the sample cell. When you are finished clean all materials and store them as they were when you started.

Instructions for use of a Turbidity Tube

Another way to study water clarity is to use a turbidity tube (Figure 10). Pour water drawn in a bucke into the tube until the image at the bottom of the tube is no longer visible when looking directly throu the water column. Rotate the tube while looking down at the image to see if the black and white are of the decal are distinguishable. Record this depth of water to the nearest 1 cm. Enter data for each observer, not the average of the different observations. If you can still see the image on the bottom the tube after filling it, simply record the depth as greater than (>) the depth of the tube.

To make a turbidity tube:

1. Put a PVC cap over one end of 3-4-foot clear tube such as a fluorescent light protector. The cap should fit tightly so water cannot leak out.
2. Cut a disk from wood, plastic, or cardboard the same size as the tube diameter.
3. Divide the disk into fourths. Paint alternating quadrants black and white. Seal the disk by laminating or painting with varnish to make it waterproof.
4. Glue the disk in the bottom of the tube, painted side facing up (toward the open end of the tube).
5. Use a marker and meter stick to make a scale on the side of the tube, beginning with 0 cm a the top of the disk.

Source: Global Learning and Observations to Benefit the Environment (GLOBE)

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Instructor's Manual Index

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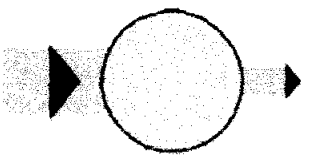
conzelmj@gvsu.edu

GRAND VALLEY STATE UNIVERSITY

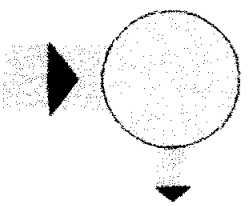
Contents

Turbidity value

The turbidity value is the quantitative statement of the qualitative phenomenon of turbidity. The objective of measuring turbidity is to obtain information on the concentration of scattering particles in a medium (solids concentration). This can be done by either of two fundamentally different methods: determination of the light loss of the transmitted beam (scatter coefficient) or determination of the intensity of the light scattered sideways. The scatter coefficient represents the total scattered light that has been withdrawn from the incident beam, while the scatter intensity states how much scattered light has been deflected at a given angle.



Determination of the light loss of the transmitted beam



Measurement of the light scattered sideways

Both variables are proportional to the particle concentration and are therefore suitable for measuring turbidity. But they differ in their applicability at various concentration levels. Measurement of the scatter intensity permits the detection of lower concentrations, while transmission measurement is used for higher concentrations. The reason for this is the phenomenon of multiple scatter. At low concentrations, the light scattered by a given particle has room to propagate freely (simple scatter). At higher concentrations, however, two things happen: the particles closer to the light source tend to screen off the incident light, and the scattered light can no longer propagate freely. As a result, the scatter intensity no longer increases in proportion to the concentration.

Simple scatter is limited to about 10 FTU. In practice, however, electronic linearization makes it possible to use scatter intensity measurement for much higher measuring ranges (up to 2000 FTU). The lowest measurable turbidity

level depends on how much stray light is present.

Measurement of the light loss of the transmitted beam permits the detection of high concentrations, but is limited at the lower levels. The trouble is that a large number of particles are necessary to detect the reduction of transmitted light reliably. In practice, transmission measurement covers a span from 50 FTU to 20,000 FTU.

Practical interpretation of the turbidity value is achieved by comparison with a standard suspension, i.e. turbidimeters are calibrated with a reference solution (usually formazine). An instrument that has been calibrated with formazine will measure any formazine concentration correctly. When it comes to other turbid media, one cannot be certain of a direct correlation between turbidity value and solids concentration, because the reading will be affected also by the particle size and the refractive index of the particles in relation to the medium.

Attempts to compare the readings produced by different instruments are admissible only if they have the same characteristics with regard to wavelength of the light, scatter angle, optical configuration, calibration and color compensation. For continuous measurements in industrial processes, the measuring technique applied (photometer) is also extremely important because of the need for high stability.

Last update: 2004-05-14.

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AIR MINUM DALAM KEMASAN

PENDAHULUAN

Standar Nasional Indonesia (SNI) Air Minum dalam Kemasan merupakan Revisi SNI 01-3553-1994.
Revisi ini selain diutamakan untuk melindungi konsumen dari segi kesehatan dan keselamatan juga untuk:

a. melindungi produsen
b. mendukung perkembangan agro indsutri
c. mendukung ekspor non migas
d. menunjang instruksi Menteri Perindsutrian No. 04/M/INS/10/1989 tentang Pengawasan Makanan.

Standar ini telah dibahas melalui rapat-rapat teknis pra Konsensus dan terakhir di Rapat Konsensuskan pada tanggal 22 Maret 1995 di Jakarta.

Hadir dalam rapat tersebut pihak Konsumen, Produsen, Asosiasi, Iptek serta Instansi terkait.

Standar ini disusun berdasarkan acuan:

1. Hasil analisis contoh Air Minum dalam Kemasan di Balai Besar Litbang Industri Hasil Pertanian Bogor.
2. SNI 01-3553-1994, Air Minum dalam Kemasan.
3. SNI 01-3554-1994, Cara Uji Air Minum dalam Kemasan.
4. PERMEN. KES.RI. No. 416/MENKES/PER/IX/1990.
5. World Health Organization Drinking Water Standart.
6. Australian Standards (yang disampaikan pada Asia Pacific Food Industry August 1991).
7. Codex Alimentarius Commison (Codex Standard 108-1998)
8. Kumpulan Perudang-undangan di Bidang Makanan Jilid I edisi III Departemen Kesehatan RI 1993-1994.
9. SNI-19-0429-1989, Petunjuk Pengambilan Contoh Cairan dan Semi Padatan.

DAFTAR ISI

2. DEFINISI
3. SYARAT MUTU
4. CARA PENGAMBILAN CONTOH
5. CARA UJI
6. CARA PENGEMASAN
7. SYARAT PENANDAAN

AIR MINUM DALAM KEMASAN

1. RUANG LINGKUP

Standar ini meliputi definisi, syarat mutu, cara pengambilan contoh, cara uji, cara pengemasan dan syarat penandaan.

2. DEFINISI

Air minum dalam kemasan adalah air yang telah diolah/diproses, dikemas dan aman diminum.

3.SYARAT MUTU

NO.	KRITERIA UJI	SATUAN	PERSYARATAN
1.	*Keadaan*		
1.1	Bau	-	Tidak Berbau
1.2	Rasa	-	Normal
1.3	Warna	Unit PtCo	Maks. 5
2.	PH	-	6,5 - 8,5
3.	Kekeruhan	NTU	Maks. 5
4.	Kesadahan, Sebagai $CaCO_3$	Mg/l	Maks 150
5.	Zat yang larut	Mg/l	Maks. 500
6.	Zat Organik (angka $KmnO_4$)	Mg/l	Maks. 1,0
7.	Nitrat dihitung sebagai (NO_3)	Mg/l	Maks. 45
8.	Nitrit dihitung sebagai (NO_2)	Mg/l	Maks. 0,005
9.	Amonium (NH_4)	Mg/l	Maks. 0,15
10.	Sulfat (SO_4)	Mg/l	Maks. 200
11.	Klorida (Cl)	Mg/l	Maks. 250
12.	Fluorida (F)	Mg/l	Maks. 1
13.	Sianida (CN)	Mg/l	Maks. 0,05
14.	Besi (Fe)	Mg/l	Maks. 0,3
15.	Mangan (Mn)	Mg/l	Maks. 0,05
16.	Klor Bebas	Mg/l	Maks. 0,1
17.	*Cemaran Logam*		
17.1	Timbal (Pb)	Mg/l	Maks. 0,005
17.2	Tembaga (Cu)	Mg/l	Maks. 0,5

17.3	Kadmium (Cd)	Mg/l	Maks. 0,005
17.4	Raksa (Hg)	Mg/l	Maks. 0,001
18.	Cemaran Arsen (As)	Mg/l	Maks. 0,05
19.	Cemaran Mikroba:		
19.1	Angka lempeng total awal*)	Koloni/ml	Maks. $1,0 \times 10^2$
19.2	Angka lempengan total	Koloni/ml	Maks. $1,0 \times 10^5$
19.3	Bakteri bentuk coli	APM/100 ml	< 2
		Koloni/100 ml	Nol
19.4	C. perfringens	-	Negatif/100 ml
19.5	Salmonella	-	Negatif/100 ml

*) DI Pabrik
**) Di Pasaran

4. CARA PENGAMBILAN CONTOH

Cara pengambilan contoh sesuai dengan SNI 19-0429-1989, Petunjuk Pengambilan Contoh Cairan dan Semi Padat.

5. CARA UJI

5.1. Persiapan Contoh
Homogenkan contoh dengan cara mengocok, membolak-balikkan kemasan ke atas dan ke bawah.

5.1.1. Keadaan
Cara uji keadaan (bau dan rasa) sesuai SNI 01-3554-1994, Cara Uji Air Minum dalam Kemasan butir 2.2.

5.1.2. Warna
Cara Uji Warna sesuai dengan SNI 01-3554-1994, butir 2.1.

5.2. pH
Cara uji pH sesuai SNI 01-3554-1994, butir 3.

5.3. Kekeruhan
Cara uji kekeruhan sesuai SNI 01-3554-1994, butir 4.

5.4. Kesadahan
Cara Uji Kesadahan sesuai SNI 01-3554-1995, butir 5.

5.5. Zat yang terlarut (Residu Terlarut)

Cara uji zat yang terlarut sesuai SNI 01-3554-1994, butir 6.

5.6. Zat Organik
Cara uji Zat Organik sesuai SNI 01-3554-1994, butir 7.

5.7. Nitrat
Cara uji Nitrat sesuai SNI 01-3554-1994, butir 8.

5.8. Nitrit
Cara Uji Nitrit sesuai SNI 01-3554-1994, butir 9.

5.9. Amonium
Cara Uji Amonium sesuai SNI 01-3554-1994, butir 10.

5.10. Sulfat
Cara Uji Sulfat sesuai SNI 01-3554-1994, butir 11.

5.11. Klorida
Cara Uji Klorida sesuai SNI 01-3554-1994, butir 13.

5.12. Fluorida
Cara Uji Fluorida sesuai SNI 01-3554-1994, butir 14.

5.13. Sianida
Cara Uji Sianida sesuai Sni 01-3554-1994, butir 15.

5.14. Besi
Cara Uji Besi sesuai SNI 01-3554-1994, butir 16.

5.15. Mangan
Cara Uji Mangan sesuai SNI 01-3554-1994, butir 17.

5.16. Klor Bebas
Cara Uji Klor Bebas sesuai SNI 01-3554-1994, butir 20.

5.18. Cenaran Logam

5.18.1.Timbal
Cara uji Timbal sesuai SNI 01-3554-1994, butir 18.1.

5.18.2.Tembaga
Cara Uji Tembaga sesuai SNI 01-3554-1994, butir 18.2.

5.18.3.Kadmium
Cara Uji Kadmium sesuai SNI 01-3554-1994, butir 18.3.

5.18.4.Raksa
Cara Uji Raksa sesuai SNI 01-3554-1994, butir 18.4.

5.19. Cemaran Arsen
Cara uji cemaran arsen sesuai SNI 01-3554-1994, butir 19.

5.20. Cemaran Mikroba
5.20.1.Cara uji cemaran Mikroba sesuai SNI 01-3554-1994, butir 21
5.20.2. Analisis Coliform Metode Penyaringan (Membran Filter).
5.20.2.1. Prinsip
Pertumbuhan bakteri coliform setelah contoh di inkubasikan dalam pembenihan yang cocok selama 24-48 jam pada suhu 36 ± 1^0 C.

5.20.2.2. Peralatan
a. pipet ukur 10 ml atau gelas ukur 100 ml
b. cawan petri ϕ 50 - 60 mm
c. penyaring membran 0,45
d. pinset
e. unit alat penyaringan (filtration unit)
f. lemari pengeram 36 ± 1^0 C.

5.20.2.3. Pembenihan
Violet red bile agar.

5.20.2.4. Cara Kerja
a. pasang peralatan penyaring membran yang terdiri dari corong, membran penyaring dan penampung yang telah disterilkan lebih dahulu, dan hubungkan dengan vakum Sistem;
b. masukkan 100 ml cuplikan contoh atau sejumlah yang diperlukan ke dalam corong dari alat penyaring dengan menggunakan pipet atau gelas ukur steril;
c. pergunakan vakum untuk menyaring cuplikan melalui membran dan saring cuplikan seluruhnya;
d. bilas seluruh permukaan dalam corong penyaring denganair pengencer atau air suling steril yang jumlahnya sama dengan jumlah cuplikan yang disaring dan saring cairan pembilas;
e. sesudah pembilasan selesai, hentikan vakum;
f. buka kembali peralatan penyaring dan dengan pinset yang steril angkat membran penyaring dari alat penyaring;

g. letakkan membran penyaring di atas perbenih-violet red bile agar dalam cawan petri (usahakan jangan ada gelembung udara di bawah membran);
h. inkubasikan cawan dengan posisi terbalik pada 36 ± 1^0 C selama 48 jam;
i. hitung koloni yang berwarna merah gelap yang berukuran 0,5 mm atau lebih pada membran yang menyatakan jumlah bakteri coliform dalam 100 ml contoh.

6. CARA PENGEMASAN

Produk dikemas dalam wadah yang tertutup rapat, tidak dipengaruhi atau mempengaruhi isi. Produk disimpan dan diangkut dengan cara yang baik dan benar.

7. SYARAT PENANDAAN

Syarat penandaan sesuai dengan UU RI. No. 23 Tahun 1992 tentang Kesehatan serta peraturan tentang label dan periklanan yang berlaku.