LAMPIRAN

LAMPIRAN 1

Program Pada Mikrokontroller

```
;KONSTANTA LCD
DISPCLR     EQU  00000001B       ;DISPLAY CLEAR
FUNCSET     EQU  00111000B       ;INTERFACE DATA LENGTH :8 BITS
ENTRMOD     EQU  00000110B       ;INCREMENT, NO DISPLAY SHIFT
DISPON      EQU  00001100B       ;DISPLAY ON, CURSOR OFF, BLINK
OFF
CURSOR      EQU  00001110B       ;DISPLAY ON, CURSOR ON, BLINK
OFF
BLINK       EQU  00001101B       ;DISPLAY ON, CURSOR OFF, BLINK
ON

detsd    equ    08h
detpd    equ    09h
mensd    equ    0ah
menpd    equ    0bh
detsu    equ    0ch
detpu    equ    0dh
mensu    equ    0eh
menpu    equ    0fh

adagerakan equ  10h
tunggu_ac  equ  11h
                ORG   00h

                AJMP  START

                org   30h

POSISI2.1:      MOV   A,r7
POSISI2:        ADD   A,#11000000B
                SJMP  POSISI.SUB

POSISI1.1:           MOV   A,r6
POSISI1:        ADD   A,#10000000B
                SJMP  POSISI.SUB

POSISI.SUB:     dec   A
                ACALL      CONTROLOUT
                RET

PRINTSTRING2:
     ACALL      POSISI2.1
                SJMP  PRINTSTRING

PRINTSTRING1:
                ACALL      POSISI1.1

PRINTSTRING:
                SJMP  OUTSTRING
```

```
PRINTSTRINGLOOP: ACALL      DATAOUT
                 INC   DPTR

OUTSTRING:       CLR   A
                 MOVC  A,@A+DPTR
                 JNZ   PRINTSTRINGLOOP
                 RET

CONTROLOUT:
                 PUSH  DPH
                 PUSH  DPL
                 clr   p2.0
                 SJMP  LCD.OUT

DATAOUT:         PUSH  DPH
                 PUSH  DPL
                 setb        p2.0

LCD.OUT:
                 MOV   p1,A
                 setb  p2.1
                 clr   p2.1

DELAY.LCD:            MOV   r2,#250
                 DJNZ  r2,$
                 POP   DPL
                 POP   DPH
                 RET

DELAY.INIT.LCD:  MOV   R2,#20H
DLY.LCD.LP:      MOV   R3,#200
                 DJNZ  R3,$
                 DJNZ  R2,DLY.LCD.LP
                 RET

INIT.LCD:        MOV   A,#DISPCLR
                 ACALL       CONTROLOUT
                 ACALL       DELAY.INIT.LCD
                 MOV   A,#FUNCSET
                 ACALL       CONTROLOUT
                 MOV   A,#DISPON
                 ACALL       CONTROLOUT
                 MOV   A,#ENTRMOD
                 ACALL       CONTROLOUT
                 RET


DELAYdetik       MOV   R2,#255
DELdet:               MOV   R3,#50
                 jnb   p2.5,terus6
                 mov      detsd,#01h
```

```
                mov     detpd,#00h
                mov     mensd,#05h
                mov     menpd,#00h
                mov   adagerakan,#01h
                clr   p0.0
                ajmp  terus4
terus6:         mov   adagerakan,#00h
terus4:         DJNZ  R3,$
                DJNZ  R2,DELdet
                RET

DELAY4M         MOV   R2,#255
DEL4M:          MOV   R3,#255
                DJNZ  R3,$
                DJNZ  R2,DEL4M
                RET

timerdown       mov     r1,detsd
                cjne    r1,#0,lom1
                mov     detsd,#9
                mov     r1,detpd
                cjne    r1,#0,lom2
                mov     detpd,#5
                mov     r1,mensd
                cjne    r1,#0,lom3
                mov     mensd,#9
                mov     r1,menpd
                cjne    r1,#0,lom4
                mov     menpd,#5
                ajmp  terus
lom1:           dec     detsd
                ajmp    terus
lom2:           dec     detpd
                ajmp    terus
lom3:           dec     mensd
                ajmp    terus
lom4:           dec     menpd
terus:          ret

timerup         mov     r1,detsu
                cjne    r1,#9,lomu1
                mov     detsu,#0
                mov       r1,detpu
                cjne    r1,#5,lomu2
                mov     detpu,#0
                mov     r1,mensu
                cjne    r1,#9,lomu3
                mov     mensu,#0
                mov     r1,menpu
                cjne    r1,#6,lomu4
                mov     menpu,#0
lomu1:          inc     detsu
```

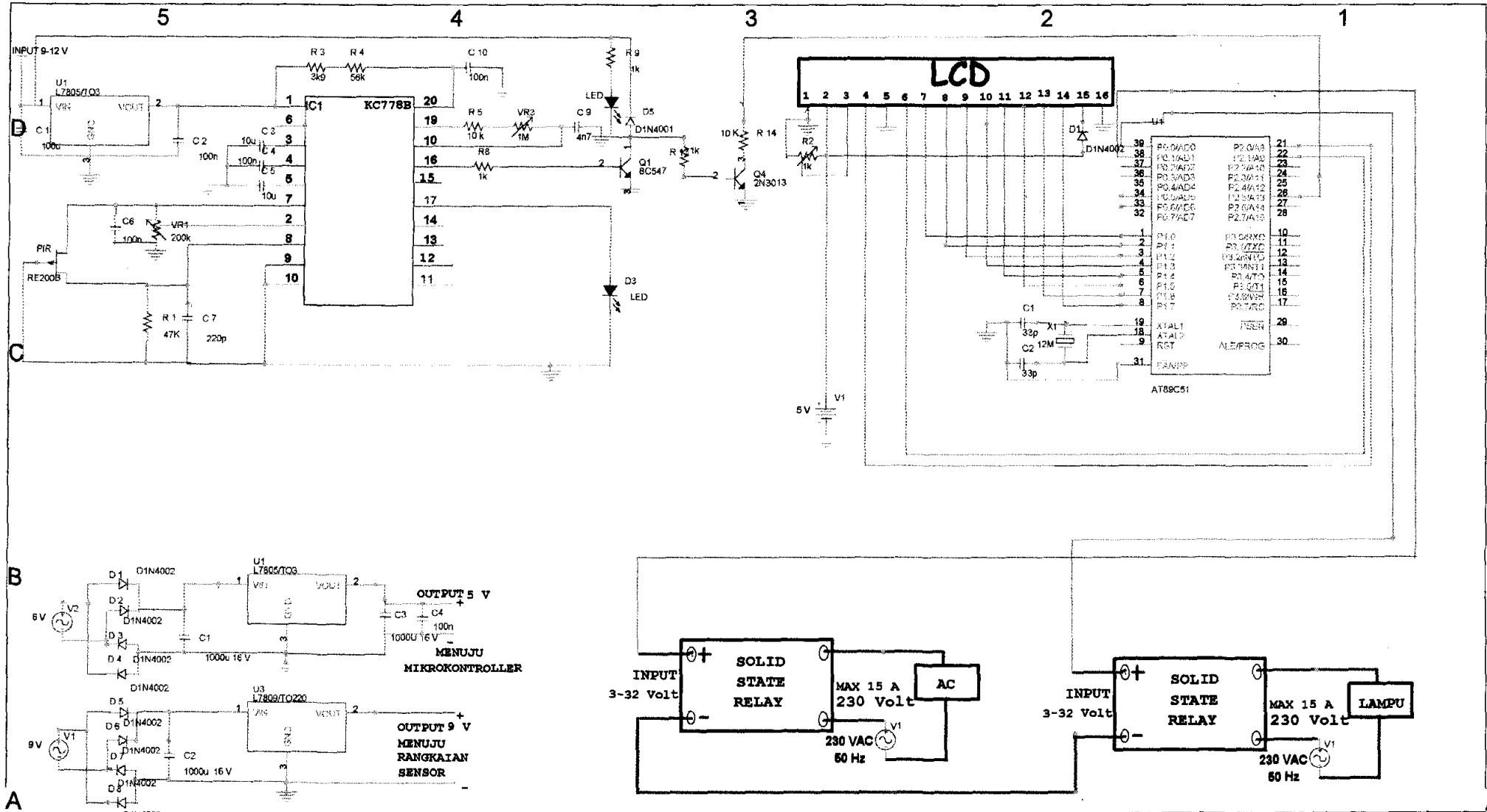
```
                ajmp    terus1
lomu2:          inc     detpu
                ajmp    terus1
lomu3:          inc     mensu
                ajmp    terus1
lomu4:          inc     menpu
terus1:                 ret

tampilan
                 mov     r7,#5
                acall   posisi2.1
                 mov     a,detsd
                 add   a,#30h
                acall   dataout
                mov     r7,#4
                acall   posisi2.1
                mov     a,detpd
                 add   a,#30h
                acall   dataout
                mov     r7,#3           ;14
                acall   posisi2.1
                mov     a,#':'
                acall   dataout
                mov     r7,#2           ;13
                acall   posisi2.1
                mov     a,mensd
                 add    a,#30h
                acall   dataout
                mov     r7,#1
                acall   posisi2.1
                mov     a,menpd
                 add    a,#30h
                acall   dataout

                 mov     r7,#16
                acall   posisi2.1
                 mov     a,detsu
                 add    a,#30h
                acall   dataout
                mov     r7,#15
                acall   posisi2.1
                mov     a,detpu
                 add    a,#30h
                acall   dataout
                mov     r7,#14
                acall   posisi2.1
                mov     a,#':'
                acall   dataout
                mov     r7,#13
                acall   posisi2.1
                mov     a,mensu
                add   a,#30h
```

```
                acall   dataout
                mov     r7,#12
                acall   posisi2.1
                mov     a,menpu
                add   a,#30h
                acall   dataout
                ret

START:          MOV   SP,#60H
                mov   r6,#1
                mov   r7,#1
                mov     detsd,#00h
                mov     detpd,#00h
                mov     mensd,#05h
                mov     menpd,#00h
                mov     detsu,#00h
                mov     detpu,#00h
                mov     mensu,#00h
                mov     menpu,#00h
                setb  p0.0
                setb  p0.1
                ;clr  p2.5
                mov   adagerakan,#00h
                mov   tunggu_ac,#00h
                ACALL       INIT.LCD
                mov   dptr,#tul1
                acall printstring1
                mov   dptr,#tul2
                acall printstring2

                mov   r4,#2
ulang3:         mov   a,#90
ulang:          acall delay4m
                djnz  a,ulang
                djnz  r4,ulang3

                mov   a,#dispclr
                acall controlout

                acall delay4m
                mov   r6,#7
                acall posisi1.1
                mov   A,#17
                acall dataout
                mov   r6,#8
                acall posisi1.1
                mov   A,#16
                acall dataout
                acall       tampilan

MAIN:
```

```
                jnb   p0.0,ada_gerakan
                mov   r6,#1
                mov   dptr,#tul3
                acall printstring1
                mov   r6,#9
                mov   dptr,#tul5
                acall printstring1
                ajmp  terus2
ada_gerakan:
                mov   r6,#9
                mov   dptr,#tul6
                acall printstring1
                acall   timerdown
                acall tampilan

                mov     r1,detsd
                cjne    r1,#00h,terus3
                mov     r1,detpd
                cjne    r1,#00h,terus3
                mov     r1,mensd
                cjne    r1,#00h,terus3
                mov     r1,menpd
                cjne    r1,#00h,terus3

                setb  p0.0
                setb  p0.1
                mov   adagerakan,#00h
                mov   tunggu_ac,#00h
                mov     detsd,#01h
                mov     detpd,#00h
                mov     mensd,#05h
                mov     menpd,#00h
                mov     detsu,#00h
                mov     detpu,#00h
                mov     mensu,#00h
                mov     menpu,#00h

terus3:
                jb     p0.0,terus2
                jnb    p0.1,terus2

                mov     r1,tunggu_ac
                cjne    r1,#00h,terus5

                acall timerup

terus5:         mov     r1,detsu
                cjne    r1,#00h,terus2
                mov     r1,detpu
                cjne    r1,#00h,terus2
                mov     r1,mensu
                cjne    r1,#05h,terus2
```

```
                mov     r1,menpu
                cjne    r1,#00h,terus2
                mov     tunggu_ac,#01h

                mov     r1,adagerakan
                cjne    r1,#01h,terus2

                clr   p0.1
                mov   r6,#1
                mov   dptr,#tul4
                acall printstring1

terus2:
                mov   r0,#38
ulang1:         acall delaydetik
                cjne  r0,#19,lom18
                sjmp  tutime
lom18:          cjne  r0,#18,lom17
                sjmp  tutime
lom17:          cjne  r0,#17,lom16
                sjmp  tutime
lom16:          cjne  r0,#16,lom15
                sjmp  tutime
lom15:          cjne  r0,#15,lom14
                sjmp  tutime
lom14:          cjne  r0,#14,lom13
                sjmp  tutime
lom13:          cjne  r0,#13,lom12
                sjmp  tutime
lom12:          cjne  r0,#12,lom11
                sjmp  tutime
lom11:          cjne  r0,#11,lom10
                sjmp  tutime
lom10:          cjne  r0,#10,lom09
                sjmp  tutime
lom09:          cjne  r0,#09,lom08
                sjmp  tutime
lom08:          cjne  r0,#08,lom07
                sjmp  tutime
lom07:          cjne  r0,#07,lom06
                sjmp  tutime
lom06:          cjne  r0,#06,lom05
                sjmp  tutime
lom05:          cjne  r0,#05,lom04
                sjmp  tutime
lom04:          cjne  r0,#04,lom03
                sjmp  tutime
lom03:          cjne  r0,#03,lom02
                sjmp  tutime
lom02:          cjne  r0,#02,lom01
                sjmp  tutime
lom01:
```

```
tukos:          mov   r7,#7
                mov   dptr,#tul8
                acall printstring2
                sjmp  tupop
tutime:         mov   r7,#7
                mov   dptr,#tul7
                acall printstring2
tupop:          dec   r0
                cjne  r0,#0,ulang1
                aJMP MAIN


tul1 db 'Adjusting Sensor',0
tul2 db 'Wait a Minute...',0
tul3 db 'AC:Off',0
tul4 db 'AC:On ',0
tul5 db 'Lamp:Off',0
tul6 db ' Lamp:On',0
tul7 db 'time',0
tul8 db '    ',0
```



Title	RANGKAIAN LENGKAP SENSOR PIR DAN MIKROKONTROLER	
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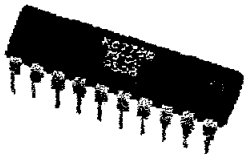
Date: Saturday, January 19, 2002	Sheet 1 of 1	

General :

The MPCC has been designed for easy implementation of AC control functions that use a Passive Infra-Red (PIR) motion detector. Due to its high sensitivity and reliability, it is also widely used in security product.

- Minimum external component
- High senstivity
- High RFI immunity
- Daylight adjustment
- Off delay timer



20 pin DIP

20 pin SOIC

Features:

A) Circuit design maximizes performance while minimizing external component count and board layout space.
B) Low cost solution for PIR motion control switching applications.
C) High sensitivity PIR input with special noise cancellation circuitry.
D) Choice of two PIR gain settings: 62 db and 68 db.
E) Adjustable PIR sensitivity.
F) Internal switched capacitor bandpass filter reduces external component count and improves reliability by minimizing sensitivity to external component values.
G) RFI noise immunity exceeds 30 V/m from 1 MHz to 1000 MHz.
H) High immunity to line frequency noise.
I) Daylight detector circuitry is designed to use either silicon photo diode or CdS detector.
J) Adjustable daylight detector sensitivity.
K) Adjustable OFF timer accuracy is determined by external components.
L) Output can directly drive TRIACs, opto-couplers and small relays (no buffering required).
M) Four main operating modes can be used in any combination:

1)Auto-ON: Load turns on when motion is detected (adjustable sensitivity).
Adjustable daylight detector disables Auto-ON during daytime.
Auto-ON mode can be disabled.
Daylight detector can be disabled.

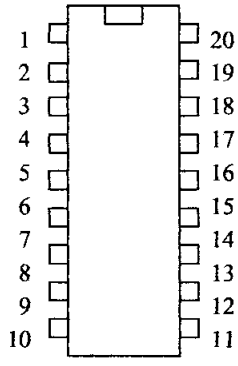
2)Auto-OFF: Adjustable OFF timer activates whenever motion stops.
Load turns off if there is no motion during the time delay.
If Auto-ON mode is disabled, the load will turn on if there is motion within 6 seconds after turn-off. (If the load goes off because you stopped moving (reading a book for example), you have 6 seconds to wave your arm to turn the load back on.)
Auto-OFF mode can be disabled.

3)Manual-ON: Load turns on manually, with a momentary contact switch.

4)Manual-OFF: Load turns off manually, with a momentary contact switch.
Load will remain off for 25 seconds, even if there is motion during this time (to give you time to leave the room).

N) If the ON/AUTO/OFF input is held either high or low, the load will be held ON or OFF respectively, overriding all other modes, until the input returns to the AUTO position.
O) If the Toggle input is held low, the load will change from on to off or from off to on, and will be held in that state, overriding all other modes, until the input returns high.
P) When power is restored after an outage, the load will be OFF and motion will be ignored for 25 seconds.
Q) Operating chip voltage is 4 - 15V.
R) Operating chip current is typically 300 μA.
S) Chip is ESD protected to more than 1000 V (human body model).
T) Operates with 50-60 Hz AC line frequency.

Pin Assignment :



20 pin DIP or SOIC

Pin	Name	Description
1	Vcc	Supply Voltage (5 V)
2	Sensitivity Adjust	PIR Motion Sensitivity Input
3	Offset Filter	PIR Motion Offset Filter
4	Anti-Alias	PIR Anti-Alias Filter
5	DC CAP	PIR Gain Stabilization Filter
6	VReg	Voltage Regulator Output
7	Pyro (D)	Pyro Drain Reference
8	Pyro (S)	Pyro Source Input Signal
9	Gnd (A)	Analog Circuitry Ground
10	Gnd (D)	Digital Circuitry Ground
11	Daylight Adjust	Daylight Adjustment and CdS Input
12	Daylight Sense	Silicon Photo Diode Input
13	Gain Select	PIR Gain Select Tri-State Input
14	ON/AUTO/OFF	Mode Select Tri-State Input
15	Toggle	Mode Select Toggle Input
16	OUT	Lights ON/OFF Output
17	LED	PIR Motion Indicator Output
18	C	OFF Timer Oscillator Input
19	R	OFF Timer Oscillator Output
20	FRef	Frequency Reference Oscillator

Pin Descriptions

1. **Vcc :** This is the regulated supply voltage to the chip (nominally 5 V).

2. **Sensitivity Adjust:** This pin is used to adjust the sensitivity threshold of the motion comparators. When the voltage on this pin equals the pyro drain reference voltage on pin 7 the PIR sensitivity will be minimum (±500 mV). When the voltage on this pin is Gnd the PIR sensitivity will be maximum (±125 mV). Intermediate voltages will provide intermediate sensitivities.

3. **Offset Filter:** This pin connects to an external capacitor of 10 μF and holds the average value of the switched capacitor bandpass filter output. Motion is detected when the difference between this average and the actual filter output is greater than the sensitivity setting. The output of the switched capacitor bandpass filter can be seen directly on this pin if the external capacitor is disconnected, however, motion will not be detected under these conditions.

4. **Anti-Alias:** This pin connects to an external capacitor of 0.1 μF providing low pass filtering of the PIR input signal, blocking input signals at and above the switching frequency of the switched capacitor bandpass filter.

5. **DC CAP:** This pin connects to an external capacitor of 10 µF and holds the average pyro source voltage. The difference between this average and the actual pyro source voltage is amplified and coupled to the switched capacitor bandpass filter. The 10 µF capacitor must be a low leakage capacitor, such as a Tantalum capacitor.

6. **VReg:** This pin outputs a voltage that can be used directly drive an external NPN/PNP volatage regulator, or the gate of an external depletion mode JFET voltage regulator pass element. This pin need not be connected if an external voltage regulator, such as a three pin regulator, is used to generate Vcc for the chip.

7. **Pyro (D):** The pyro drain reference voltage is output on this pin. This voltage is power supply independent and is connected internally to special noise cancellation circuitry to improve the performance and reliability of the PIR interface. Externally, this pin is connected to the pyro drain and to a 0.1 µF capacitor. This voltage can also be divided down by an external pot to supply the Sensitivity Adjust voltage to pin 2.

8. **Pyro (S):** This is the pyro source input pin that receives the PIR input signal. It is connected externally to the pyro source, a 200 pF capacitor and a 47 KΩ resistor to Gnd. This is a **sensitive** node and the length of the external interconnect to this pin should be made as short as possible. There should be a ground plane on the PC board under the PIR sensor.

9. **Gnd (A):** This pin is the electrical ground for the internal analog circuitry of the chip.

10. **Gnd (D) :** This pin is the electrical ground for the internal digital circuitry of the chip.

11. **Daylight Adjust:** This pin is the output of the Daylight Sense amplifier and the input to the daylight comparator. When using a silicon photo diode daylight sensor, this pin is connected to Daylight Sense (pin 12) by a resistor or pot. The amount of resistance determines the gain of the Daylight Sense amplifier and hence the sensitivity of the daylight detector. When using a CdS daylight sensor, a pot is connected between this pin and Vcc, while the CdS sensor is connected across one side of the pot (two fixed resistors can be used instead of the pot). Daylight Sense (pin 12) must be connected to Vcc when using a CdS sensor. To disable the daylight detector, Daylight Adjust (pin 11) must be unconnected and Daylight Sense (pin 12) must be connected to Vcc. To disable Auto-ON mode, Daylight Adjust (pin 11) and Daylight Sense (pin 12) must both be connected to Vcc (the daylight detector is not used when Auto-ON mode is disabled).

12. **Daylight Sense:** This pin is the input to the Daylight Sense amplifier. When using a silicon photo diode daylight sensor, this pin is connected to the cathode of the silicon photo diode and to a feedback resistor (or pot) from Daylight Adjust (pin 11). In all other cases, this pin is connected to Vcc.

13. **Gain Select:** The Gain Select pin is a tri-state input used to select the gain of the PIR circuitry. When this pin is connected to Gnd, the PIR gain is set to 62 db. When this pin is unconnected or connected to Vcc, the PIR gain is set to 68 db. Normally this pin is unconnected except when less gain is required by a particular PIR sensor.

14. **ON/AUTO/OFF:** This pin is a tri-state input used to determine the operation of the chip. Normally this pin is unconnected, allowing the chip to operate in its configured operating mode. If this pin is connected to Gnd, the load will turn off unconditionally and will remain off as long as this pin is connected to Gnd. If this pin is connected to Vcc, the load will turn on unconditionally and will remain on as long as this pin is connected to Vcc.

15. **Toggle:** This pin is a toggle input used to determine the operation of the chip. Normally this pin is unconnected, allowing the chip to operate in its configured operating mode. If this pin is connected to Gnd, the load will change from on to off or from off to on and will remain in the new state unconditionally as long as this pin is connected to Gnd. If the ON/AUTO/OFF (pin 14) and Toggle (pin 15) switches are pressed such that one is trying to turn the load on unconditionally and the other is trying to turn the load off unconditionally, the load will be turned off (off overrides on).

16. **OUT :** The output from this pin is used to turn the external load on or off through a TRIAC, relay or opto-coupler. The impedance of this pin is less than 35 Ω, enabling it to directly drive a small (100 Ω DC coil resistance) pulse relay through a 150 µF series capacitor. For proper operation, the load should come on when this pin goes high, the load should go off when this pin goes low.

17. **LED:** The output from the motion comparator drives this pin through an internal 500 Ω current limiting resistor, enabling it to directly drive an LED motion indicator. Whenever motion is detected this pin will go high and the LED will light. When there is no motion this pin will be low.

18. **C:** This pin is the input to the OFF timer oscillator. It is connected externally to a pot (or resistor) from R (pin 19) and to a capacitor. The OFF timer delay, in seconds, will be 5678 x (40,000 + pot resistance in Ohms) x (capacitance in Farads). To disable Auto-OFF mode, this pin can be connected to Gnd or Vcc. For minimum time delay, C(pin 18) and R(pin 19) can be shorted together with no external resistor or capacitor. In this configuration, the output at OUT(pin 16) should be the same as the output at LED(pin 17).

19. **R :** The output of the OFF timer oscillator drives this pin through an internal 40 KΩ series resistor. This pin is connected externally to C (pin 18) through a pot (or resistor). This pin can be connected directly to C (pin 18) for the minimum OFF timer delay (maximum oscillator frequency).

20. **FRef :** This is the 160 Hz reference oscillator input. It is connected externally through a 330KΩ resistor to Vcc and a 0.022µF capacitor to Gnd. Other values of resistance and capacitance can be chosen, provided this input oscillates at 160Hz. This frequency is used to drive the internal switched capacitor bandpass filter and the timing delays.

Electrical Specifications

Below are the specifications at room temperature (25 °C).

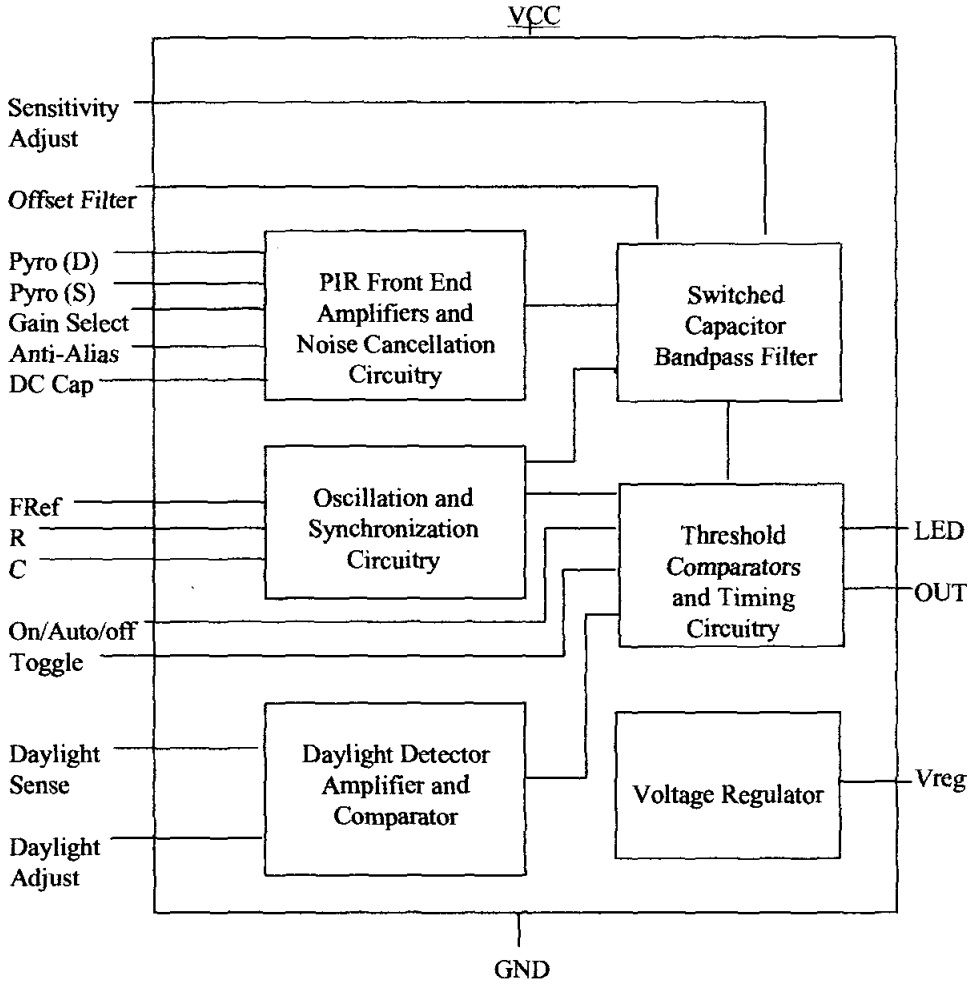
Parameter	Min.	Typ.	Max.	Unit
Vcc	4	5	15	V
Icc		300		µA
Input Voltage on any Pins	Gnd - 0.5		Vcc + 0.5	V
PIR Power Supply Rejection Ratio	74			dB
PIR Input Gain	62		68	dB
Overall gain variation			5	%
Overall threshold variation			7	%
Daylight Adjust (pin 11) Pull-down Current		5		µA
Gain Select (pin 13) Pull-up Current		5		µA
ON/AUTO/OFF (pin 14) Pull-up Current		10		µA
ON/AUTO/OFF (pin 14) Pull-Down Current		10		µA
Toggle (pin 15) Pull-up Current		5		µA
Pyro (D) (pin 7) Reference Voltage	2.3	2.5	2.7	V
OUT (pin 16) Output Impedance			35	Ω
LED (pin 17) Output Impedance	375	500	625	Ω
R (pin 19) Output Impedance	30	40	50	KΩ
Operating Temperature	-25		+100	°C
Storage Temperature	-55		+125	°C

Application Notes:

1. Normally, Gain Select (pin 13) is unconnected, providing a PIR gain of 68 db. For reduced sensitivity, Gain Select is connected to Gnd, providing a gain of 62 db.
2. Auto-ON mode can be disabled by connecting both Daylight Sense (pin 12) and Daylight Adjust (pin 11) to Vcc.
3. Auto-OFF mode can be disabled by connecting C (pin 18) to Gnd or Vcc.
4. Daylight detector can be disabled by connecting Daylight Sense (pin 12) to Vcc.
5. With a 5 MΩ Daylight adjust pot, the daylight sensitivity can be adjusted from complete darkness (always on) to complete daylight (always off). Additional fixed resistors and possibly a smaller pot can be used to restrict the range for specific applications.
6. The OFF timer range can be set by selecting a pot and capacitor and possibly additional fixed resistors that will produce the minimum and maximum time delays at the extremes of the pot.

7. OFF timer delay = 5678 x (R+40,000) x C seconds, R is in Ohms, C is in Farads.
8. The Sensitivity Adjust pot is used to select a voltage between the pyro drain reference voltage (minimum sensitivity) and Gnd (maximum sensitivity). The value of the pot is not critical and any value between 100 KΩ and 5 MΩ can be used.
9. The output of the switched capacitor bandpass filter can be seen on pin 3 (Offset Filter) when the external capacitor(10μF) is disconnected. The filter response can be measured in this way. (Disconnecting the external capacitor prevents motion from being detected.)
10. Pin 8 (Pyro (S)) is a **sensitive** node and the external interconnect to this pin should be made as short as possible. This node should also be closely surrounded by a ground plane.

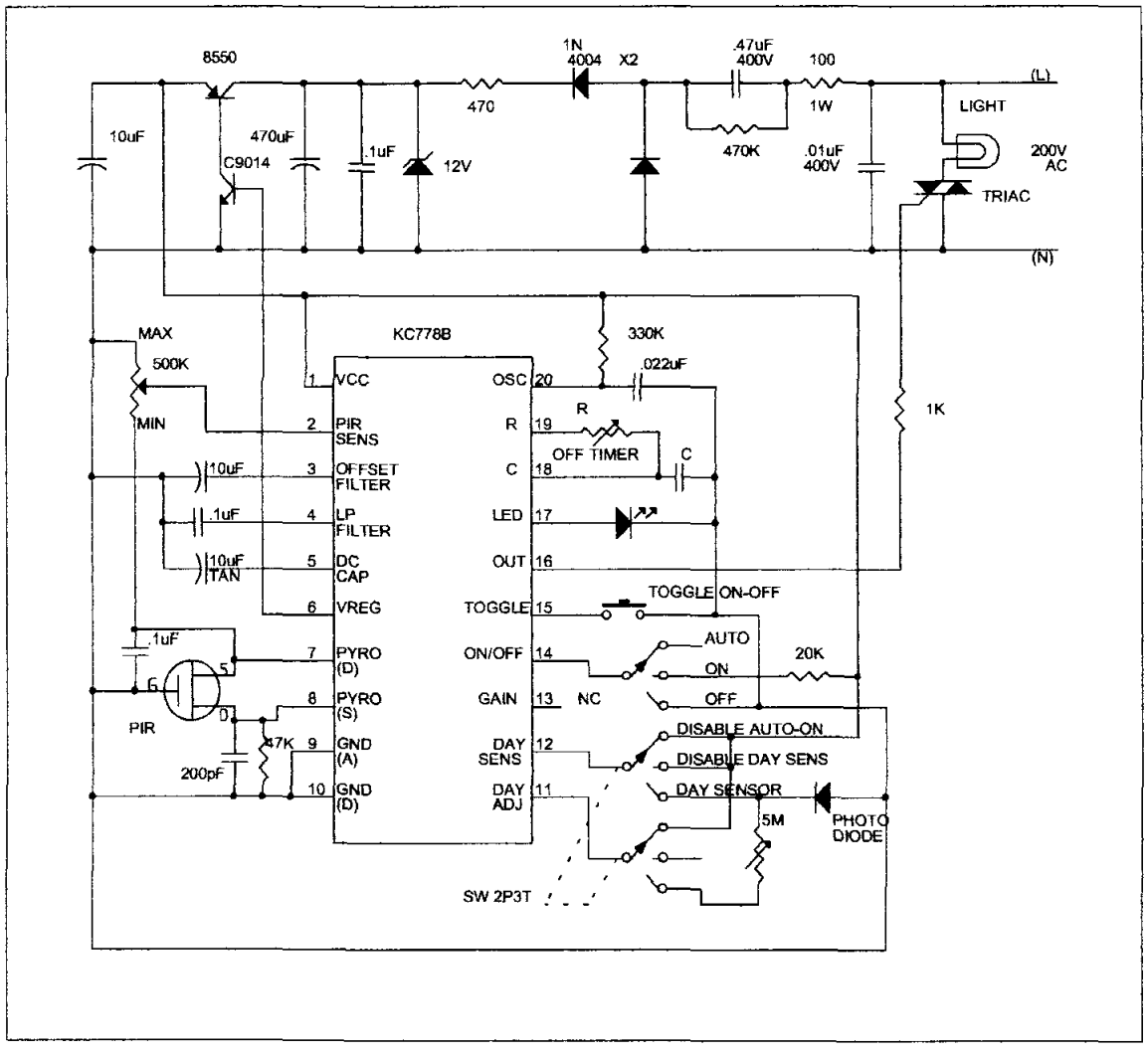
Block Diagram



Application Circuit

1. Typical Hook-up

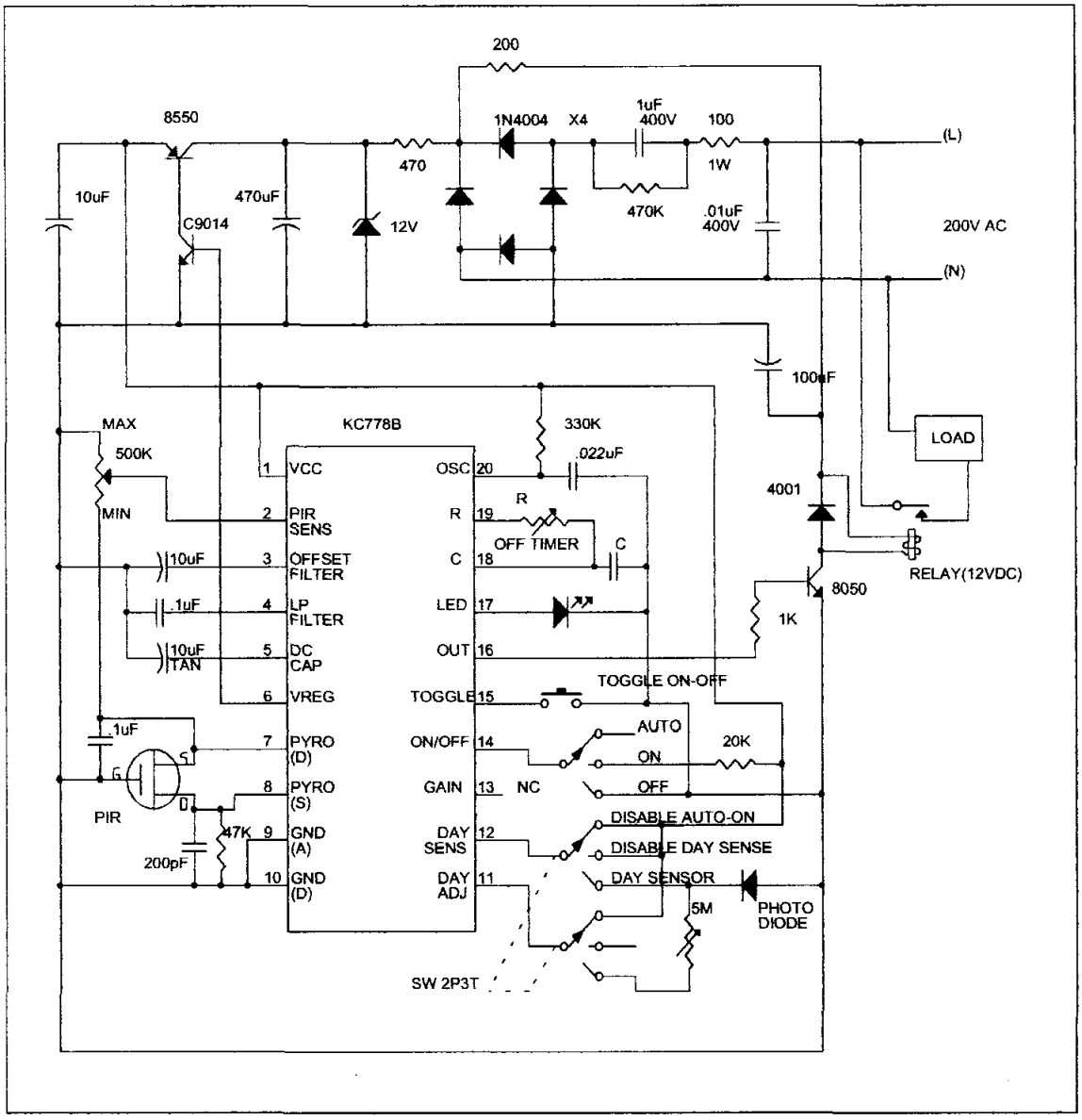
Below is a typical hook up for connecting KC778B to a PIR sensor, a TRIAC light switch and a silicon photodiode daylight detector. VReg is used for voltage regulation. 2 slide switches are used. One for select ON/AUTO/OFF and the other one used for enable, disable the daylight sensor and disable auto-on function. A simple AC regulation circuit is used in this system such that only a small gate current TRIAC can be used.



Note : Off Time Delay = 5678 x (R+40,000) x C Second
R in Ohm, C in Farad

2. Hook-up with with relay

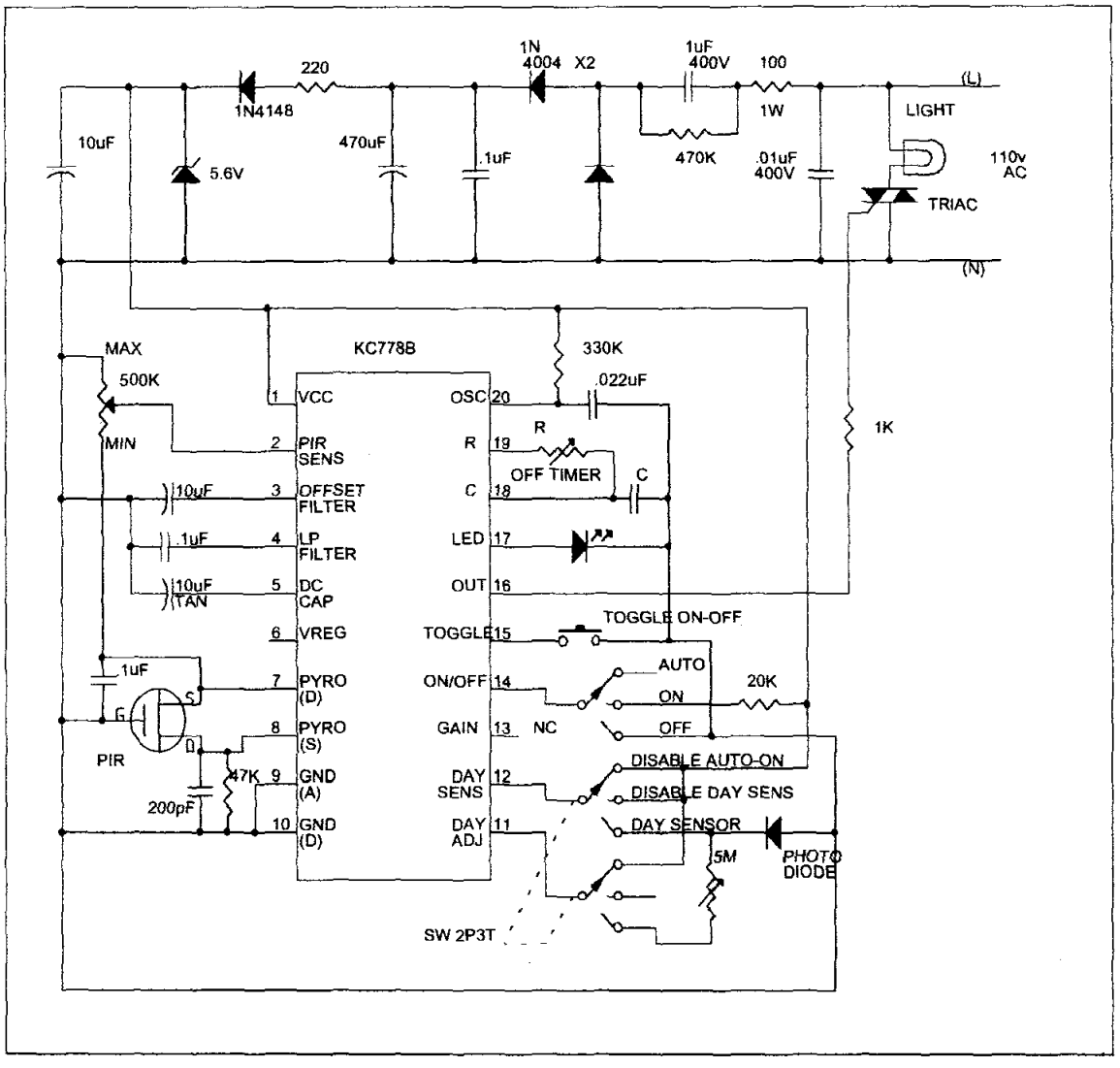
The following is similar to the typical hook-up. Due to the higher current require by relay, the bridge regulation method is used in AC circuit. This application is suitable to a high current loading such as heater, flood light, motor and etc.



Note : Off Time Delay = 5678 x (R+40,000) x C Second
R in Ohm, C in Farad

3. Hook-up with minimun regulator

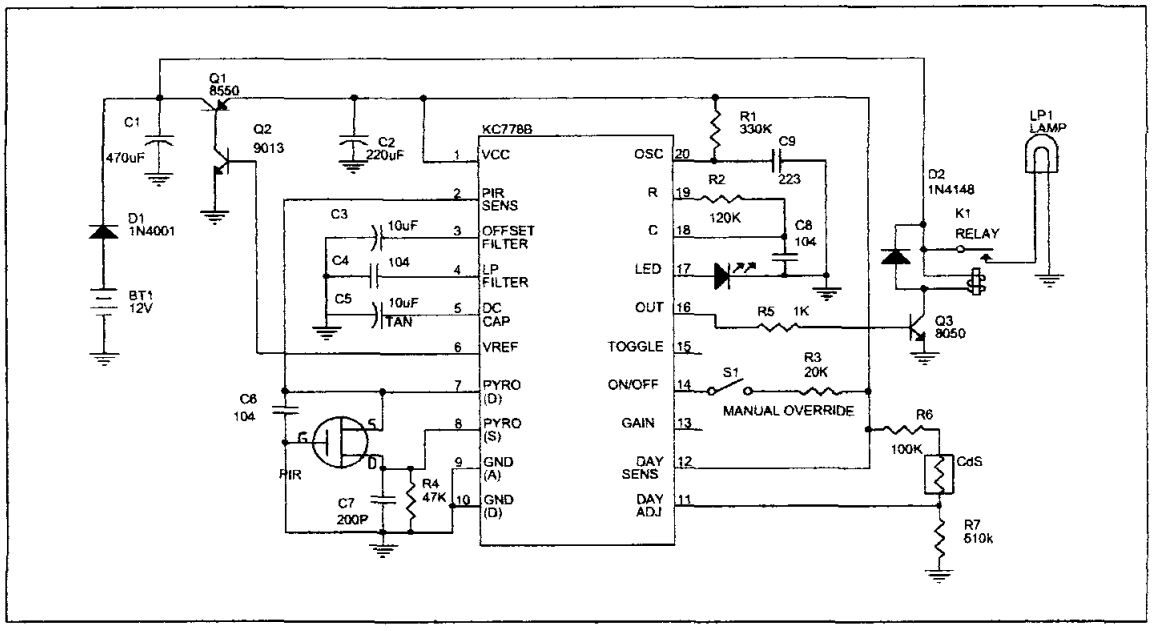
Below is an example of 110V application. Only one stages of regulator is used in the system by use of zener diode



Note : Off Time Delay = 5678 x (R+40,000) x C Second
R in Ohm, C in Farad

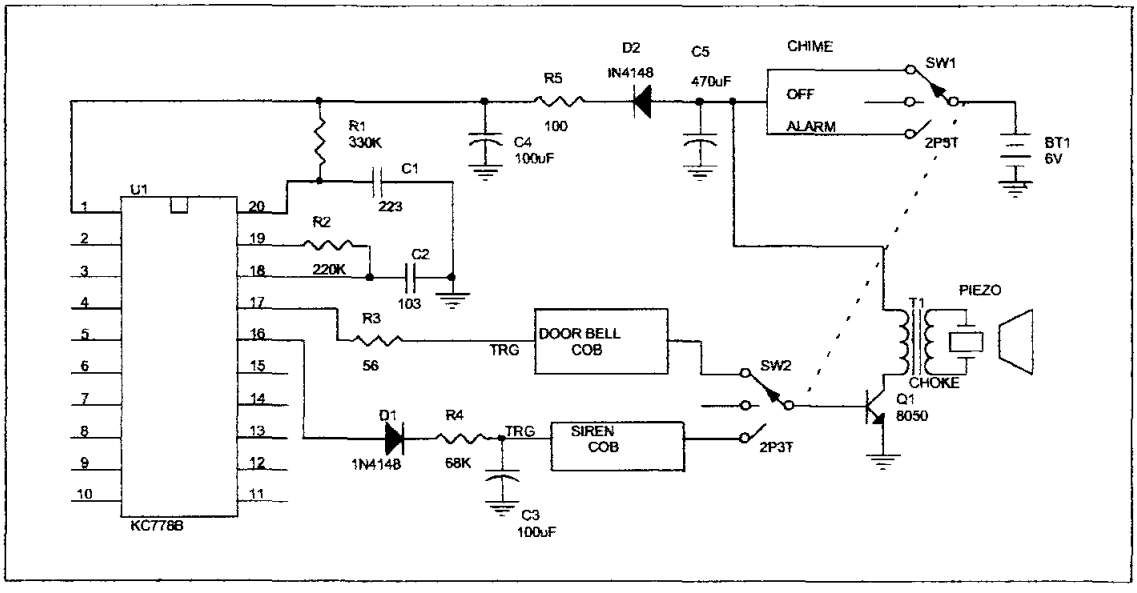
4. Hook-up with 12VDC system

Below is an example of Auto camp light which uses an auto battery (12VDC). Internal voltage regulator is used, it needs 12V to start up but can work down to 7V.



5. Hook-up with Door Chime and Alarm circuit

A 2P3T slide switch is used in the system.When it is positioned at Chime, the LED output of KC778B will trigger the door bell COB at anytime. If the switch is positioned at OFF, power will be cut off. When switch to Alarm position, after 25sec delay, the KC778B start working. It outputs a high signal when motion is detected. This signal will charge up the cap such that the siren COB will be triggered after the charge up delay time. It forms a very simple alarm product.



Features

- **Compatible with MCS-51™ Products**
- **4K Bytes of In-System Reprogrammable Flash Memory**
  - **Endurance: 1,000 Write/Erase Cycles**
- **Fully Static Operation: 0 Hz to 24 MHz**
- **Three-Level Program Memory Lock**
- ***128 x 8-Bit Internal RAM***
- **32 Programmable I/O Lines**
- **Two 16-Bit Timer/Counters**
- **Six Interrupt Sources**
- **Programmable Serial Channel**
- **Low Power Idle and Power Down Modes**

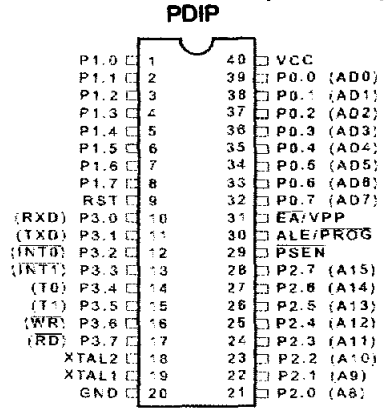
Description

The AT89C51 is a low-power, high-performance CMOS 8-bit microcomputer with 4K bytes of Flash Programmable and Erasable Read Only Memory (PEROM). The device is manufactured using Atmel's high density nonvolatile memory technology and is compatible with the industry standard MCS-51™ instruction set and pinout. The on-chip Flash allows the program memory to be reprogrammed in-system or by a conventional nonvolatile memory programmer. By combining a versatile 8-bit CPU with Flash on a monolithic chip, the Atmel AT89C51 is a powerful microcomputer which provides a highly flexible and cost effective solution to many embedded control applications.

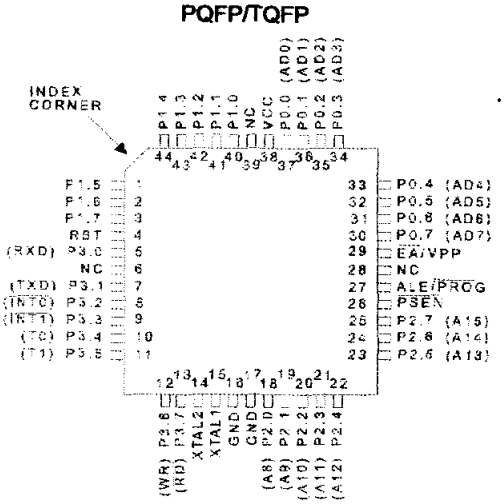
(continued)

Pin Configurations

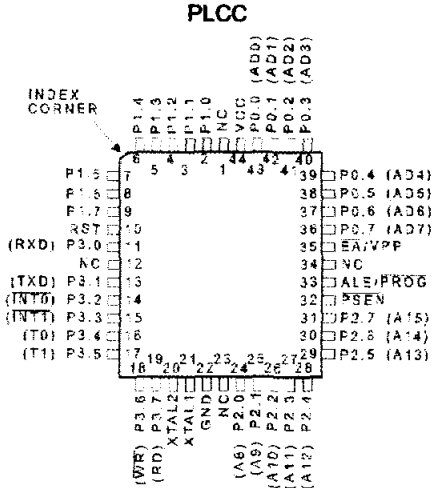
PDIP



PQFP/TQFP



PLCC

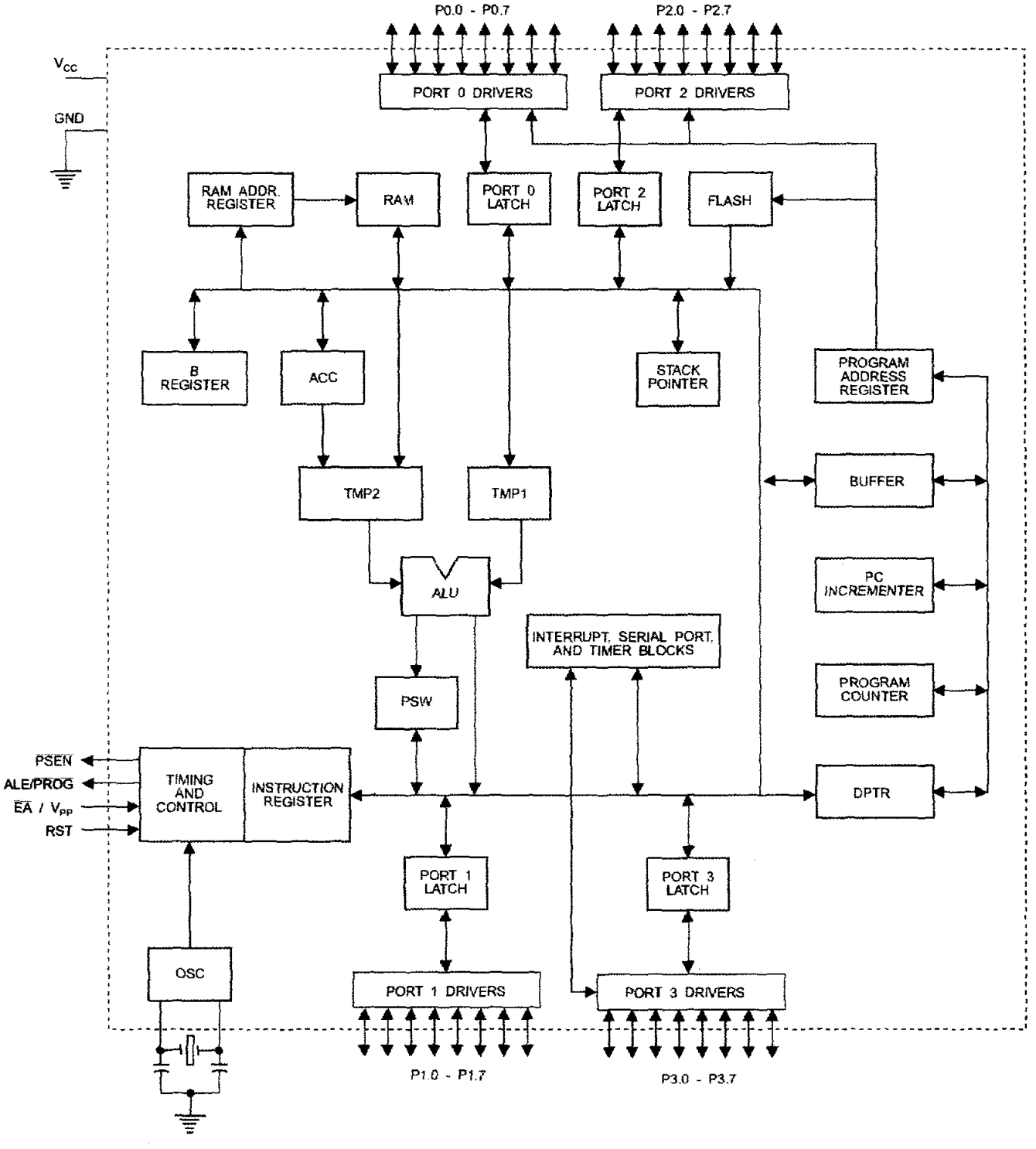


8-Bit Microcontroller with 4K Bytes Flash

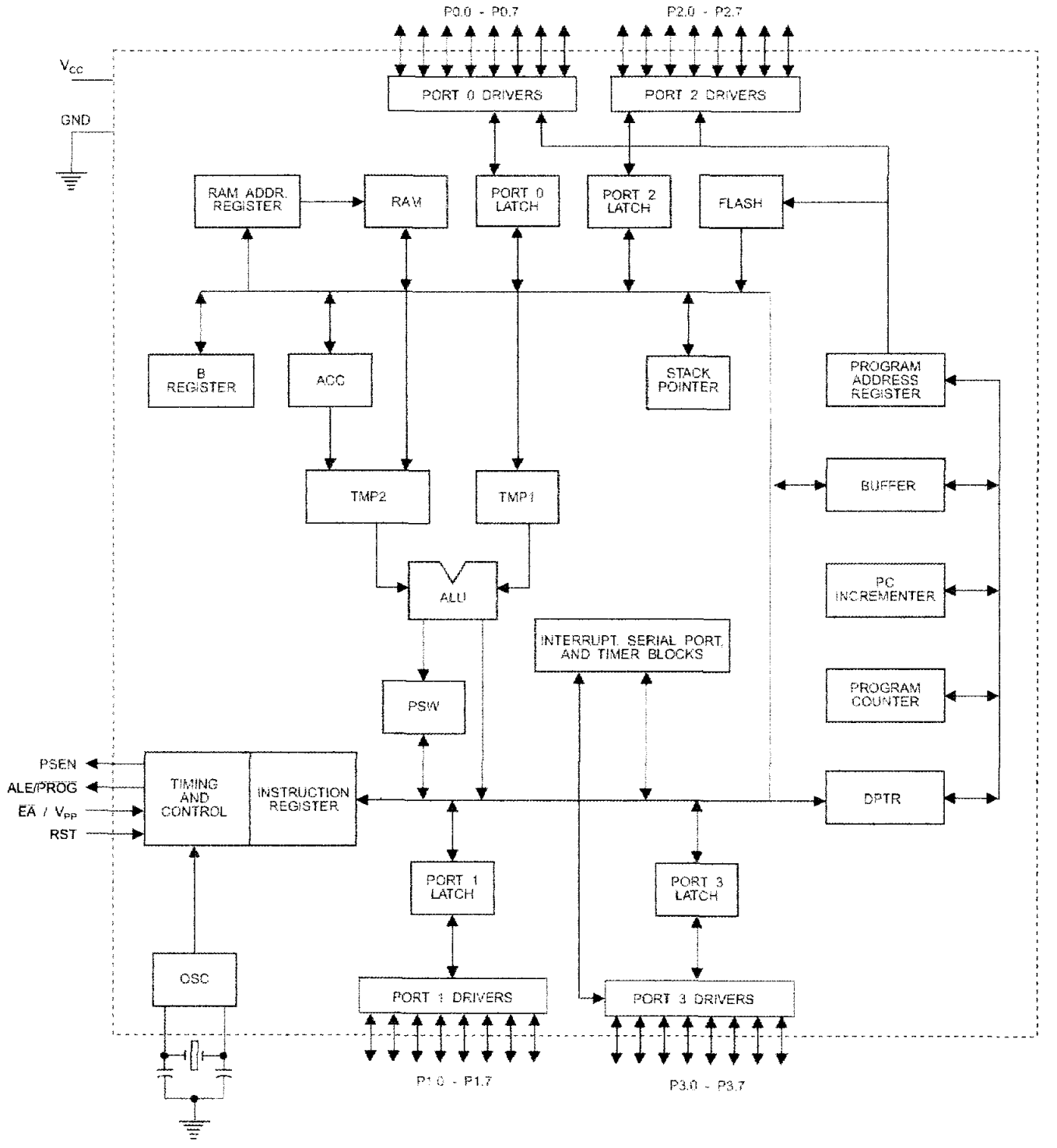
AT89C51

0265F-A–12/97

Block Diagram



Block Diagram



The AT89C51 provides the following standard features: 4K bytes of Flash, 128 bytes of RAM, 32 I/O lines, two 16-bit timer/counters, a five vector two-level interrupt architecture, a full duplex serial port, on-chip oscillator and clock circuitry. In addition, the AT89C51 is designed with static logic for operation down to zero frequency and supports two software selectable power saving modes. The Idle Mode stops the CPU while allowing the RAM, timer/counters, serial port and interrupt system to continue functioning. The Power Down Mode saves the RAM contents but freezes the oscillator disabling all other chip functions until the next hardware reset.

Pin Description

V_{CC}
Supply voltage.

GND
Ground.

Port 0
Port 0 is an 8-bit open drain bidirectional I/O port. As an output port each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high-impedance inputs.

Port 0 may also be configured to be the multiplexed low-order address/data bus during accesses to external program and data memory. In this mode P0 has internal pullups.

Port 0 also receives the code bytes during Flash programming, and outputs the code bytes during program verification. External pullups are required during program verification.

Port 1
Port 1 is an 8-bit bidirectional I/O port with internal pullups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}) because of the internal pullups.

Port 1 also receives the low-order address bytes during Flash programming and verification.

Port 2
Port 2 is an 8-bit bidirectional I/O port with internal pullups. The Port 2 output buffers can sink/source four TTL inputs. When 1s are written to Port 2 pins they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL}) because of the internal pullups.

Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application it uses strong internal pullups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

Port 3
Port 3 is an 8-bit bidirectional I/O port with internal pullups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}) because of the pullups.

Port 3 also serves the functions of various special features of the AT89C51 as listed below:

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

Port 3 also receives some control signals for Flash programming and verification.

RST
Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device.

ALE/$\overline{PROG}$
Address Latch Enable output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input ($\overline{PROG}$) during Flash programming.

In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external Data Memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

$\overline{PSEN}$
Program Store Enable is the read strobe to external program memory.

When the AT89C51 is executing code from external program memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external data memory.

$\overline{EA}$/V_{PP}

External Access Enable. $\overline{EA}$ must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed, $\overline{EA}$ will be internally latched on reset.

$\overline{EA}$ should be strapped to V_{CC} for internal program executions.

This pin also receives the 12-volt programming enable voltage (V_{PP}) during Flash programming, for parts that require 12-volt V_{PP}.

XTAL1

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

XTAL2

Output from the inverting oscillator amplifier.

Oscillator Characteristics

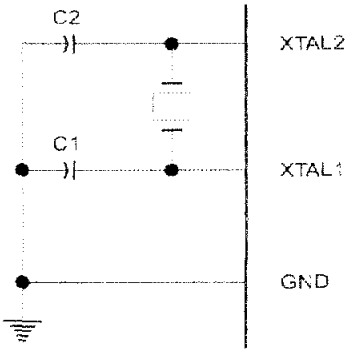
XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier which can be configured for use as an on-chip oscillator, as shown in Figure 1. Either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven as shown in Figure 2. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

Idle Mode

In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special functions registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

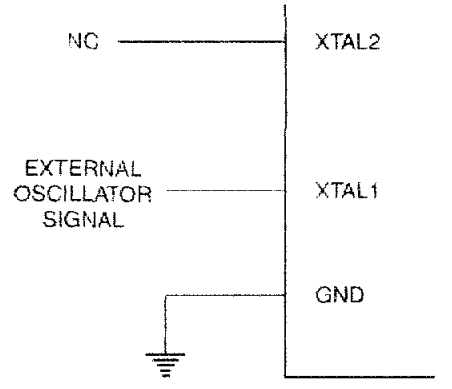
It should be noted that when idle is terminated by a hard ware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.

Figure 1. Oscillator Connections



Note: C1, C2 = 30 pF ± 10 pF for Crystals
= 40 pF ± 10 pF for Ceramic Resonators

Figure 2. External Clock Drive Configuration



Status of External Pins During Idle and Power Down Modes

Mode	Program Memory	ALE	$\overline{PSEN}$	PORT0	PORT1	PORT2	PORT3
Idle	Internal	1	1	Data	Data	Data	Data
Idle	External	1	1	Float	Data	Address	Data
Power Down	Internal	0	0	Data	Data	Data	Data
Power Down	External	0	0	Float	Data	Data	Data

Power Down Mode

In the power down mode the oscillator is stopped, and the instruction that invokes power down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the power down mode is terminated. The only exit from power down is a hardware reset. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

Program Memory Lock Bits

On the chip are three lock bits which can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in the table below:

When lock bit 1 is programmed, the logic level at the $\overline{EA}$ pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value, and holds that value until reset is activated. It is necessary that the latched value of $\overline{EA}$ be in agreement with the current logic level at that pin in order for the device to function properly.

Lock Bit Protection Modes

Program Lock Bits				Protection Type
	LB1	LB2	LB3	
1	U	U	U	No program lock features.
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, $\overline{EA}$ is sampled and latched on reset, and further programming of the Flash is disabled.
3	P	P	U	Same as mode 2, also verify is disabled.
4	P	P	P	Same as mode 3, also external execution is disabled.

Programming the Flash

The AT89C51 is normally shipped with the on-chip Flash memory array in the erased state (that is, contents = FFH) and ready to be programmed. The programming interface accepts either a high-voltage (12-volt) or a low-voltage (V_{CC}) program enable signal. The low voltage programming mode provides a convenient way to program the AT89C51 inside the user's system, while the high-voltage programming mode is compatible with conventional third party Flash or EPROM programmers.

The AT89C51 is shipped with either the high-voltage or low-voltage programming mode enabled. The respective top-side marking and device signature codes are listed in the following table.

	V_{PP} = 12V	V_{PP} = 5V
Top-Side Mark	AT89C51 xxxx yyww	AT89C51 xxxx-5 yyww
Signature	(030H)=1EH (031H)=51H (032H)=FFH	(030H)=1EH (031H)=51H (032H)=05H

The AT89C51 code memory array is programmed byte-by-byte in either programming mode. *To program any non-blank byte in the on-chip Flash Memory, the entire memory must be erased using the Chip Erase Mode.*

Programming Algorithm: Before programming the AT89C51, the address, data and control signals should be set up according to the Flash programming mode table and Figures 3 and 4. To program the AT89C51, take the following steps.

1. Input the desired memory location on the address lines.
2. Input the appropriate data byte on the data lines.
3. Activate the correct combination of control signals.
4. Raise $\overline{EA}/V_{PP}$ to 12V for the high-voltage programming mode.
5. Pulse ALE/$\overline{PROG}$ once to program a byte in the Flash array or the lock bits. The byte-write cycle is self-timed and typically takes no more than 1.5 ms. Repeat steps 1 through 5, changing the address and data for the entire array or until the end of the object file is reached.

Data Polling: The AT89C51 features Data Polling to indicate the end of a write cycle. During a write cycle, an attempted read of the last byte written will result in the complement of the written datum on PO.7. Once the write cycle has been completed, true data are valid on all outputs, and the next cycle may begin. Data Polling may begin any time after a write cycle has been initiated.

Ready/Busy: The progress of byte programming can also be monitored by the RDY/BSY output signal. P3.4 is pulled low after ALE goes high during programming to indicate BUSY. P3.4 is pulled high again when programming is done to indicate READY.

Program Verify: If lock bits LB1 and LB2 have not been programmed, the programmed code data can be read back via the address and data lines for verification. The lock bits cannot be verified directly. Verification of the lock bits is achieved by observing that their features are enabled.

Chip Erase: The entire Flash array is erased electrically by using the proper combination of control signals and by holding ALE/$\overline{PROG}$ low for 10 ms. The code array is written with all "1"s. The chip erase operation must be executed before the code memory can be re-programmed.

Reading the Signature Bytes: The signature bytes are read by the same procedure as a normal verification of locations 030H,

031H, and 032H, except that P3.6 and P3.7 must be pulled to a logic low. The values returned are as follows.

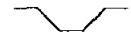
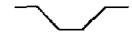
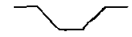
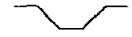
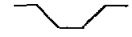
(030H) = 1EH indicates manufactured by Atmel
(031H) = 51H indicates 89C51
(032H) = FFH indicates 12V programming
(032H) = 05H indicates 5V programming

Programming Interface

Every code byte in the Flash array can be written and the entire array can be erased by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

All major programming vendors offer worldwide support for the Atmel microcontroller series. Please contact your local programming vendor for the appropriate software revision.

Flash Programming Modes

Mode		RST	$\overline{PSEN}$	ALE/$\overline{PROG}$	$\overline{EA}$/V_{PP}	P2.6	P2.7	P3.6	P3.7
Write Code Data		H	L		H/12V	L	H	H	H
Read Code Data		H	L	H	H	L	L	H	H
Write Lock	Bit - 1	H	L		H/12V	H	H	H	H
	Bit - 2	H	L		H/12V	H	H	L	L
	Bit - 3	H	L		H/12V	H	L	H	L
Chip Erase		H	L	 (1)	H/12V	H	L	L	L
Read Signature Byte		H	L	H	H	L	L	L	L

Note: 1. Chip Erase requires a 10-ms PROG pulse.

Figure 3. Programming the Flash

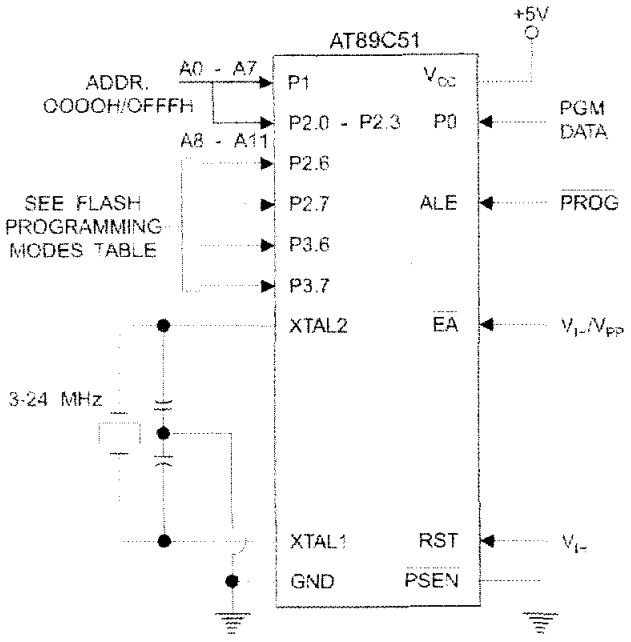
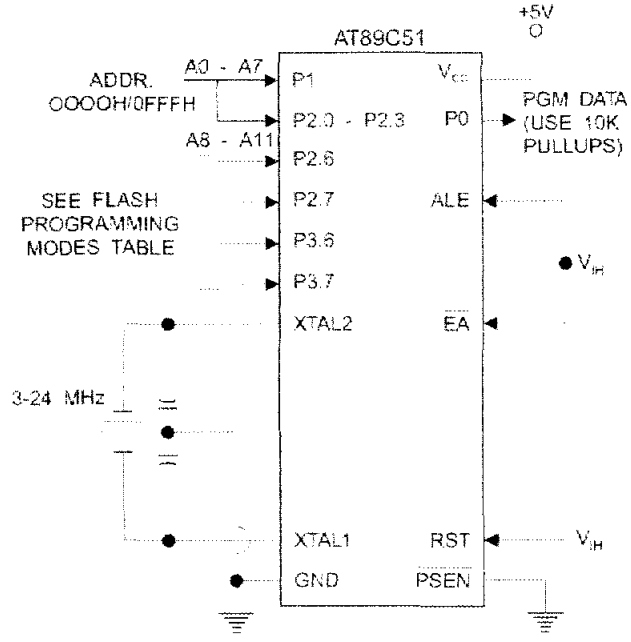


Figure 4. Verifying the Flash



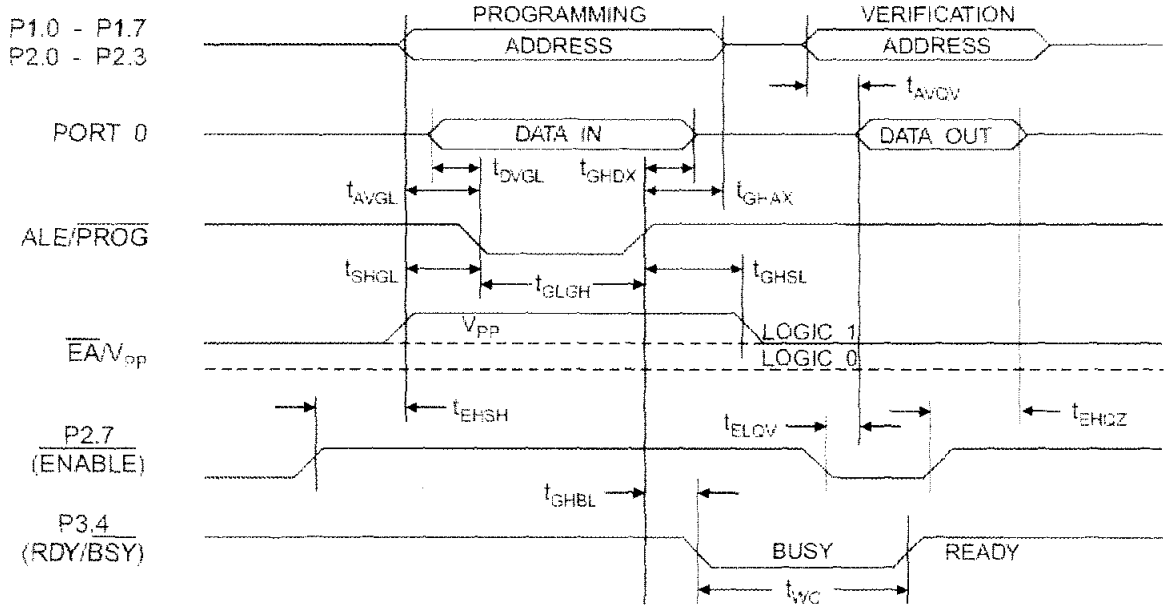
Flash Programming and Verification Characteristics

T_A = 0°C to 70°C, V_{CC} = 5.0 ± 10%

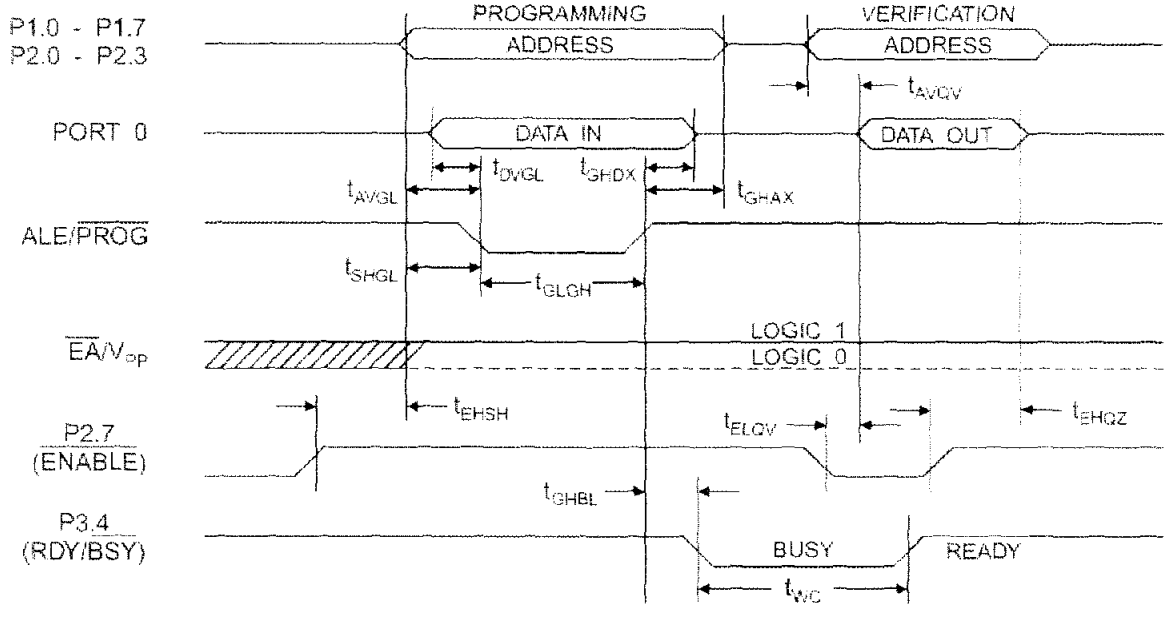
Symbol	Parameter	Min	Max	Units
V_{PP}(1)	Programming Enable Voltage	11.5	12.5	V
I_{PP}(1)	Programming Enable Current		1.0	mA
$1/t_{CLCL}$	Oscillator Frequency	3	24	MHz
t_{AVGL}	Address Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
t_{GHAX}	Address Hold After $\overline{PROG}$	$48t_{CLCL}$		
t_{DVGL}	Data Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
t_{GHDX}	Data Hold After $\overline{PROG}$	$48t_{CLCL}$		
t_{EHSH}	P2.7 ($\overline{ENABLE}$) High to V_{PP}	$48t_{CLCL}$		
t_{SHGL}	V_{PP} Setup to $\overline{PROG}$ Low	10		µs
t_{GHSL}(1)	V_{PP} Hold After $\overline{PROG}$	10		µs
t_{GLGH}	$\overline{PROG}$ Width	1	110	µs
t_{AVQV}	Address to Data Valid		$48t_{CLCL}$	
t_{ELQV}	$\overline{ENABLE}$ Low to Data Valid		$48t_{CLCL}$	
t_{EHQZ}	Data Float After $\overline{ENABLE}$	0	$48t_{CLCL}$	
t_{GHBL}	$\overline{PROG}$ High to $\overline{BUSY}$ Low		1.0	µs
t_{WC}	Byte Write Cycle Time		2.0	ms

Note: 1. Only used in 12-volt programming mode.

Flash Programming and Verification Waveforms - High Voltage Mode (V_{PP} = 12V)



Flash Programming and Verification Waveforms - Low Voltage Mode (V_{PP} = 5V)



Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0V to +7.0V
Maximum Operating Voltage	6.6V
DC Output Current	15.0 mA

*NOTICE: *Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

DC Characteristics

T_A = -40°C to 85°C, V_{CC} = 5.0V ± 20% *(unless otherwise noted)*

Symbol	Parameter	Condition	Min	Max	Units
V_{IL}	Input Low Voltage	(Except $\overline{EA}$)	-0.5	0.2 V_{CC} - 0.1	V
V_{IL1}	Input Low Voltage ($\overline{EA}$)		-0.5	0.2 V_{CC} - 0.3	V
V_{IH}	Input High Voltage	(Except XTAL1, RST)	0.2 V_{CC} + 0.9	V_{CC} + 0.5	V
V_{IH1}	Input High Voltage	(XTAL1, RST)	0.7 V_{CC}	V_{CC} + 0.5	V
V_{OL}	Output Low Voltage[1] (Ports 1,2,3)	I_{OL} = 1.6 mA		0.45	V
V_{OL1}	Output Low Voltage[1] (Port 0, ALE, $\overline{PSEN}$)	I_{OL} = 3.2 mA		0.45	V
V_{OH}	Output High Voltage (Ports 1,2,3, ALE, $\overline{PSEN}$)	I_{OH} = -60 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -25 µA	0.75 V_{CC}		V
		I_{OH} = -10 µA	0.9 V_{CC}		V
V_{OH1}	Output High Voltage (Port 0 in External Bus Mode)	I_{OH} = -800 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -300 µA	0.75 V_{CC}		V
		I_{OH} = -80 µA	0.9 V_{CC}		V
I_{IL}	Logical 0 Input Current (Ports 1,2,3)	V_{IN} = 0.45V		-50	µA
I_{TL}	Logical 1 to 0 Transition Current (Ports 1,2,3)	V_{IN} = 2V, VCC = 5V ± 10%		-650	µA
I_{LI}	Input Leakage Current (Port 0, $\overline{EA}$)	0.45 < V_{IN} < V_{CC}		±10	µA
RRST	Reset Pulldown Resistor		50	300	KΩ
C_{IO}	Pin Capacitance	Test Freq. = 1 MHz, T_A = 25°C		10	pF
I_{CC}	Power Supply Current	Active Mode, 12 MHz		20	mA
		Idle Mode, 12 MHz		5	mA
	Power Down Mode[2]	V_{CC} = 6V		100	µA
		V_{CC} = 3V		40	µA

Notes: 1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
Maximum I_{OL} per port pin: 10 mA
Maximum I_{OL} per 8-bit port: Port 0: 26 mA
Ports 1, 2, 3: 15 mA
Maximum total I_{OL} for all output pins: 71 mA
If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

2. Minimum V_{CC} for Power Down is 2V.

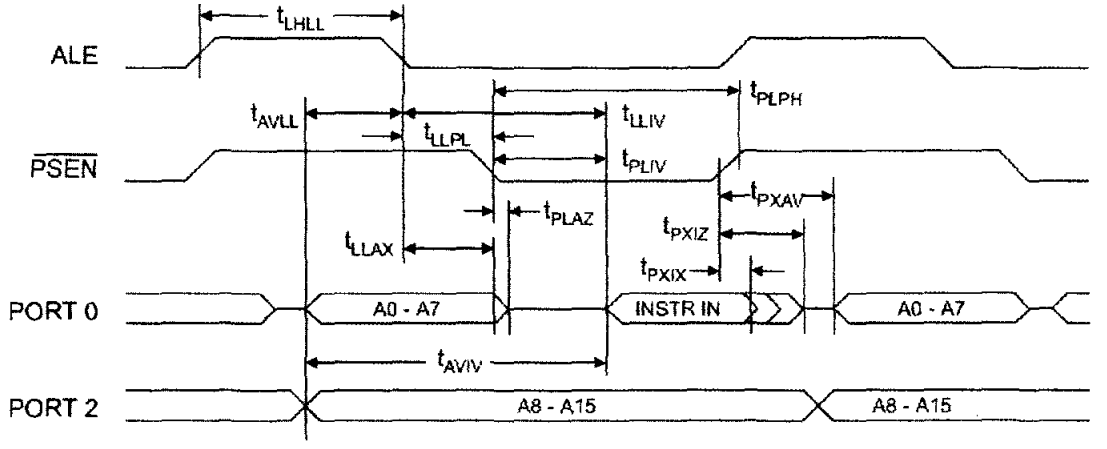
AC Characteristics

(Under Operating Conditions; Load Capacitance for Port 0, ALE/$\overline{PROG}$, and $\overline{PSEN}$ = 100 pF; Load Capacitance for all other outputs = 80 pF)

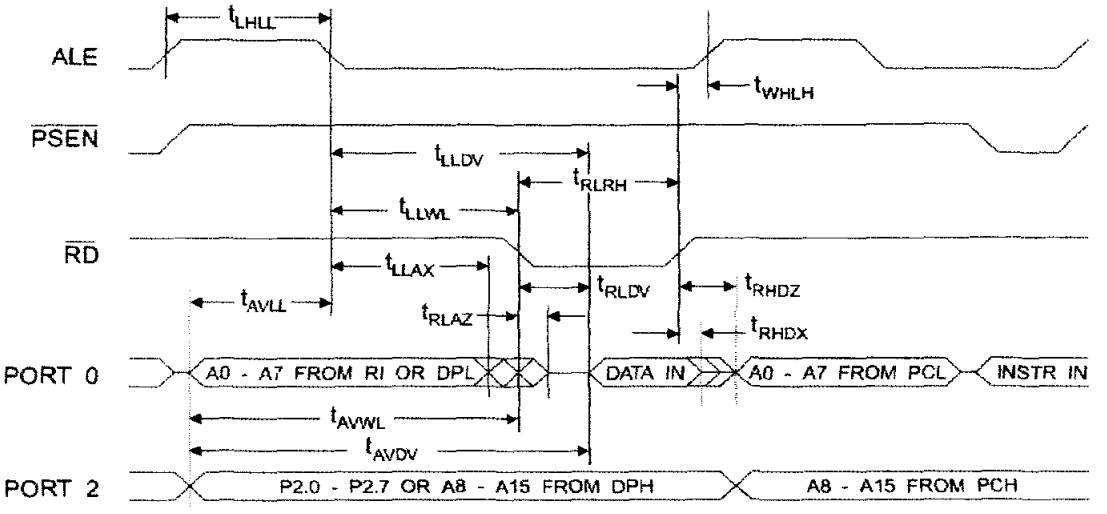
External Program and Data Memory Characteristics

Symbol	Parameter	12 MHz Oscillator		16 to 24 MHz Oscillator		Units
		Min	Max	Min	Max	
$1/t_{CLCL}$	Oscillator Frequency			0	24	MHz
t_{LHLL}	ALE Pulse Width	127		$2t_{CLCL}$-40		ns
t_{AVLL}	Address Valid to ALE Low	43		t_{CLCL}-13		ns
t_{LLAX}	Address Hold After ALE Low	48		t_{CLCL}-20		ns
t_{LLIV}	ALE Low to Valid Instruction In		233		$4t_{CLCL}$-65	ns
t_{LLPL}	ALE Low to $\overline{PSEN}$ Low	43		t_{CLCL}-13		ns
t_{PLPH}	$\overline{PSEN}$ Pulse Width	205		$3t_{CLCL}$-20		ns
t_{PLIV}	$\overline{PSEN}$ Low to Valid Instruction In		145		$3t_{CLCL}$-45	ns
t_{PXIX}	Input Instruction Hold After $\overline{PSEN}$	0		0		ns
t_{PXIZ}	Input Instruction Float After $\overline{PSEN}$		59		t_{CLCL}-10	ns
t_{PXAV}	$\overline{PSEN}$ to Address Valid	75		t_{CLCL}-8		ns
t_{AVIV}	Address to Valid Instruction In		312		$5t_{CLCL}$-55	ns
t_{PLAZ}	$\overline{PSEN}$ Low to Address Float		10		10	ns
t_{RLRH}	$\overline{RD}$ Pulse Width	400		$6t_{CLCL}$-100		ns
t_{WLWH}	$\overline{WR}$ Pulse Width	400		$6t_{CLCL}$-100		ns
t_{RLDV}	$\overline{RD}$ Low to Valid Data In		252		$5t_{CLCL}$-90	ns
t_{RHDX}	Data Hold After $\overline{RD}$	0		0		ns
t_{RHDZ}	Data Float After $\overline{RD}$		97		$2t_{CLCL}$-28	ns
t_{LLDV}	ALE Low to Valid Data In		517		$8t_{CLCL}$-150	ns
t_{AVDV}	Address to Valid Data In		585		$9t_{CLCL}$-165	ns
t_{LLWL}	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	200	300	$3t_{CLCL}$-50	$3t_{CLCL}$+50	ns
t_{AVWL}	Address to $\overline{RD}$ or $\overline{WR}$ Low	203		$4t_{CLCL}$-75		ns
t_{QVWX}	Data Valid to $\overline{WR}$ Transition	23		t_{CLCL}-20		ns
t_{QVWH}	Data Valid to $\overline{WR}$ High	433		$7t_{CLCL}$-120		ns
t_{WHQX}	Data Hold After $\overline{WR}$	33		t_{CLCL}-20		ns
t_{RLAZ}	$\overline{RD}$ Low to Address Float		0		0	ns
t_{WHLH}	$\overline{RD}$ or $\overline{WR}$ High to ALE High	43	123	t_{CLCL}-20	t_{CLCL}+25	ns

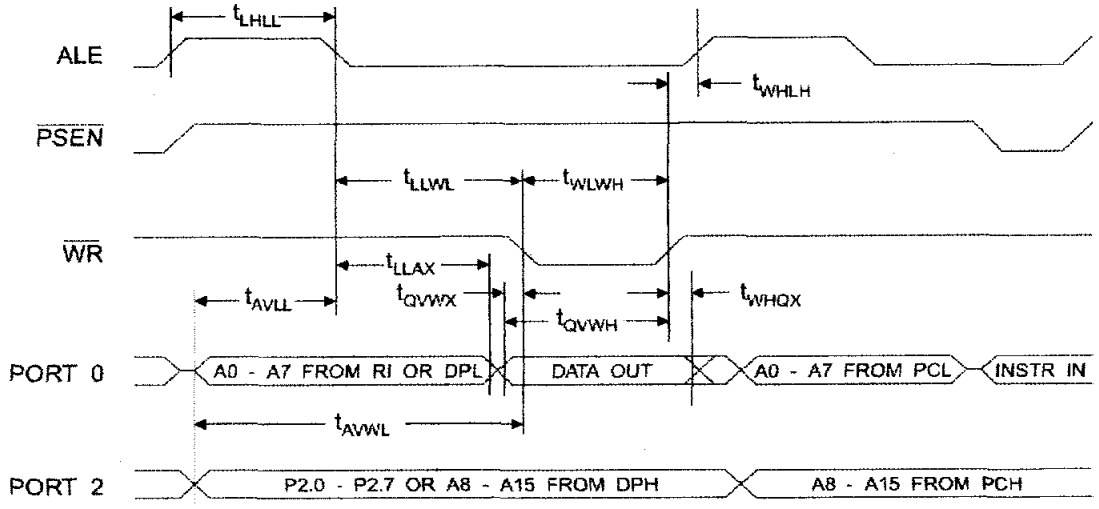
External Program Memory Read Cycle



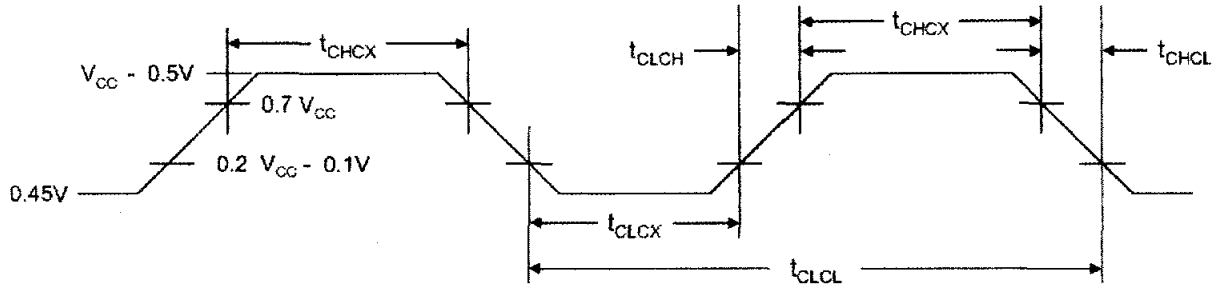
External Data Memory Read Cycle



External Data Memory Write Cycle



External Clock Drive Waveforms



External Clock Drive

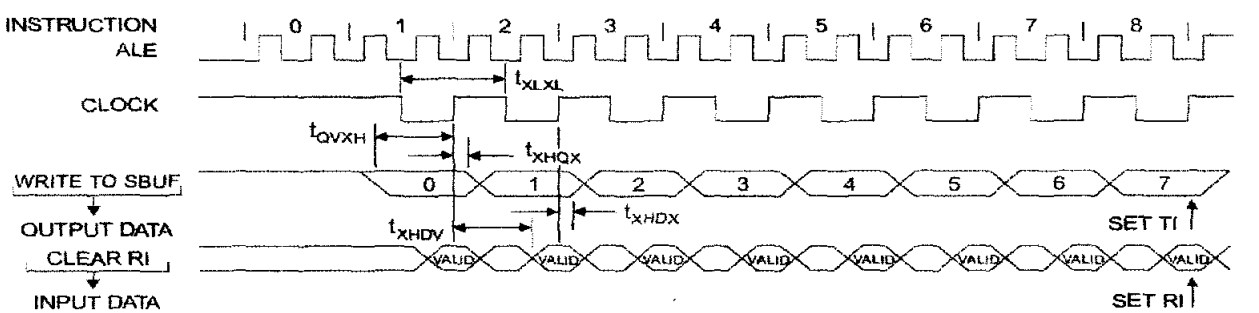
Symbol	Parameter	Min	Max	Units
$1/t_{CLCL}$	Oscillator Frequency	0	24	MHz
t_{CLCL}	Clock Period	41.6		ns
t_{CHCX}	High Time	15		ns
t_{CLCX}	Low Time	15		ns
t_{CLCH}	Rise Time		20	ns
t_{CHCL}	Fall Time		20	ns

Serial Port Timing: Shift Register Mode Test Conditions

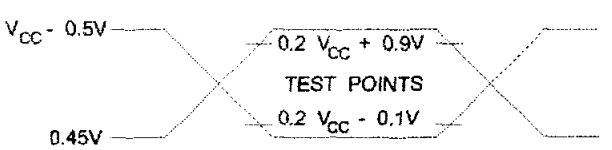
(V_{CC} = 5.0 V ± 20%; Load Capacitance = 80 pF)

Symbol	Parameter	12 MHz Osc		Variable Oscillator		Units
		Min	Max	Min	Max	
t_{XLXL}	Serial Port Clock Cycle Time	1.0		$12t_{CLCL}$		µs
t_{QVXH}	Output Data Setup to Clock Rising Edge	700		$10t_{CLCL}$-133		ns
t_{XHQX}	Output Data Hold After Clock Rising Edge	50		$2t_{CLCL}$-117		ns
t_{XHDX}	Input Data Hold After Clock Rising Edge	0		0		ns
t_{XHDV}	Clock Rising Edge to Input Data Valid		700		$10t_{CLCL}$-133	ns

Shift Register Mode Timing Waveforms

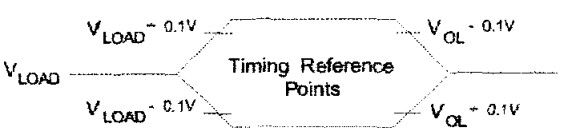


AC Testing Input/Output Waveforms[1]



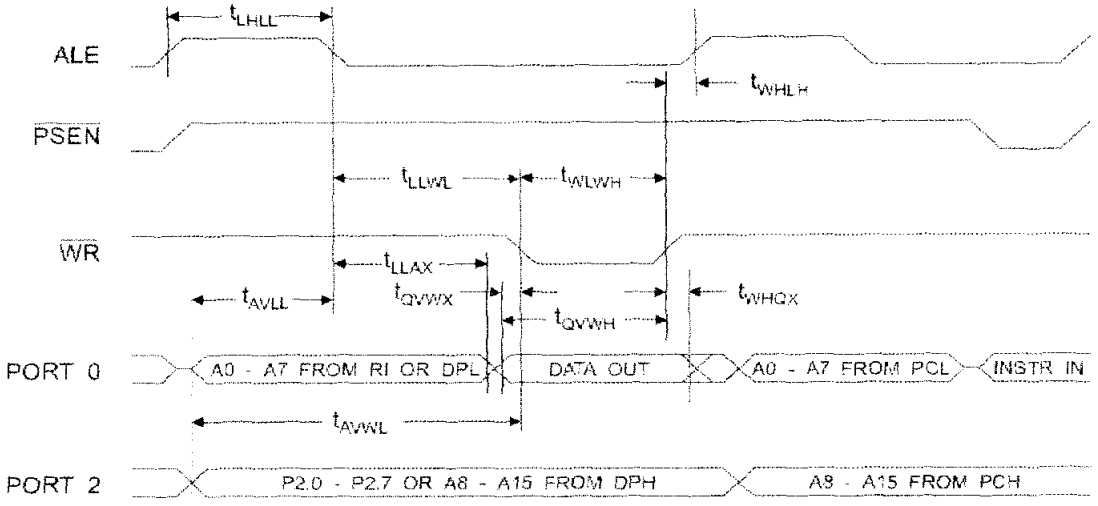
Note: 1. AC Inputs during testing are driven at V_{CC} - 0.5V for a logic 1 and 0.45V for a logic 0. Timing measurements are made at V_{IH} min. for a logic 1 and V_{IL} max. for a logic 0.

Float Waveforms[1]

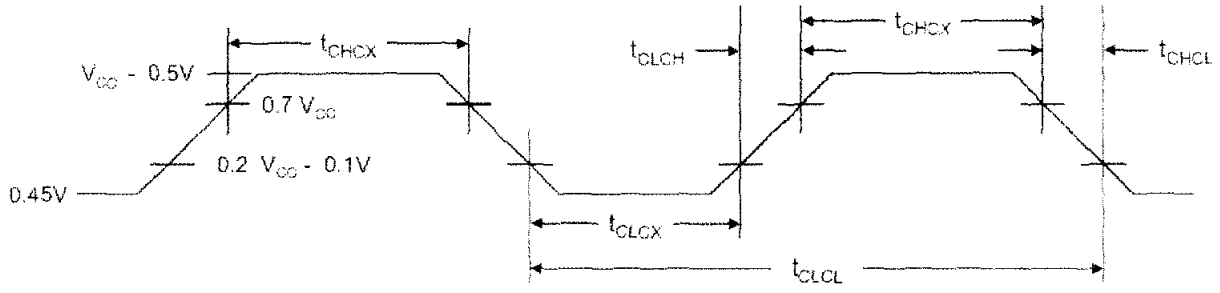


Note: 1. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when 100 mV change from the loaded V_{OH}/V_{OL} level occurs.

External Data Memory Write Cycle



External Clock Drive Waveforms



External Clock Drive

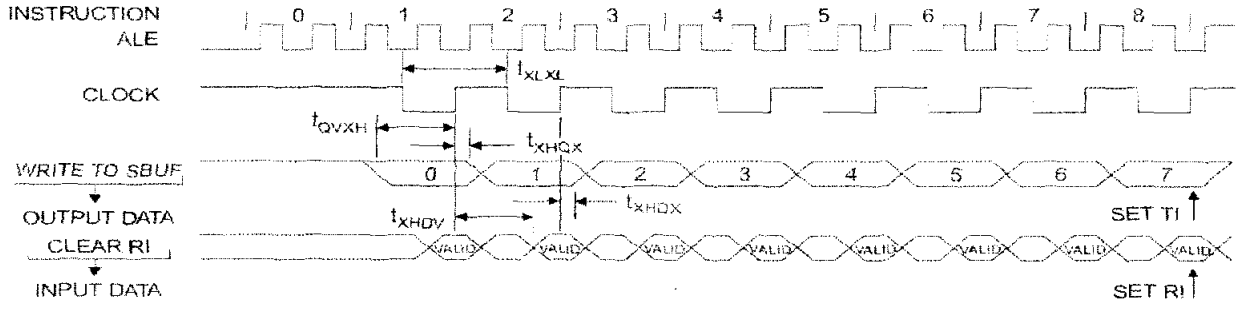
Symbol	Parameter	Min	Max	Units
$1/t_{CLCL}$	Oscillator Frequency	0	24	MHz
t_{CLCL}	Clock Period	41.6		ns
t_{CHCX}	High Time	15		ns
t_{CLCX}	Low Time	15		ns
t_{CLCH}	Rise Time		20	ns
t_{CHCL}	Fall Time		20	ns

Serial Port Timing: Shift Register Mode Test Conditions

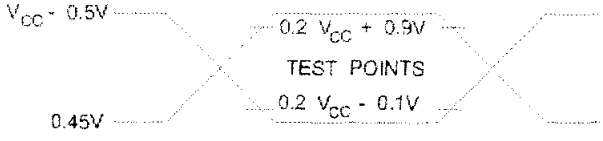
(V_{CC} = 5.0 V ± 20%; Load Capacitance = 80 pF)

Symbol	Parameter	12 MHz Osc		Variable Oscillator		Units
		Min	Max	Min	Max	
t_{XLXL}	Serial Port Clock Cycle Time	1.0		$12t_{CLCL}$		µs
t_{QVXH}	Output Data Setup to Clock Rising Edge	700		$10t_{CLCL}$-133		ns
t_{XHQX}	Output Data Hold After Clock Rising Edge	50		$2t_{CLCL}$-117		ns
t_{XHDX}	Input Data Hold After Clock Rising Edge	0		0		ns
t_{XHDV}	Clock Rising Edge to Input Data Valid		700		$10t_{CLCL}$-133	ns

Shift Register Mode Timing Waveforms

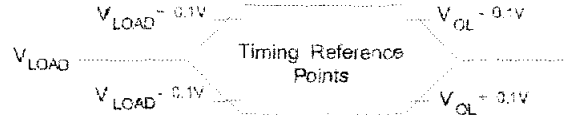


AC Testing Input/Output Waveforms[1]



Note: 1. AC Inputs during testing are driven at V_{CC} - 0.5V for a logic 1 and 0.45V for a logic 0. Timing measurements are made at V_{IH} min. for a logic 1 and V_{IL} max. for a logic 0.

Float Waveforms[1]



Note: 1. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when 100 mV change from the loaded V_{OH}/V_{OL} level occurs.

Ordering Information

Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
12	5V ± 20%	AT89C51-12AC	44A	Commercial
		AT89C51-12JC	44J	(0°C to 70°C)
		AT89C51-12PC	40P6	
		AT89C51-12QC	44Q	
		AT89C51-12AI	44A	Industrial
		AT89C51-12JI	44J	(-40°C to 85°C)
		AT89C51-12PI	40P6	
		AT89C51-12QI	44Q	
		AT89C51-12AA	44A	Automotive
		AT89C51-12JA	44J	(-40°C to 105°C)
		AT89C51-12PA	40P6	
		AT89C51-12QA	44Q	
16	5V ± 20%	AT89C51-16AC	44A	Commercial
		AT89C51-16JC	44J	(0°C to 70°C)
		AT89C51-16PC	40P6	
		AT89C51-16QC	44Q	
		AT89C51-16AI	44A	Industrial
		AT89C51-16JI	44J	(-40°C to 85°C)
		AT89C51-16PI	40P6	
		AT89C51-16QI	44Q	
		AT89C51-16AA	44A	Automotive
		AT89C51-16JA	44J	(-40°C to 105°C)
		AT89C51-16PA	40P6	
		AT89C51-16QA	44Q	
20	5V ± 20%	AT89C51-20AC	44A	Commercial
		AT89C51-20JC	44J	(0°C to 70°C)
		AT89C51-20PC	40P6	
		AT89C51-20QC	44Q	
		AT89C51-20AI	44A	Industrial
		AT89C51-20JI	44J	(-40°C to 85°C)
		AT89C51-20PI	40P6	
		AT89C51-20QI	44Q	

Ordering Information

Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
24	5V ± 20%	AT89C51-24AC	44A	Commercial
		AT89C51-24JC	44J	(0°C to 70°C)
		AT89C51-24PC	44P6	
		AT89C51-24QC	44Q	
		AT89C51-24AI	44A	Industrial
		AT89C51-24JI	44J	(-40°C to 85°C)
		AT89C51-24PI	44P6	
		AT89C51-24QI	44Q	

Package Type	
44A	44 Lead, Thin Plastic Gull Wing Quad Flatpack (TQFP)
44J	44 Lead, Plastic J-Leaded Chip Carrier (PLCC)
40P6	40 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
44Q	44 Lead, Plastic Gull Wing Quad Flatpack (PQFP)

BIODATA

Nama : **MULIANTO**

Nrp : 5103097009

Nirm : 97.7.003.31073.38695

TTL : Bojonegoro, 13 Agustus 1978

Agama : Katolik

Alamat : Dinoyo langgar 16

SURABAYA

Riwayat Pendidikan:

- SDN Banjarjo I Bojonegoro tahun 1985-1991.
- SMPN 1 Bojonegoro tahun 1991-1994.
- SMUK Ign. Slamet Riyadi Bojonegoro tahun 1994-1997
- Universitas Katolik Widya Mandala Surabaya Fakultas Teknik Jurusan Teknik Elektro tahun 1997. Pada bulan Januari 2002 mengikuti seminar dan ujian Skripsi.