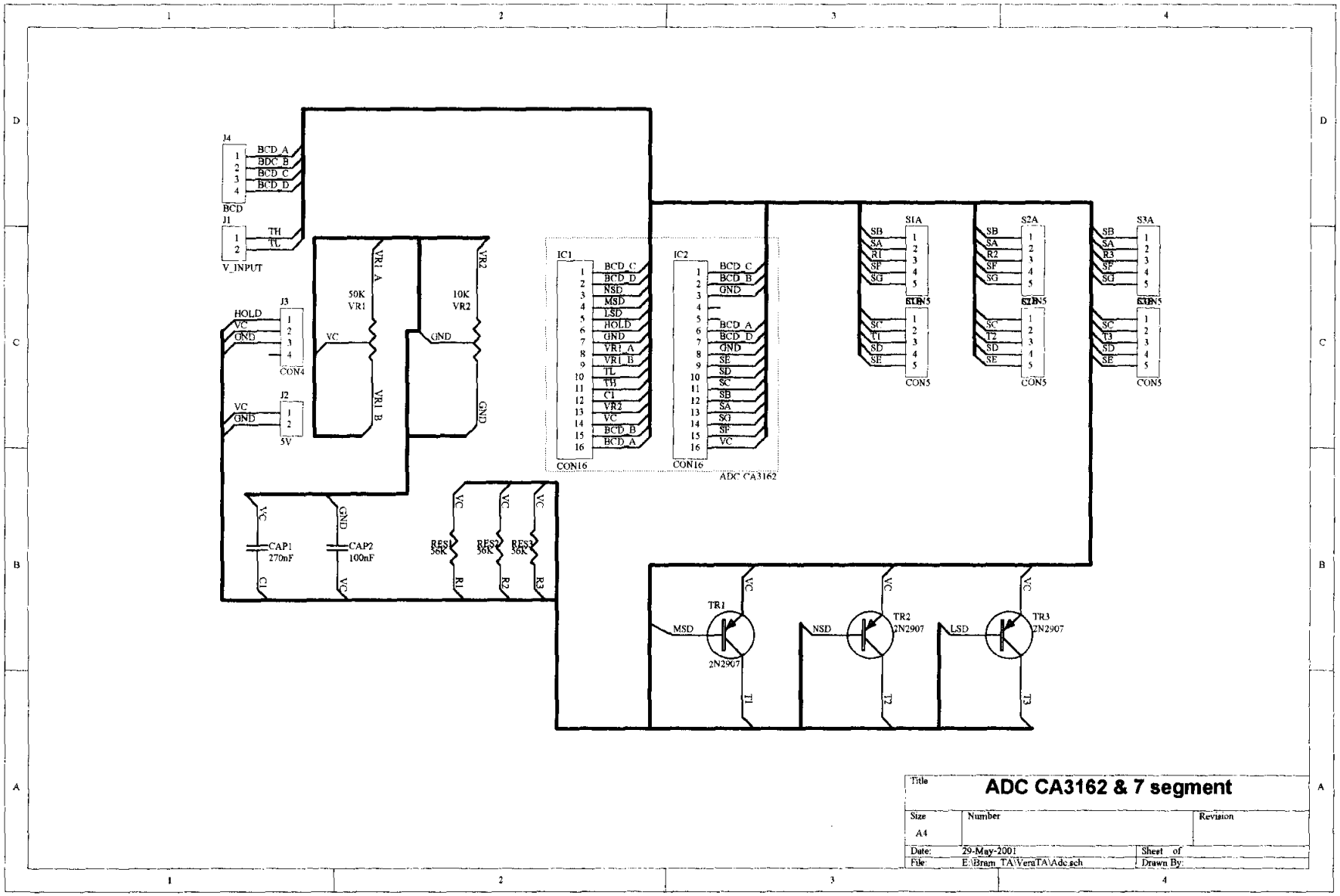
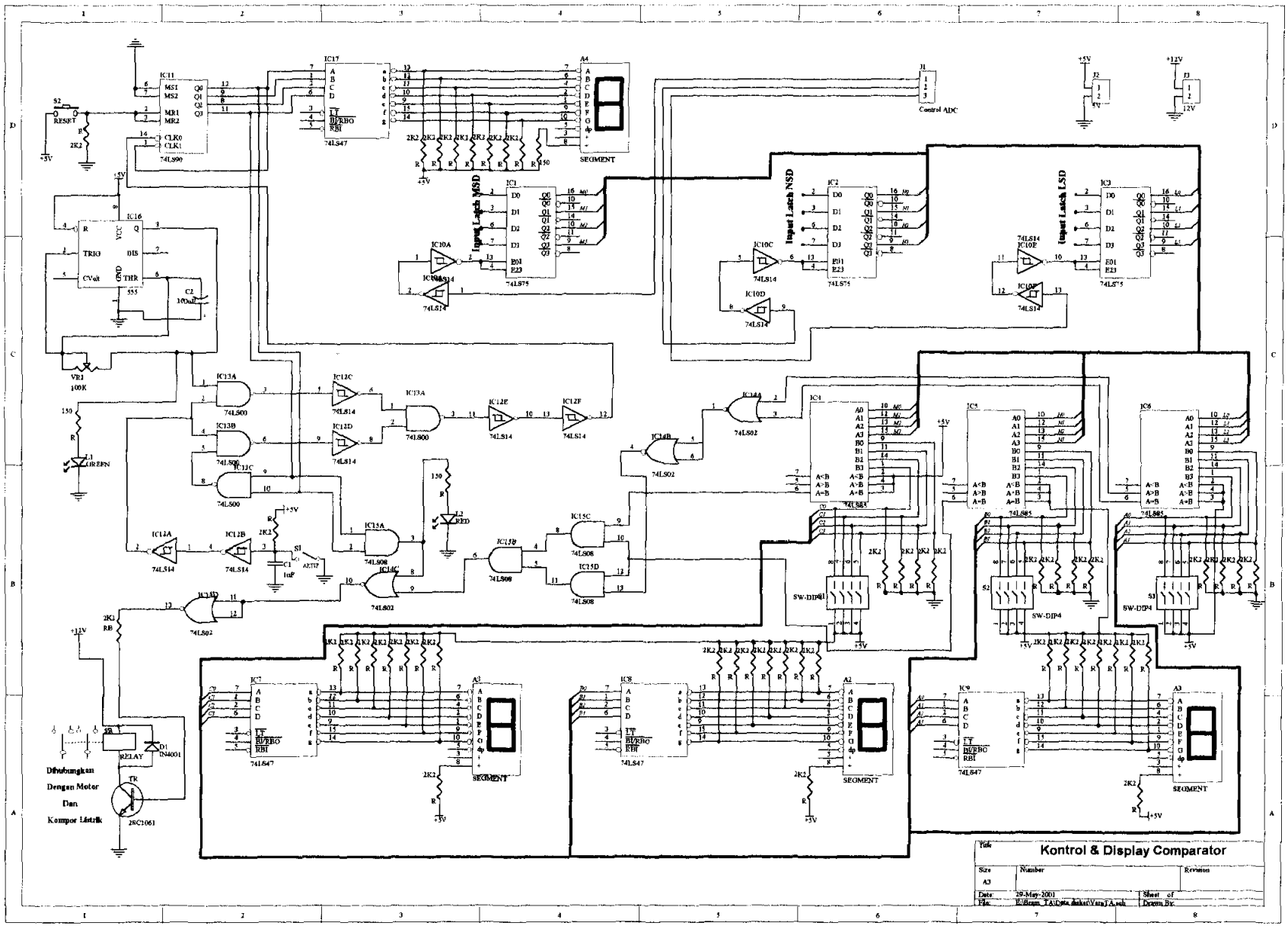
LAMPIRAN



Title	**ADC CA3162 & 7 segment**	
Size: A4	Number:	Revision:
Date: 29-May-2001		Sheet of
File: E:\Bram_TA\VeruTA\Adc.sch		Drawn By:


Kontrol & Display Comparator
Size
A3
Number
Revision
Date: 29-Mar-2001
File: E:\Ibrm_TA\Dft_duket\Vers1A.sch
Sheet of
Drawn By:
Dihubungkan
Dengan Motor
Dan
Kompor Listrik
RESET
Control ADC
Input Latch MSD
Input Latch NSD
Input Latch LSD
SEGMENT
SW-DIP4
RELAY
D1
IN4001
2SC1061
555
74LS90
74LS47
74LS75
74LS14
74LS00
74LS02
74LS08
74LS85

The circuit's transient response, when the input shifted from 1260Hz to 1540Hz and when an R, C passive loop filter was used, is shown in Figure 4. The cutoff frequency of the R, C passive, Figure 3B, was set at 53Hz. The VCO output jitter, Figure 4B, was $\Delta t = 90ns$ and was measured over 5 periods. This yields a $\Delta t/5T \times 100\% = 0.32\%$ total phase jitter of the output frequency, $f_{OUT} = 1400 \times 128 = 179.2kHz$.

Figures 4C and 4D show the loop's performance when an LTC1062 replaces the R, C passive filter. The LTC1062 was set for a cutoff frequency of $f_C = 250Hz$ or 1/5 of the $f_{IN(MIN)}$. The internal oscillator of the LTC1062 was set at 43kHz or 172 times its cutoff frequency. The VCO output jitter was $\Delta t = 30ns$ (or 0.09%) and was measured over 6 periods. Note the excellent transient response of the circuit, Figure 4C, when compared to the underdamped response, Figure 4A.

These two PLL cases demonstrate the advantages of using the LTC1062 as a loop filter in conjunction with the CD4046B phase locked loop. For a variety of low frequency inputs and high ÷ N numbers, the LTC1062 allows the loop to simultaneously achieve good transient response and minimum output jitter. For best results, use the LTC1062 for PLL input frequencies below 5kHz and when the CD4046B operates with a single 5V supply, set 2.75V bias at the VCO input as the center of the tracking range. The minimum and maximum locking range settings of the VCO input should then be 2.25V and 3.25V, respectively.

Clock Sweepable Pseudo Bandpass/Notch Filters

If the feedback capacitor from pins 1 to 7 is replaced with a resistor, Figure 5, the circuit loses its lowpass characteristics and the response of the filter becomes selective like a bandpass. Also, since the two external components (R2, R1) are frequency independent, *the LTC1062 can be fully swept with an external clock.*

Figure 6 shows the frequency response of Figure 5, for a clock frequency of 100kHz. Figure 7 shows the variation of the peak gain, Hop, and the peak frequency, f_p, of Figure 6 versus different values of the (R1/R2) resistor ratio.

As can be seen from Figure 7, the resistor ratio (R1, R2) alters mainly the peak gain of the filter and has very little effect on the value of the peak frequency of Figures 5 or 6. Because of this, two LTC1062s can now be stagger-tuned with a common clock, as shown in Figures 8 and 9, to produce a respectable bandpass response.

In Figure 6, the – 180° phase shift occurs just before the frequency of the peak. Using this property and summing

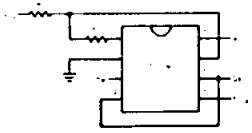


Figure 5

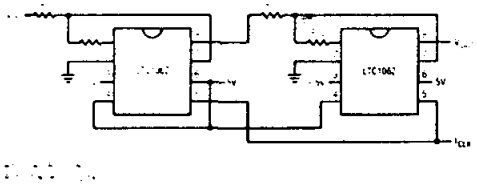


Figure 8. Cascading Two LTC1062s to Form a Very Selective Clock Sweepable Bandpass

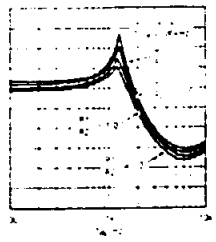


Figure 6

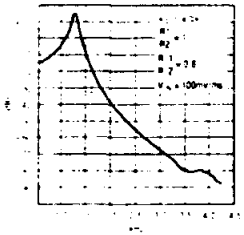


Figure 9

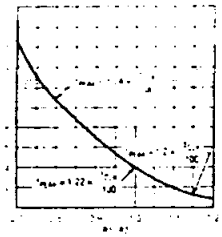


Figure 7

the output of the bandpass filter, Figure 10, with the input voltage, a clock tunable notch response is realized, Figure 11. The clock to notch frequency ratio is 79.3:1 and it is predictable and repeatable from part to part. The notch frequency response of Figure 11 is obtained by setting the ratio (R1/R2) equal to 1.24 and by letting all the gain resistors be equal. Standard 1% value resistors will produce a 40dB deep notch. Additional notch depth can be obtained by tuning resistor R1.

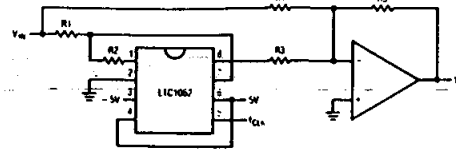


Figure 10. Clock Tunable Notch Filter
For simplicity use R3 = R4 = R5 = 10k;
$\frac{R1}{R2} = 1.234$, $\frac{f_{CLK}}{f_{notch}} = \frac{79.3}{1}$

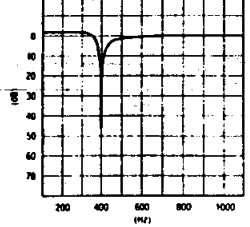


Figure 11. LTC1062 Notch Response

Accommodating High Input Voltages

High input voltages outside the input common-mode range of the LTC1062 can be divided down through a simple resistor divider, *Figure 12.* The DC gain of the lowpass filter is R2/(R1 + R2) and for maximum passband flatness, the paralleled combination of R1, R2 should be chosen as:

$$\frac{1}{2\pi(R1//R2) \times C} = \frac{f_{CUTOFF}}{1.63}; R1//R2 \geq 5k\Omega$$

Note, in Figure 12, there is no need for an external op amp to buffer the divided down input voltage. The internal buffer input, pin 7, performs this function.

An obvious and often encountered application is to use this technique to interface the LTC1062 with op amps powered from ± 15V supplies, Figure 13. Two inexpensive 7V zeners limit the LTC1062 power supply voltage to ± 8V; meanwhile, the output of the op amp A is divided by 2. The DC accurate output of the LTC1062 is then amplified by 2. For this application, an LT1013 precision dual op amp is recommended. The maximum DC output voltage will be 300μV if the A grade of the LT1013 is used.

Programming Various Cutoff Frequencies

To obtain several cutoff frequencies with a single LTC1062, the clock frequency and the external R x C product should be simultaneously varied such as:

$$\frac{1}{2\pi RC} = \frac{f_C}{1.64} = \frac{f_{CLOCK}}{164}$$

For instance, to double the filter's cutoff frequency, we should double the clock frequency and, at the same time, divide by two the R x C product of the external resistor-capacitor combination. With a dual four channel multiplexer, we can easily obtain four different cutoff frequencies by selecting four input resistors *and four clock* frequencies. In Figure 14, the clock frequencies, all of them being ≤ 50kHz, where derived through a simple R, C oscillator.

Applying an External Clock Before the Power Supplies are ON

If the clock at pin 5 is externally applied before the power supplies turn ON, the device will latch. To avoid this, insert a 500Ω resistor or in series with pin 5. This will prevent latch up over temperature. If the power supplies exceed ±6V, the input protection resistor should be increased to 1k.

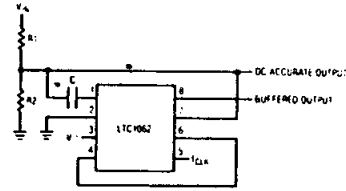


Figure 12. Using Input Resistor Divider to Accommodate High DC and/or AC Input Voltages. Pin 7 DC Buffers the Input Voltage.

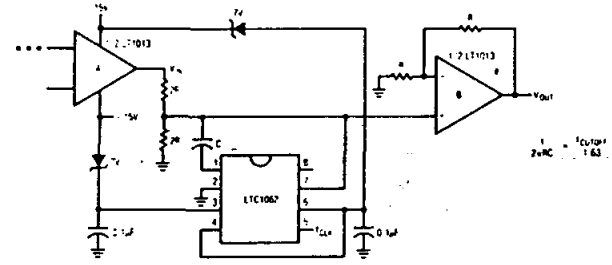


Figure 13. Using the LTC1062 in Conjunction with Precision Op Amps Operating from ± 15V Power Supply

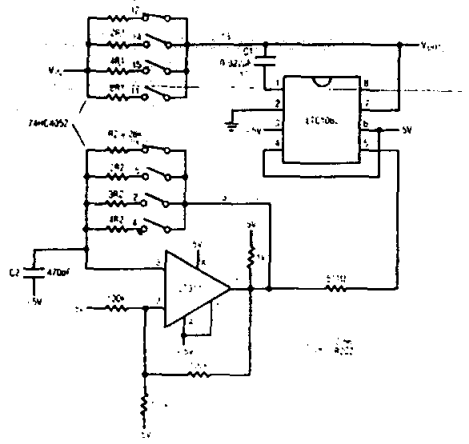


Figure 14. Using a Dual 4 Channel Multiplexer to Obtain Four Different Cutoff Frequencies (500Hz, 250Hz, 125Hz, 62.5Hz)

Thermocouple Measurement

Jim Williams

Introduction

In 1822, Thomas Seebeck, an Estonian physician, accidentally joined semicircular pieces of bismuth and copper (Figure 1) while studying thermal effects on galvanic arrangements. A nearby compass indicated a magnetic disturbance. Seebeck experimented repeatedly with different metal combinations at various temperatures, noting relative magnetic field strengths*. Curiously, he did not believe that electric current was flowing, and preferred to describe the effect as "thermo-magnetism." He published his results in a paper, "Magnetische Polarisation der Metalle und Erze durch Temperatur-Differenz" (see references)

Subsequent investigation has shown the "Seebeck Effect" to be fundamentally electrical in nature, repeatable, and quite useful. Thermocouples, by far the most common transducer, are Seebeck's descendants.

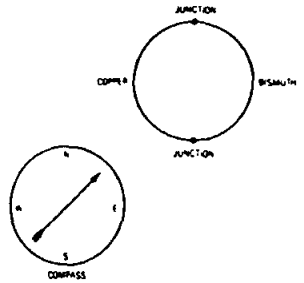


Figure 1. The Arrangement for Dr. Seebeck's Accidental Discovery of "Thermo-Magnetism"

Thermocouples in Perspective

Temperature is easily the most commonly measured physical parameter. A number of transducers serve temperature measuring needs and each has advantages and considerations. Before discussing thermocouple based measurement it is worthwhile putting these sensors in perspective. Figure 2's chart shows some common contact temperature sensors and lists characteristics. Study reveals thermocouple strengths and weaknesses compared to other sensors. In general, thermocouples are inexpensive, wide range sensors. Their small size makes them fast and their low output impedance is a benefit. The inherent voltage output eliminates the need for excitation.

Signal Conditioning Issues

Potential problems with thermocouples include low level outputs, poor sensitivity and non-linearity (see Figures 3 and 4). The low level output requires stable signal conditioning components and makes system accuracy difficult to achieve. Connections (see Appendix A) in thermocouple systems must be made with great care to get good accuracy. Unintended thermocouple effects (e.g., solder and copper create a 3μV/°C thermocouple) in system connections make "end-to-end" system accuracies better than 0.5°C difficult to achieve.

TYPE	RANGE OF OPERATION	SENSITIVITY AT +25°C	ACCURACY	LINEARITY	SPEED IN STIRRED OIL	SIZE	PACKAGE	COST	COMMENTS
Thermocouples (All Types)	-270°C to +1800°C	Typically less than 50μV/°C	±0.5°C with Reference	Poor over wide range, better over a 100°C	Typically 1 Sec. Some Types are Faster	0.02 In. Bead Typical, 0.0005 In. Units are Available	Metallic Bead, Variety of Probes Available.	$1 to $50 Depending on Type, Specifications and Package.	Requires Reference. Low Level Output Requires Stable Signal Conditioning Components.
Thermistors and Thermistor Composites	-100°C to +450°C	±5%/°C for Thermistors, ±0.5%/°C for Linearized Units	±0.1°C Standard from -40°C to +100°C, ±0.01°C from 0°C to +50°C Available	±0.2°C for Linearized Composite Units over 100°C Ranges	1 to 10 Sec. is Standard, 3 to 100ms Types are Available	Beads Can be as Small as 0.005 In., But 0.04 to 0.1 In. is Typical. "Flake" Types are Only 0.001 In. Thick.	Glass, Epoxy, Teflon Encapsulated, Metal Housing, Etc.	$2 to $10 for Standard Units, $10 to $30 for High Precision Types and Specials	Highest Temperature Sensitivity of All Common Sensors. Special Units Required for Long Term Stability Above +100°C.
Platinum Resistance Wire	-250°C to +900°C	Approximately +0.5%/°C	±0.1°C Readily Available, ±0.01°C in Precision Standards — Lab Units	Nearly Linear Over Large Spans; Typically Within 1° Over 200°C Ranges	Typically Several Seconds	1/8 to 1/4 In. Typical, Smaller Sizes Available	Glass, Epoxy, Ceramic, Teflon, Metal, Etc.	$25 to $1000 Depending on Specs. Most Industrial Types Below $100	Best Standard Stability Over Long Term. Has Wider Temp. Range Than Thermistor, but Lower Sensitivity
Diodes and Transistors	-270°C to +175°C	-2.2 mV/°C (Approx. 0.33%/°C)	±2°C to ±5°C Over -55°C to +125°C	Within 2° Over Operating Range	1 to 10 Sec. is Standard. Small Diode Packages Permit Speeds in ms Range	Standard Diode and Transistor Case Sizes. Glass Passivated Chips Permit Extremely Small Sizes.	Glass, Metal	Below 50 ¢. Cryogenic Units More Expensive	Require Individual Calibration. Must be Driven from Current Source for Optimum Performance. Extremely Inexpensive. Calibrated Cryogenic Types Available.
Integrated Circuit	-85°C to +125°C Typical	0.4%/°C Typical	Over -55°C to +125°C	Within 1° (0.2° From 0°C to +70°C) Typical	Several Seconds	TO-18 Transistor Package Size. Also MiniDIP	Metal, Plastic	$1 to $10	Current and Voltage Outputs Available

Figure 2. Characteristics of Some Contact Temperature Sensors (Chart Adapted from Reference 2)

JUNCTION MATERIALS	APPROXIMATE SENSITIVITY IN μV/°C AT 25°C	USEFUL TEMPERATURE RANGE (°C)	APPROXIMATE VOLTAGE SWING OVER RANGE	LETTER DESIGNATION
Copper — Constantan	40.6	-270 to +600	25.0mV	T
Iron — Constantan	51.70	-270 to +1000	60.0mV	J
Chromel — Alumel	40.6	-270 to +1300	55.0mV	K
Chromel — Constantan	60.9	-270 to +1000	75.0mV	E
Platinum 10% — Rhodium/Platinum	6.0	0 to +1550	16.0mV	S
Platinum 13% — Rhodium/Platinum	6.0	0 to +1600	19.0mV	R

Figure 3. Temperature vs Output for Some Thermocouple Types

(Figure 3). The term "cold junction" derives from the historical practice of maintaining the reference junction at 0°C in an ice bath. Ice baths, while inherently accurate, are impractical in most applications. Another approach servo controls a Peltier cooler, usually at 0°C, to electronically simulate the ice bath (Figure 6). This approach* eliminates ice bath maintenance, but is too complex and bulky for most applications.

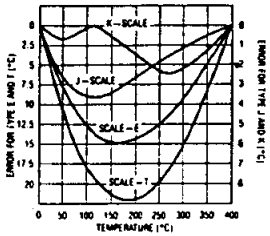


Figure 4. Thermocouple Nonlinearity for Types J, K, E and T Over 0°C–400°C. Error Increases Over Wider Temperature Ranges.

Cold Junction Compensation

The unintended, unwanted and unavoidable parasitic thermocouples require some form of temperature reference for absolute accuracy. (See Appendix A for a discussion on minimizing these effects). In a typical system, a "cold junction" is used to provide a temperature reference

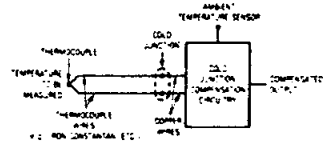


Figure 7. Typical Cold Junction Compensation Arrangement. Cold Junction and Compensation Circuitry must be Isothermal

Figure 7 conveniently deals with the cold junction requirement. Here, the cold junction compensator circuitry does not maintain a stable temperature but tracks the cold junction. This temperature tracking, subtractive term has the same effect as maintaining the cold junction at constant temperature, but is simpler to implement. It is designed to produce 0V output at 0°C and have a slope equal to the thermocouple output (Seebeck coefficient) over the expected range of cold junction temperatures. For proper operation, the compensator must be at the same temperature as the cold junction.

Figure 8 shows a monolithic cold junction compensator IC, the LT1025. This device measures ambient (e.g., cold junction) temperature and puts out a voltage scaled for use with the desired thermocouple. The low supply current minimizes self-heating, ensuring isothermal operation with the cold junction. It also permits battery or low power operation. The 0.5°C accuracy is compatible with overall achievable thermocouple system performance. Various

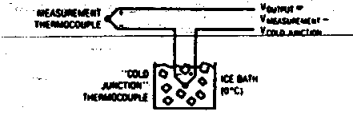


Figure 5. Ice Bath Based Cold Junction Compensator

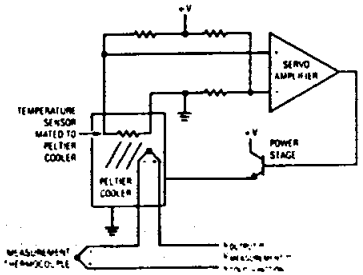


Figure 6. A 0°C Reference Based on Feedback Control of a Peltier Cooler (Sensor is Typically a Platinum RTD)

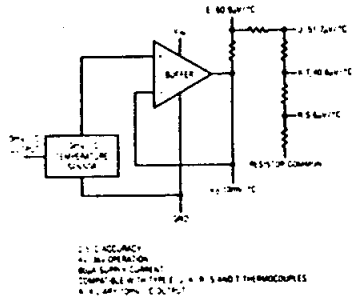


Figure 8. LT1025 Thermocouple Cold Junction Compensator

compensated outputs allow one part to be used with many thermocouple types. Figure 9 uses an LT1025 and an amplifier to provide a scaled, cold junction compensated output. The amplifier provides gain for the difference between the LT1025 output and the type J thermocouple. C1 and C2 provide filtering, and R5 trims gain. R6 is a typical value, and may require selection to accommodate R5's trim range. Alternately, R6 may be re-scaled, and R5 enlarged, at some penalty in trim resolution. Figure 10 is similar, except that the type K thermocouple subtracts from the LT1025 in series-opposed fashion, with the residue fed to the amplifier. The optional pull down resistor allows readings below 0°C.

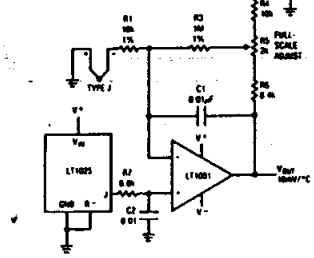


Figure 9. LT1025 Cold Junction Compensates a Type J Thermocouple. The Op Amp Provides the Amplified Difference Between the Thermocouple and the LT1025 Cold Junction Output.

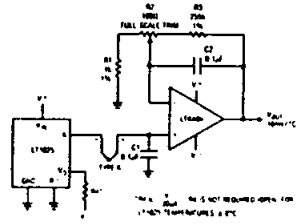


Figure 10. LT1025 Compensates a Type K Thermocouple. The Amplifier Provides Gain for the LT1025-Thermocouple Difference.

Amplifier Selection

The operation of these circuits is fairly straightforward, although amplifier selection requires care.

Thermocouple amplifiers need very low offset voltage and drift, and fairly low bias current if an input filter is used. The best precision bipolar amplifiers should be used for type J, K, E, and T thermocouples which have Seebeck coefficients of 40–60μV/°C. In particularly critical applications, or for R and S thermocouples (6–15μV/°C), a chopper-stabilized amplifier is required. Linear Technology offers two amplifiers specifically tailored for thermocouple applications. The LTKA0x is a bipolar design with extremely low offset (30μV), low drift (1.5μV/°C), very low bias current (1nA), and almost negligible warm-up drift (supply current is 400μA).

For the most demanding applications, the LTC1052 CMOS chopper-stabilized amplifier offers 5μV offset and 0.05μV/°C drift. Input bias current is 30pA, and gain is typically 30 million. This amplifier should be used for R and S thermocouples, especially if no offset adjustments can be tolerated, or where a large ambient temperature swing is expected. Alternatively, the LTC1050, which has similar drift and slightly higher noise can be used. If board space is at a premium, the LTC1050 has the capacitors internally.

Regardless of amplifier type, for best possible performance dual-in-line (DIP) packages should be used to avoid thermocouple effects in the kovar leads of TO-5 metal can packages. This is particularly true if amplifier supply current exceeds 500μA. These leads can generate both DC and AC offset terms in the presence of thermal gradients in the package and/or external air motion.

environments, and some sort of input filter is required. To reject 60Hz pick-up with reasonable capacitor values, input resistors in the 10k–100k range are needed. Under these conditions, bias current for the amplifier needs to be less than 1nA to avoid offset and drift effects.

To avoid gain error, high open loop gain is necessary for single-stage thermocouple amplifiers with 10mV/°C or higher outputs. A type K amplifier, for instance, with 100mV/°C output, needs a closed loop gain of 2,500. An ordinary op amp with a minimum loop of 50,000 would have an initial gain error of (2,500)(50,000) = 5%! Although closed loop gain is commonly trimmed, temperature drift of open loop gain will have a deleterious effect on output accuracy. Minimum suggested loop gain for type E, J, K, and T thermocouples is 250,000. This gain is adequate for type R and S if output scaling is 10mV/°C or less.

Additional Circuit Considerations

Other circuit considerations involve protection and common-mode voltage and noise. Thermocouple lines are often exposed to static and accidental high voltages, necessitating circuit protection. Figure 11 shows two suggested approaches. These examples are designed to prevent excessive overloads from damaging circuitry. The added series resistance can serve as part of a filter. Effects of the added components on overall accuracy should be evaluated. Diode clamping to supply lines is effective, but leakage should be noted, particularly when large current limiting resistors are used. Similarly, IC bias currents combined with high value protection resistors can generate apparent measurement errors. Usually, a favorable compromise is possible, but sometimes the circuit configuration will be dictated by protection or noise rejection requirements.

Differential Thermocouple Amplifiers

Figure 12A shows a way to combine filtering and full differential sensing. This circuit features 120dB DC common-mode rejection if all signals remain within the LTC1043 supply voltage range. The LTC1043, a switched capacitor building block, transfers charge between the input "flying" capacitor and the output capacitor. The LTC1043's commutating frequency, which is settable, controls rate of charge transfer, and hence overall bandwidth. The differential inputs reject noise and common-mode voltages inside the LTC1043's supply rails. Excursions outside these limits require protection networks, as previously discussed. As in Figure 9, an optional resistor pull-down permits negative readings. The 1M resistor provides a bias path for the LTC1043's floating inputs. Figure 12B, for use with grounded thermocouples, subtracts sensor output from the LT1025.

Isolated Thermocouple Amplifiers

In many cases, protection networks and differential operation are inadequate. Some applications require continuous operation at high common-mode voltages with severe noise problems. This is particularly true in industrial environments, where ground potential differences of 100V are

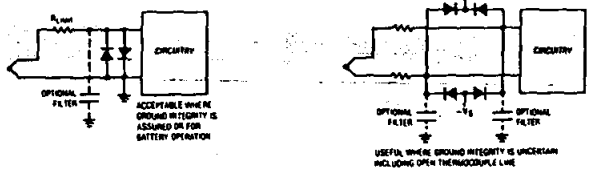


Figure 11. Input Protection Schemes

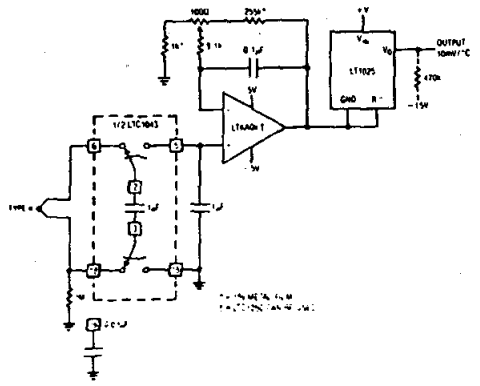


Figure 12A. Full Differential Input Thermocouple Amplifiers

common. Under these conditions the thermocouple and signal conditioning circuitry must be completely galvanically isolated from ground. This requires a fully isolated power source and an isolated signal transmission path to the ground referred output. Thermocouple work allows bandwidth to be traded for DC accuracy. With careful design, a single path can transfer floating power and isolated signals. The output may be either analog or digital, depending on requirements.

Figure 13 shows an isolated thermocouple signal conditioner which provides 0.25% accuracy at 175V common-mode. A single transformer transmits isolated power and data. 74C14 inverter I1 forms a clock (trace A, Figure 14). I2, I3 and associated components deliver a stretched pulse to the 2.2k resistor (trace B). The amplitude of this pulse is stabilized because A1's fixed output supplies 74C14 power. The resultant current through the 2.2k resistor drives L1's primary (trace E). A pulse appears at L1's secondary (trace F, Q2's emitter). A2 compares this amplitude with A5's signal conditioned thermocouple voltage. To close its loop, A2's output (trace G) drives Q2's base to force L1's secondary (pins 3-6) to clamp at A5's output value. Q2 operates in inverted mode, permitting clamping action even for very low A5 outputs. When L1's secondary (trace F) clamps, its primary (trace E) also clamps. After A2 settles, the clamp value is stable. This stable clamp value represents A5's thermocouple related information. Inverter I4 generates a clock delayed pulse (trace C) which is fed to A3, a sample-hold amplifier. A3 samples L1's primary winding clamp value. A4 provides gain scaling and the LT1004 and associated components adjust offset. When

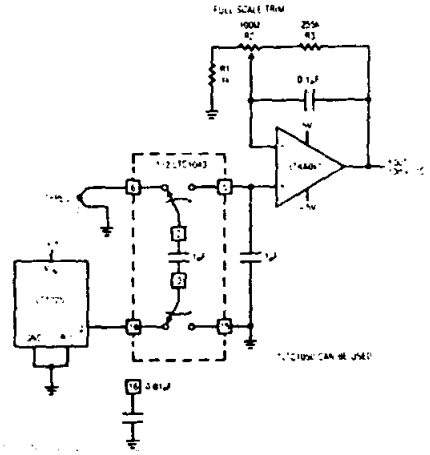


Figure 12B.

the clock pulse (trace A) goes low, sampling ceases. When trace B's stretched clock pulse goes low, the I5-I6 inverter chain output (trace D) is forced low by the 470k-75pF differentiator's action. This turns on Q1, forcing substantial energy into L1's primary (trace E). L1's secondary (trace F) sees large magnetic flux. A2's output (trace G) too great, however, and A2 rails. The excess energy is dumped into the pin 1-4 winding, placing a large current pulse (trace H) into the 22µF capacitor. This current pulse occurs with each clock pulse, and the capacitor charges to a DC voltage, furnishing the circuit's isolated supply. When the 470k-75pF differentiator times out, the I5-I6 output goes high, shutting off Q1. At the next clock pulse the entire cycle repeats.

Figure 14. Waveforms for Figure 12's Thermocouple Isolation Amplifier

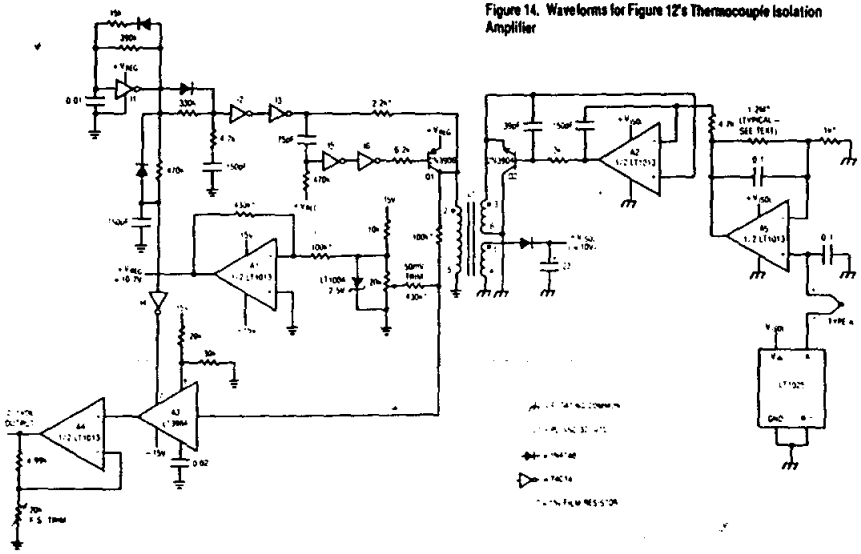


Figure 13. 0.25% Thermocouple Isolation Amplifier

Proper operation of this circuit relies on several considerations. Achievable accuracy is primarily limited by transformer characteristics. Current during the clamp interval is kept extremely low relative to transformer core capacity. Additionally, the clamp period must also be short relative to core capacity. The clamping scheme relies on avoiding core saturation. This is why the power refresh pulse occurs immediately after data transfer, and not before. The transformer must completely reset before the next data transfer. A low clock frequency (350Hz) ensures adequate transformer reset time. This low clock frequency limits bandwidth, but the thermocouple data does not require any speed.

Gain slope is trimmed at A5, and will vary depending upon the desired maximum temperature and thermocouple type. The "50mV" trim should be adjusted with A5's output at 50mV. The circuit cannot read A5 outputs below 20mV (0.5% of scale) due to Q2's saturation limitations.

Drift is primarily due to the temperature dependence of L1's primary winding copper. This effect is swamped by the 2.2k series value with the 60ppm/°C residue partially compensated by I3's saturation resistance tempco. Overall tempco, including the LT1004, is about 100ppm/°C. Increased isolation voltages are possible with higher transformer breakdown ratings.

Figure 15's thermocouple isolation amplifier is somewhat more complex, but offers 0.01% accuracy and typical drift of 10ppm/°C. This level of performance is useful in servo systems or high resolution applications. As in Figure 13, a single transformer provides isolated data and power transfer. In this case the thermocouple information is width modulated across the transformer and then demodulated back to DC. I1 generates a clock pulse (trace A, Figure 16). This pulse sets the 74C74 flip-flop (trace B) after a small delay generated by I2, I3 and associated components. Simultaneously, I4, I5 and Q1 drive L1's primary (trace C). This energy, received by L1's secondary (trace H), is stored in the 47µF capacitor and serves as the circuit's isolated supply. L1's secondary pulse also clocks a closed loop pulse width modulator composed of C1, C2, A3 and A4. A4's positive input receives A5's LT1025 based thermocouple signal. A4 servo-biases C2 to produce a pulse width each time C1 allows the 0.003µF capacitor (trace E)

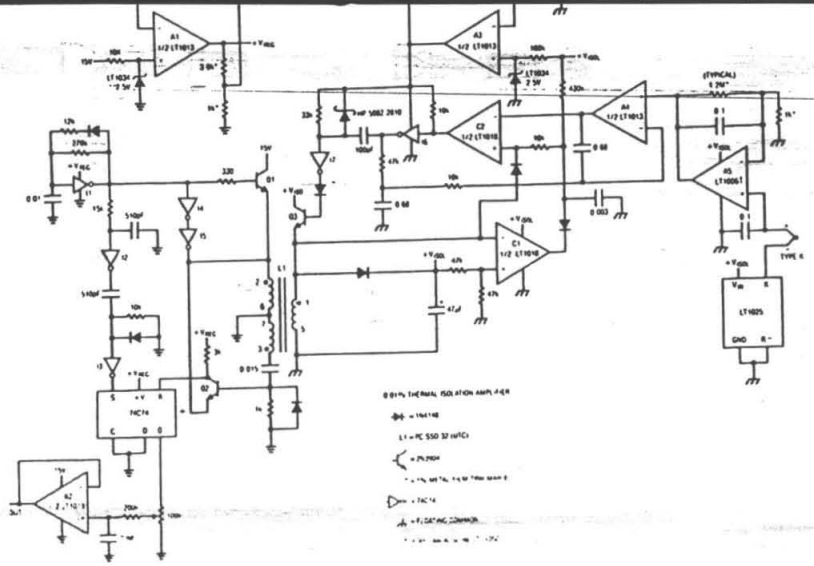


Figure 15. 0.01% Thermocouple Isolation Amplifier

to receive charge via the 430kΩ resistor. C2's output width is inverted by I6 (trace F), integrated to DC by the 47k-0.68μF filter and fed back to A4's negative input. The 0.68μF capacitor compensates A4's feedback loop. A4 servo controls C2 to produce a pulse width that is a function of A5's thermocouple related output. I6's low loss MOS switching characteristics combined with A3's supply stabilization ensure precise control of pulse width by A4. Operating frequency, set by the I1 oscillator on L1's primary side, is normally a stability concern, but ratios out because it is common to the demodulation scheme, as will be shown.

I6's output width's (trace F) negative-going edge is differentiated and fed to I7. I7's output (trace G) drives Q3. Q3 puts a fast spike into L1's secondary (trace H). "Sing around" behavior by C1 is gated out by the diode at C2's positive input. Q3's spike is received at L1's primary, pins 7 and 3. Q2 serves as a clocked synchronous demodulator, pulling its collector low (trace D) only when its base is high and its emitter is low (e.g., when L1 is transferring data, not power). Q2's collector spike resets the 74C74 flip-flop. The MOS flip-flop is driven from a stable source (A1) and it is also clocked at the same frequency as the pulse width modulator. Because of this, the DC average of its Q output depends on A5's output. Variations with supply, temperature and I1 oscillator frequency have no effect. A2 and its associated components extract the DC average by simple filtering. The 100k potentiometer permits desired gain scaling. Because this scheme depends on edge timing at the flip-flop, the delay in resetting the 0.003μF capacitor causes a small offset error. This term is eliminated by matching this delay in the 74C74 "set" line with the previously mentioned I2-I3 delay network. This delay is set so that the rising edge of the flip-flop output (trace B) corresponds to I6's rising edge. No such compensation is required for falling edge data because circuit elements in this path (I7, Q3, L1 and Q2) are wideband. With drift matched LT1004s and the specified resistors, overall drift is typically 10ppm/°C with 0.01% linearity.

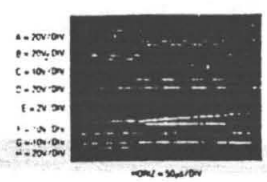


Figure 16. Pulse-Width-Modulation Based Thermocouple Isolation Amplifier Waveforms

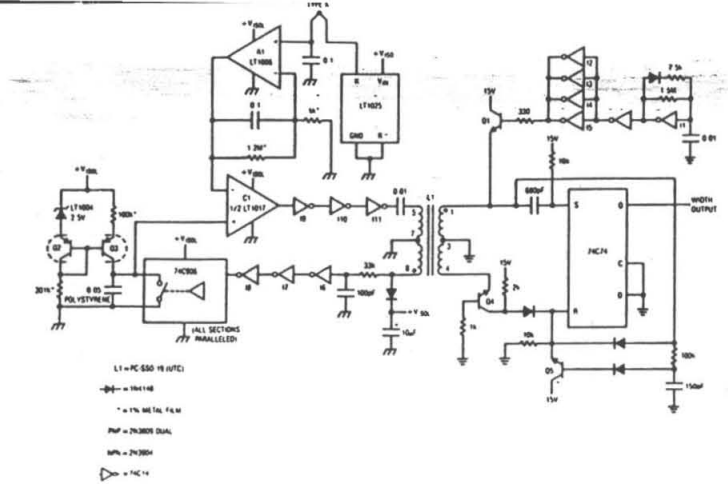


Figure 17. Digital Output Thermocouple Isolator

Digital Output Thermocouple Isolator

Figure 17 shows another isolated thermocouple signal conditioner. This circuit has 0.25% accuracy and features a digital (pulse width) output. I1 produces a clock pulse (trace A, Figure 18). I2-I5 buffers this pulse and biases Q1 to drive L1. Concurrently, the 680pF-10k values provide a differentiated spike (trace B), setting the 74C74 flip-flop (trace C). L1's primary drive is received at the secondary.

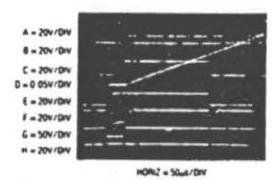


Figure 18. Waveforms for Digital-Output Thermocouple Isolator

The 10μF capacitor charges to DC, supplying isolated power. The pulse received at L1's secondary also resets the 0.05μF capacitor (trace D) via the inverters (I6, I7, I8) and the 74C906 open drain buffer. When the received pulse ends, the 0.05μF capacitor charges from the Q2-Q3 current source. When the resultant ramp crosses C1's threshold (A1's thermocouple related output voltage) C1 switches high, tripping the I9-I11 inverter chain. I11 (trace E) drives L1's secondary via the 0.01μF capacitor (trace F). The 33k-100pF filter prevents regenerative "sing around". The resultant negative-going spike at L1's primary biases Q4, causing its collector (trace G) to go low. Q4 and Q5 form a clocked synchronous demodulator which can pull the 74C74 reset pin low only when the clock is low. This condition occurs during data transfer, but not during power transfer. The demodulated output (trace H) contains a single negative spike synchronous with C1's (e.g., I11's) output transition. This spike resets the flip-flop, providing the circuit output. The 74C74's width output thus varies with thermocouple temperature.

Linearization Techniques

It is often desirable to linearize a thermocouple based signal. Thermocouples' significant nonlinear response requires design effort to get good accuracy. Four techniques are useful. They include offset addition, breakpoints, analog computation, and digital correction. Offset addition schemes rely on biasing the nonlinear "bow" with a constant term. This results in the output being high at low scale and low at high scale with decreased errors between these extremes (Figure 19). This compromise reduces overall error. Typically, this approach is limited to slightly nonlinear behavior over wide ranges or larger nonlinearity over narrow ranges.

Figure 20 shows a circuit utilizing offset linearization for a type S thermocouple. The LT1025 provides cold junction compensation and the LTC1052 chopper stabilized amplifier is used for low drift. The type S thermocouple output slope varies greatly with temperature. At 25°C it is 6μV/°C, with an 11μV/°C slope at 1000°C. This circuit gives 3°C accuracy over the indicated output range. The circuit, similar to Figure 10, is not particularly unusual except for the offset term derived from the LT1009 and applied through R4. To calibrate, trim R5 for $V_{OUT} = 1.669$ at $V_{IN} = 0.000mV$. Then, trim R2 for $V_{OUT} = 9.998V$ at T = 1000°C or for V_{IN} (+ input) = 9.585mV.

Figure 21, an adaption of a configuration shown by Sheingold (reference 3), uses breakpoints to change circuit gain as input varies. This method relies on scaling of the input

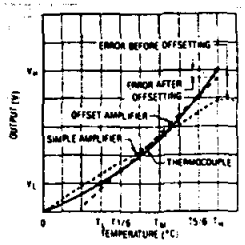


Figure 19. Offset Curve Fitting

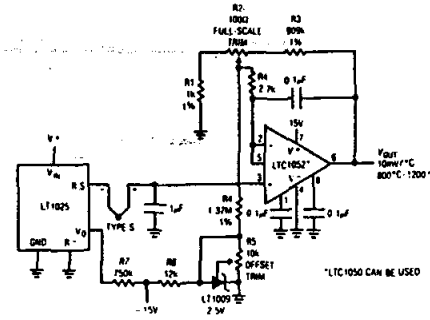


Figure 20. Offset Based Linearization

and feedback resistors associated with A2-A6 and A7's reference output. Current summation at A8 is linear with the thermocouple's temperature. A3-A6 are the breakpoints, with the diodes providing switching when the respective summing point requires positive bias. As shown, typical accuracy of 1°C is possible over a 0°C-650°C sensed range.

Figure 22, also derived from Sheingold (reference 3), yields similar performance but uses continuous function analog computing to replace breakpoints, minimizing amplifiers and resistors. The AD538 combines with a single breakpoint and appropriate scaling to linearize response. The causality of this circuit is similar to Figure 22; the curve fit mechanism (breakpoint vs. continuous function) is the primary difference.

Digital techniques for thermocouple linearization have become quite popular. Figure 23, developed by Guy M. Hoover and William C. Rempfer, uses a microprocessor fed from a digitized thermocouple output to achieve linearization. The great advantage of digital techniques is elimination of trimming. In this scheme a large number of breakpoints are implemented in software.

The 10-bit LTC1091A A/D gives 0.5°C resolution over a 0°C to 500°C range. The LTC1052 amplifies and filters the thermocouple signal, the LT1025A provides cold junction compensation and the LT1019A provides an accurate reference. The J type thermocouple characteristic is linearized digitally inside the processor. Linear interpolation between known temperature points spaced 30°C apart introduces less than 0.1°C error. The 1024 steps provided by the LTC1091 (24 more than the required 1000) ensure 0.5°C resolution even with the thermocouple curvature.

Offset error is dominated by the LT1025 cold junction compensator which introduces 0.5°C maximum. Gain error is 0.75°C max because of the 0.1% gain resistors and, to a lesser extent, the output voltage tolerance of the LT1019A and the gain error of the LTC1091A. It may be reduced by trimming the LT1019A or gain resistors. The LTC1091A keeps linearity better than 0.15°C. The LTC1052's 5μV offset contributes negligible error (0.1°C or less). Combined errors are typically inside 0.5°C. These errors don't include the thermocouple itself. In practice, connection and wire errors of 0.5°C to 1°C are not uncommon. With care, these errors can be kept below 0.5°C.

The 20k-10k divider on CH1 of the LTC1091 provides low supply voltage detection (the LT1019A reference requires a minimum supply of 6.5V to maintain accuracy). Remote location is possible with data transferred from the MCU to the LTC1091 via the 3 wire serial port.

Figure 24 is a complete software listing* of the code required for the 68HC05 processor. Preparing the circuit involves loading the software and applying power. No trimming is required.

*The use of a software based circuit was not without attendant conscience searching and pain on the author's part. Hopefully, the Analog Faithful will tolerate this transgression. I'm sorry everybody, it just works too well!

References

1. Seebeck, Thomas Dr., "Magnetische Polarisation der Metalle und Erze durch Temperatur-Differenz", Abhaandlungen der Preussischen Akademic der Wissenschaften (1822-1823), pg. 265-373.
2. Williams, J., "Designer's Guide to Temperature Sensors", EDN, May 5, 1977.
3. Sheingold, D.H., "Nonlinear Circuits Handbook", Analog Devices, Inc., pg. 92-97.
4. "Omega Temperature Measurement Handbook", Omega Engineering, Stamford Connecticut.
5. "Practical Temperature Measurements", Hewlett-Packard Applications Note #290, Hewlett-Packard.
6. Thermocouple Reference Tables, NBS Monograph 125, National Bureau of Standards.
7. Manual on the Use of Thermocouples in Temperature Measurement, ASTM Special Publication 470A.

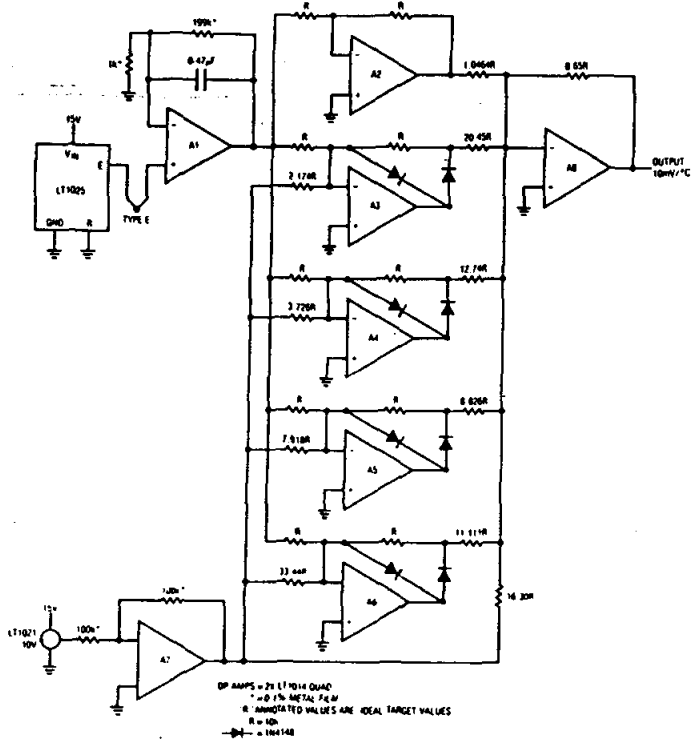


Figure 21. Breakpoint Based Linearization (see Reference 3)

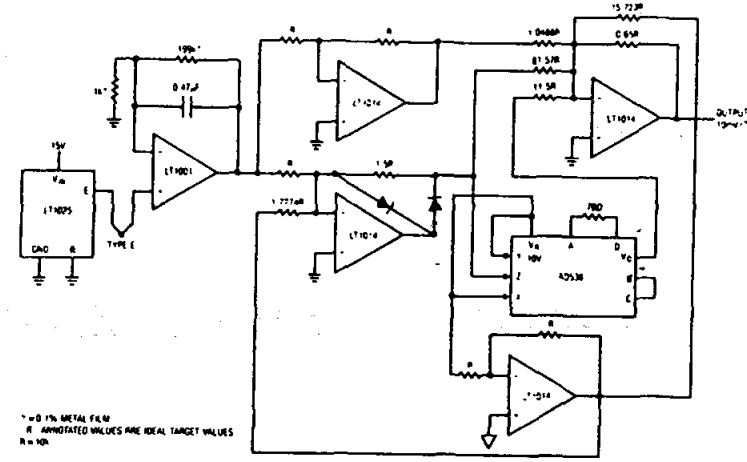


Figure 22. Continuous Function Linearization (see Reference 3)

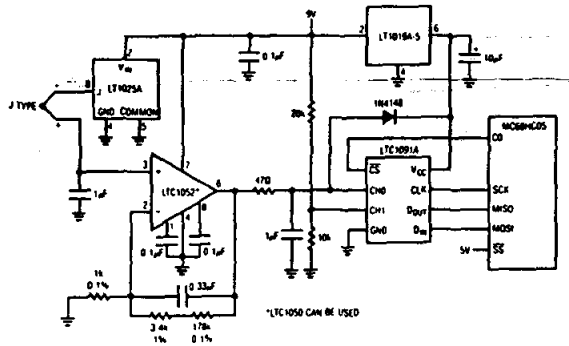


Figure 23. Processor Based Linearization

```
*       TYPE J THERMOCOUPLE LINEARIZATION PROGRAM
*       WRITTEN BY GUY HOOVER LINEAR TECHNOLOGY CORPORATION
*       REV 1  10/4/87
*       N IS NUMBER OF SEGMENTS THAT THERMOCOUPLE RESPONSE IS DIVIDED INTO
*       TEMPERATURE (°C) = M*X + B
*       M IS SLOPE OF THERMOCOUPLE RESPONSE FOR A GIVEN SEGMENT
*       X IS A/D OUTPUT — SEGMENT END POINT
*       B IS SEGMENT START POINT IN DEGREES (°C * 2)
        ORG     $1000
        FCB     $0F,$39,$74,$BC,$EE,$12B,$193,$262,$33C,$39?        TABLE OF X
        ORG     $1020
        FCB     $85CD,$8203A,$7FB4,$7DD4,$7CAF,$7BC8,$7B54,$7D24,$7C1F,$7B3A  TABLE OF M
        ORG     $1040
        FCB     $0C,$3C,$78,$B4,$F0,$12C,$190,$256,$320,$384         TABLE OF B
        ORG     $10FF
        FCB     $13                                                  N - 2
        ORG     $0100
        OPT     I
        STA     $08     LOAD CONFIGURATION DATA INTO $08
        LDA     #$00    CONFIGURATION DATA FOR PORT A DDR
        STA     $04     LOAD CONFIGURATION DATA INTO PORT A
        LDA     #$FF    CONFIGURATION DATA FOR PORT B DDR
        STA     $05     LOAD CONFIGURATION DATA INTO PORT B
        LDA     #$F7    CONFIGURATION DATA FOR PORT C DDR
        STA     $06     LOAD CONFIGURATION DATA INTO PORT C
        JSR     HOUSEKP INITIALIZE ASSORTED REGISTERS
WES92L  NOP
        JSR     CHECK
        LDA     #$6F    D_IN WORD FOR LTC1091 CH0 (W RESPECT TO GND MSB FIRST
        STA     $5C     STORE IN D_IN BUFFER
        JSR     READ91  READ LTC1091
LINEAR  LDX     #$0E    LOAD SEGMENT COUNTER INTO X
DOAGAIN LDA     $1000,X LOAD LSBs OF SEGMENT N
        STA     $55     STORE LSBs IN $55
        DECX            DECREMENT X
        LDA     $1000,X LOAD MSBs OF SEGMENT N
        STA     $54     STORE MSBs IN $54
        JSR     SUBTRCT
        BPL     SEGMENT
        JSR     ADD8
        DECX            DECREMENT X
        JMP     DOAGAIN
SEGMENT LDA     $1020,X LOAD MSBs OF SLOPE
        STA     $54     STORE MSBs IN $54
        INCX            INCREMENT X
        LDA     $1020,X LOAD LSBs OF SLOPE
        STA     $55     STORE LSBs IN $55
        JSR     TB4MULT RETURNS RESULT IN $61 AND $62
        LDA     $1040,X LOAD LSBs OF BASE TEMP
        STA     $55     STORE LSBs IN $55
        DECX            DECREMENT X
        LDA     $1040,X LOAD MSBs OF BASE TEMP
        STA     $54
        JSR     ADD8
CHECK   LDA     #$7F    D_IN WORD FOR CH1
        STA     $50     LOAD D_IN WORD INTO $50
        JSR     READ91  READ BATTERY VOLTAGE
        LDA     #$62    LOAD MSB OF MIN BATT VOLTAGE
        STA     $54     PUT IN MSB OF SUBTRACT BUFFER
        LDA     #$CC    LOAD LSB OF MIN BATT VOLTAGE
        STA     $55     PUT IN LSB OF SUBTRACT BUFFER
```



```
        JSR     SUBTRCT COMPARE BATT VOLTAGE WITH MINIMUM
        BPL     NOPROB  IF BATT OK GOTO NOPROB
        JSR     ADD8
        LDA     #$01
        STA     $56     SET BATTERY LOW FLAG
        RTS
NOPROB  JSR     ADD8
        CLR     $56     CLEAR LOW BATTERY FLAG
        RTS
READ91  LDA     #$50    CONFIGURATION DATA FOR SPCR
        STA     $0A     LOAD CONFIGURATION DATA
        LDA     $50
        BCLR    2,$02   BIT 0 PORT C GOES LOW (CS GOES LOW)
        STA     $0C     LOAD D_IN INTO SPI DATA REG. START TRANSFER.
BACK91  TST     $08     TEST STATUS OF SPIF
        BPL     BACK91  LOOP TO PREVIOUS INSTRUCTION IF NOT DONE
        LDA     $0C     LOAD CONTENTS OF SPI DATA REG. INTO ACC
        STA     $0C     START NEXT CYCLE
        AND     #$03    CLEAR 6 MSBs OF FIRST D_OUT
        STA     $61     STORE MSBs IN $61
BACK92  TST     $08     TEST STATUS OF SPIF
        BPL     BACK92  LOOP TO PREVIOUS INSTRUCTION IF NOT DONE
        BSET    2,$02   SET BIT 0 PORT C (CS GOES HIGH)
        LDA     $0C     LOAD CONTENTS OF SPI DATA INTO ACC
        STA     $62     STORE LSBs IN $62
        RTS

SUBTRCT LDA     $62     LOAD LSBs
        SUB     $55     SUBTRACT LSBs
        STA     $62     STORE REMAINDER
        LDA     $61     LOAD MSBs
        SBC     $54     SUBTRACT W/CARRY MSBs
        STA     $61     STORE REMAINDER
        RTS
ADD8    LDA     $62     LOAD LSBs
        ADD     $55     ADD LSBs
        STA     $62     STORE SUM
        LDA     $61     LOAD MSBs
        ADC     $54     ADD W/CARRY MSBs
        STA     $61     STORE SUM
        RTS
TB4MULT CLR     $68
        CLR     $69
        CLR     $6A
        CLR     $6B
        STX     $56     STORE CONTENTS OF X IN $56
        LSL     $62     MULTIPLY LSBs BY 2
        ROL     $61     MULTIPLY MSBs BY 2
        LDA     $62     LOAD LSBs OF LTC1091 INTO ACC
        LDX     $55     LOAD LSBs OF M INTO X
        MUL             MULTIPLY LSBs
        STA     $68     STORE LSBs IN $68
        STX     $6A     STORE IN $6A
        LDA     $62     LOAD LSBs OF LTC1091 INTO ACC
        LDX     $54     LOAD MSBs OF M INTO X
        MUL
        ADD     $6A     ADD NEXT BYTE
        STA     $6A     STORE BYTE
        TXA             TRANSFER X TO ACC
        ADC     $69     ADD NEXT BYTE
        STA     $69     STORE BYTE
        LDA     $61     LOAD MSBs OF LTC1091 INTO ACC
        LDX     $55     LOAD LSBs OF M INTO X
        MUL
        ADD     $6A     ADD NEXT BYTE
        STA     $6A     STORE BYTE
        TXA             TRANSFER X TO ACC
        ADC     $69     ADD NEXT BYTE
        STA     $69     STORE BYTE
        LDA     $61     LOAD MSBs OF LTC1091 INTO ACC
        LDX     $54     LOAD MSBs OF M INTO X
        MUL
        ADD     $69     ADD NEXT BYTE
        STA     $69     STORE BYTE
        TXA             TRANSFER X TO ACC
        ADC     $68     ADD NEXT BYTE
        STA     $68     STORE BYTE
        LDA     $6A     LOAD CONTENTS OF $6A INTO ACC
        BPL     NNN
        LDA     $69     LOAD CONTENTS OF $69 INTO ACC
        ADD     #$01    ADD 1 TO ACC
        STA     $69     STORE IN $69
        LDA     $68     LOAD CONTENTS OF $68 INTO ACC
        ADC     #$00    FLOW THROUGH CARRY
        STA     $68     STORE IN $68
NNN     LDA     $68     LOAD CONTENTS OF $68 INTO ACC
        STA     $61     STORE MSBs IN $61
        LDA     $69     LOAD CONTENTS OF $69 INTO ACC
        STA     $62     STORE IN $62
        LDX     $56     RESTORE X REGISTER
        RTS             RETURN
HOUSEKP BSET    0,$02   SET B0 PORT C
        BSET    2,$02   SET B2 PORT C
        RTS
```

Figure 24. Code for Processor Based Linearization

APPENDIX A

Error Sources in Thermocouple Systems

Obtaining good accuracy in thermocouple systems mandates care. The small thermocouple signal voltages require careful consideration to avoid error terms when signal processing. In general, thermocouple *system* accuracy better than 0.5°C is difficult to achieve. Major error sources include connection wires, cold junction uncertainties, amplifier error and sensor placement.

Connecting wires between the thermocouple and conditioning circuitry introduce undesired junctions. These junctions form unintended thermocouples. The number of junctions and their effects should be minimized, and kept isothermal. A variety of connecting wires and accessories are available from manufacturers and their literature *should be consulted (reference 4).*

Thermocouple voltages are generated whenever dissimilar materials are joined. This includes the leads of IC packages, which may be kovar in TO-5 cans, alloy 42 or copper in dual-in-line packages, and a variety of other materials in plating finishes and solders. The net effect of these thermocouples is "zero" if all are at exactly the same temperature, but temperature gradients exist within IC packages and across PC boards whenever power is dissipated. For this reason, extreme care must be used to ensure that no temperature gradients exist in the vicinity of the thermocouple terminations, the cold junction compensator (e.g., LT1025) or the thermocouple amplifier. If a gradient cannot be eliminated, leads should be positioned isothermally, especially the LT1025 R⁻ and appropriate output pins, the amplifier input pins, and the gain setting resistor leads. An effect to watch for is amplifier offset voltage warm-up drift caused by mismatched thermocouple materials in the wire-bond/lead system of the IC package. This effect can be as high as tens of microvolts in TO-5 cans with kovar leads. It has nothing to do with the actual offset drift specification of the amplifier and can occur in amplifiers with measured "zero" drift. Warm-up drift is directly proportional to amplifier power dissipation. It can be minimized by avoiding TO-5 cans, using low supply current amplifiers, and by using the lowest possible supply voltages. *Finally, it can be accommodated by calibrating* and specifying the system after a five minute warm-up period.

A significant error source is the cold junction. The error takes two forms. The subtractive voltage produced by the cold junction must be correct. In a true cold junction (ice point reference) this voltage will vary with inability to maintain the desired temperature, introducing error. In a cold junction compensator like the LT1025, error occurs with inability to sense and track ambient temperature. Minimizing sensing error is the manufacturer's responsibility (we do our best!), but tracking requires user care. Every effort should be made to keep the LT1025 isothermal with the cold junction. Thermal shrouds, high thermal capacity blocks and other methods are commonly employed to ensure that the cold junction and the compensator are at the same temperature.

Amplifier offset uncertainties and, to a lesser degree, bias currents and open loop gain should be considered. Amplifier selection criteria is discussed in the text under "Amplifier Selection."

A final source of error is thermocouple placement. Remember that the thermocouple measures its own temperature. In flowing or fluid systems, remarkably large errors can be generated due to effects of laminar flow or eddy currents around the thermocouple. Even a "simple" surface measurement can be wildly inaccurate due to thermal conductivity problems. Silicone thermal grease can reduce this, but attention to sensor mounting is usually required. As much of the sensor surface as possible should be mated to the measured surface. Ideally, the sensor *should be tightly mounted in a drilled recess in the* surface. Keep in mind that the thermocouple leads act as heat pipes, providing a direct thermal path to the sensor. With high thermal capacity surfaces this may not be a problem, but other situations may require some thought. Often, thermally mating the lead wire to the surface or coiling the wire in the environment of interest will minimize heat piping effects.

As a general rule, skepticism is warranted, even in the most "obviously simple" situations. Experiment with several sensor positions and mounting options. If measured results agree, you're probably on the right track. If not, rethink and try again.

New Developments in RS232 Interfaces

Robert Dobkin

New RS232 interface chips have been developed that offer significant advantages over older devices such as the 1488 and 1489. The new RS232 interface ICs improve speed, power, voltage supply requirements, and protection over older devices. Further, the new chips are easier to use, requiring fewer external components and may be turned off to a "zero" power supply current condition for use in battery powered systems.

The new RS232 drivers are implemented in a monolithic bipolar technology. A unique output stage was designed that provides large output swings, minimizing power supply voltage requirements, while retaining outstanding overload protection features. The outputs can be driven beyond the power supply voltage without drawing excessive current or forcing current back into the power supplies. Of course, current limiting is included to protect against short circuit conditions.

Initial consideration of technologies for implementing RS232 interfacing might include CMOS as a possible technology for this type of application. Power supply requirements are low, output voltage swing is high, and higher voltage CMOS technologies are available to allow operation up to ± 15V. Consideration of some of the problems associated with CMOS decreases its attractiveness for RS232 drivers.

Inherent in the CMOS structure, are diodes between the drain and source of the CMOS devices and the power supplies as is shown in Figure 1. A requirement of RS232 interfaces is the ability to withstand voltage applied to the output pins. With a CMOS output stage this is achieved with the inclusion of a 300Ω resistor in series with the output. (The resistor is similar to the resistors included in older drivers.) It protects the interface chip, but still allows damage to other devices powered *by the same supply.*

A problem occurs when the output of a driver which is powered from the 5V logic supply is connected to an external 12V or 15V source as is allowed by the RS232 specification. External current flows through the 300Ω limiting resistor, through the diodes, which are a part of the CMOS structure, and into the power supply. This forces the power supply to 12V or 15V damaging the 5V logic that is connected to the supplies. This problem can even cause latchup if the logic supply is off when external RS232 signals feed voltage into *the supply. This problem did not usually exist in the past,* because the RS232 interfaces were powered by separate ± 12V supplies

ESD damage is probably the most frequent cause of failure of interface chips. Bipolar devices are relatively rugged but still can be damaged by ESD. System requirements for ESD may be as high as 20kV. No IC can withstand that much voltage without external protection.

A requirement of the RS232 specification is the ability to withstand ± 25V input signals. *The CMOS LTC1045 which is* used as an RS232 receiver has been designed to operate with external resistors in series with the input. These resistors allow very large voltage swings at the input pins and provide ESD protection to the IC. Using on-chip resistors precludes the use of the optimum ESD protection structures, so CMOS devices may be more sensitive to ESD destruction at their inputs.

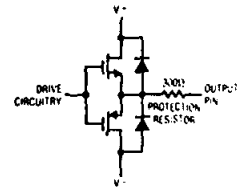


Figure 1. CMOS Line Driver Showing Parasitic Diodes to the Power Supplies

The output stage of the bipolar drivers is shown in Figure 2. Opposed collector NPN and PNP transistors give the widest possible output swings. The PNP transistor will swing to within 200mV of the positive supply while the NPN transistor with its associated Schottky diode will swing within about 900mV of the negative supply. If the output voltage is forced above the positive supply the emitter base junction of the PNP transistor reverse biases, and no current flows into the supply. The device is unaffected by external voltage up to the breakdown voltage of the transistor. If the output is forced below the negative supply, the Schottky diode reverse biases and prevents external current flow into the chip. Capacitor C1 is used to control the output slew rate so that no frequency compensation components are required to meet the RS232 specification of 4V/μs to 30V/μs.

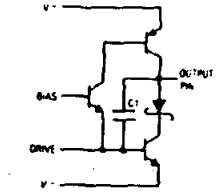


Figure 2. New Bipolar Driver Output Stage

Typically the slew rate of these drivers is about 8–10V/μs. *This* allows them to be used successfully up to about 64k baud. The output slew rate of the bipolar drivers is well controlled by an internal capacitor and relatively independent of load resistance or capacitance. The bipolar receiver is relatively straightforward utilizing a level detector with hysteresis to set the trip point. Nominally the trip point is set at about 1.5V with 200mV of hysteresis. The receivers go into a high output state with an open input. The receivers outputs are both TTL and CMOS compatible.

For an application with a 12-bit A/D converter with a 10V full scale to a 1/2LSB error maximum:

$$F_{max} = \frac{2^{-(12+1)}}{\pi\,(0.5\times10^{-6})} = 77.7\text{kHz}$$

Track-to-hold offset is caused by the transfer of charge to the holding capacitor via the gate capacitance of the switch when switching into hold. Since the gate capacitance couples the switch-control voltage applied to the gate on to the hold capacitor, the resulting track-to-hold offset is a function of the logic level applied to the gate and the change in the gate capacitance over temperature.

HOLD MODE

In the hold mode there are two important specifications that must be considered; feedthrough and the droop rate. Feedthrough errors appear as an attenuated version of the input at the output while in the hold mode. Hold-Mode feedthrough varies with frequency, increasing at higher frequencies. Feedthrough is an important specification when a track and hold follows an analog multiplexer that switches among many different channels.

Hold-mode droop rate is the change in output voltage per unit of time while in the hold mode. Hold mode droop originates as leakage from the hold capacitor, of which the major leakage current contributors are switch leakage current and bias current. The rate of voltage change on the capacitor dV/dt is the ratio of the total leakage current I_L to the hold capacitance C_H.

$$\text{Droop Rate} = \frac{dV_{OUT}}{dt}\,(\text{Volts/Sec}) = \frac{I_L(\text{pA})}{C_H(\text{pF})}$$

For the AD365 in particular;

$$\text{Droop Rate} = \frac{100\text{pA}}{100\text{pF}} = 1\text{V/sec maximum}$$

Additionally the leakage current doubles for every 10°C increase in temperature above 25°C; therefore, the hold-mode droop rate characteristic will also double in the same fashion.

Since a track and hold is used typically in combination with an A/D converter, then the total droop in the output voltage has to be less than 1/2LSB during the period of a conversion. The maximum allowable signal change on the input of an A/D converter is:

$$\Delta V \text{ max} = \frac{\text{Full Scale Voltage}}{2^{(N+1)}}$$

Once the maximum ΔV is determined then the conversion time of the A/D converter (t_{CONV}) is required to calculate the maximum allowable dV/dt:

$$\frac{dV \text{ max}}{dt} = \text{max}$$

The maximum $\frac{dV \text{ max}}{dt}$ the previous equation is the limit not only at 25°C but at maximum expected operating temperature range. Therefore, over the operating temperature range the following criteria must be met ($T_{OPERATION} - 25°C$) = ΔT.

$$\frac{dV\ 25°C}{dt} \times 2^{\frac{\Delta T°C}{10°C}} \le \frac{dV \text{ max}}{dt}$$

HOLD-TO-TRACK TRANSITION

The Nyquist theorem states that a band-lim signal which is sampled at a rate at least twice the maxim al frequency can be reconstructed without loss of inform This means that a sampled data system must sample, convert and acquire the next point at a rate at least twice the signal frequency. Thus the maximum input frequency is equal to

$$f_{MAX} = \frac{1}{2(T_{ACQ} + T_{CONV} + T_{AP})}$$

Where T_{ACQ} is the acquisition time of the sample-to-hold amplifier, T_{AP} is the maximum aperture time (small enough to be ignored) and T_{CONV} is the conversion time of the A/D converter.

DATA ACQUISITION SYSTEMS

The fast acquisition time of the AD365 when used with a high speed A/D converter allows accurate digitization of high frequency signals and high throughput rates in multichannel data acquisition systems. The AD365 can be used with a number of different A/D converters to achieve high throughput rates. Figures 23 and 24 show the use of an AD365 with the AD578 and AD574A.

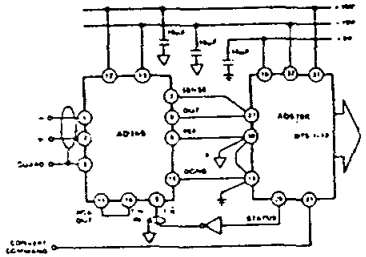


Figure 23. A D Conversion System, 117.6kHz Throughput 53.8kHz Max Signal Input

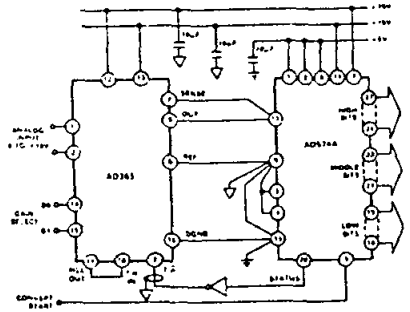


Figure 24. 12-Bit A D Conversion System, 26.3kHz Throughput Rate, 13.1kHz Max Signal Input

ANALOG DEVICES

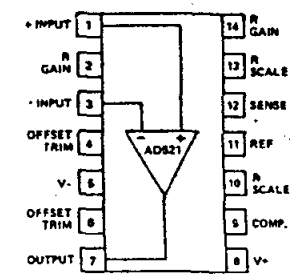
Integrated Circuit Precision Instrumentation Amplifier

AD521

FEATURES

- Programmable Gains from 0.1 to 1000
- Differential Inputs
- High CMRR: 110dB min
- Low Drift: 2μV/°C max (L)
- Complete Input Protection, Power ON and Power OFF
- Functionally Complete with the Addition of Two Resistors
- Internally Compensated
- Gain Bandwidth Product: 40MHz
- Output Current Limited: 25mA
- Very Low Noise: 0.5μV p-p, 0.1Hz to 10Hz, RTI @ G = 1000
- Chips are Available

AD521 PIN CONFIGURATION



PRODUCT DESCRIPTION

The AD521 is a second generation, low cost, monolithic IC instrumentation amplifier developed by Analog Devices. As a true instrumentation amplifier, the AD521 is a gain block with differential inputs and an accurately programmable input/output gain relationship.

The AD521 IC instrumentation amplifier should not be confused with an operational amplifier, although several manufacturers (including Analog Devices) offer op amps which can be used as building blocks in variable gain instrumentation amplifier circuits. Op amps are general-purpose components which, when used with precision-matched external resistors, can perform the instrumentation amplifier function.

An instrumentation amplifier is a precision differential voltage gain device optimized for operation in a real world environment, and is intended to be used wherever acquisition of a useful signal is difficult. It is characterized by high input impedance, balanced differential inputs, low bias currents and high CMR.

As a complete instrumentation amplifier, the AD521 requires only two resistors to set its gain to any value between 0.1 and 1000. The ratio matching of these resistors does not affect the high CMRR (up to 120dB) or the high input impedance ($3 \times 10^9\,\Omega$) of the AD521. Furthermore, unlike most operational amplifier-based instrumentation amplifiers, the inputs are protected against overvoltages up to ±15 volts beyond the supplies.

The AD521 IC instrumentation amplifier is available in four different versions of accuracy and operating temperature range. The economical "J" grade, the low drift "K" grade, and the lower drift, higher linearity "L" grade are specified from 0 to +70°C. The "S" grade guarantees performance to specification over the extended temperature range: -55°C to +125°C.

PRODUCT HIGHLIGHTS

1. The AD521 is a true instrumentation amplifier in integrated circuit form, offering the user performance comparable to many modular instrumentation amplifiers at a fraction of the cost.
2. The AD521 has low guaranteed input offset voltage drift (2μV/°C for L grade) and low noise for precision, high gain applications.
3. The AD521 is functionally complete with the addition of two resistors. Gain can be preset from 0.1 to more than 1000.
4. The AD521 is fully protected for input levels up to 15V beyond the supply voltages and 30V differential at the inputs.
5. Internally compensated for all gains, the AD521 also offers the user the provision for limiting bandwidth.
6. Offset nulling can be achieved with an optional trim pot.
7. The AD521 offers superior dynamic performance with a gain-bandwidth product of 40MHz, full peak response of 100kHz (independent of gain) and a settling time of 5μs to 0.1% of a 10V step.

SPECIFICATIONS (typical @ V_S = ±15V, R_L = 2kΩ and T_A = 25°C unless otherwise specified)

MODEL	AD521JD	AD521KD	AD521LD	AD521SD (AD521S0/883B)
GAIN				
Range (For Specified Operation, Note 1)	1 to 1000	•	•	•
Equation	$G = R_S/R_G$ V/V	•	•	•
Error from Equation	(0.25 + 0.004G)%	•	•	•
Nonlinearity (Note 2)				
1≤G≤1000	0.1% max	•	0.1% max	•
Gain Temperature Coefficient	typ 20.85G ppm/°C	•	•	typ 40.4G ppm/°C
OUTPUT CHARACTERISTICS				
Rated Output	±10V, 10mA min	•	•	•
Output at Maximum Operating Temperature	±10V @ 5mA min	•	•	•
Impedance	0.1Ω	•	•	•
DYNAMIC RESPONSE				
Small Signal Bandwidth (±3dB)				
G = 1	> 2MHz	•	•	•
G = 10	800kHz	•	•	•
G = 100	200kHz	•	•	•
G = 1000	40kHz	•	•	•
Small Signal, ±1.0% Flatness				
G = 1	75kHz	•	•	•
G = 10	24kHz	•	•	•
G = 100	24kHz	•	•	•
G = 1000	4kHz	•	•	•
Full Peak Response (Note 3)	100kHz	•	•	•
Slew Rate, 1≤G≤1000	10V/µs	•	•	•
Settling Time (any 10V step to within 10mV of Final Value)				
G = 1	7µs	•	•	•
G = 10	5µs	•	•	•
G = 100	10µs	•	•	•
G = 1000	55µs	•	•	•
Differential Overload Recovery (±30V input to within 10mV of Final Value) (Note 4)				
G = 1000	50µs	•	•	•
Common Mode Step Recovery (30V Input to within 10mV of Final Value) (Note 5)				
G = 1000	10µs	•	•	•
VOLTAGE OFFSET (may be nulled)				
Input Offset Voltage (V_{OS_I})	3mV max (2mV typ)	1.5mV max (0.5mV typ)	1.0mV max (0.5mV typ)	**
vs. Temperature	15µV/°C max (2µV/°C typ)	5µV/°C max (1.5µV/°C typ)	2µV/°C max	**
vs. Supply	3µV/%	•	•	•
Output Offset Voltage (V_{OS_O})	400mV max (200mV typ)	200mV max (30mV typ)	100mV max	**
vs. Temperature	400µV/°C max (150µV/°C typ)	150µV/°C max (50µV/°C typ)	75µV/°C max	**
vs. Supply (Note 6)	0.005%/%	•	•	•
INPUT CURRENTS				
Input Bias Current (either input)	80nA max	40nA max	**	**
vs. Temperature	1nA/°C max	500pA/°C max	**	**
vs. Supply	2%/V	•	•	•
Input Offset Current	20nA max	10nA max	**	**
vs. Temperature	250pA/°C max	125pA/°C max	**	**
INPUT				
Differential Input Impedance (Note 7)	3×10^9 Ω‖1.8pF	•	•	•
Common Mode Input Impedance (Note 8)	6×10^{11} Ω‖3.0pF	•	•	•
Input Voltage Range for Specified Performance (with respect to ground)	±10V	•	•	•
Maximum Voltage without Damage to Unit, Power ON or OFF Differential Mode (Note 9)	30V	•	•	•
Voltage at either input (Note 9)	V_S ±15V	•	•	•
Common Mode Rejection Ratio, DC to 60Hz with 1kΩ source unbalance				
G = 1	70dB min (74dB typ)	74dB min (80dB typ)	**	**
G = 10	90dB min (94dB typ)	94dB min (100dB typ)	**	**
G = 100	100dB min (104dB typ)	104dB min (110dB typ)	**	**
G = 1000	100dB min (110dB typ)	110dB min (120dB typ)	**	**
NOISE				
Voltage RTO (p-p) 0.1Hz to 10Hz (Note 10)	$\sqrt{(0.3G)^2 + (23)^2}$ µV	•	•	•
RMS RTO, 10Hz to 10kHz	$\sqrt{(1.2G)^2 + (15nV)^2}$ µV	•	•	•
Input Current, rms, 0.01Hz to 10kHz	15pA (rms)	•	•	•
REFERENCE TERMINAL				
Bias Current	3µA	•	•	•
Input Resistance	10kΩ	•	•	•
Voltage Range	±10V	•	•	•
Gain to Output	1	•	•	•
POWER SUPPLY				
Operating Voltage Range	±5V to ±18V	•	•	•
Quiescent Supply Current	3mA max	•	•	•
TEMPERATURE RANGE				
Specified Performance	0 to +70°C	•	•	-55°C to +125°C
Operating	-25°C to +85°C	•	•	-55°C to +125°C
Storage	-65°C to +150°C	•	•	•
PACKAGE OPTION[1]				
Ceramic (D-14)	AD521JD	AD521KD	AD521LD	AD521SD

NOTES
[1] See Section 16 for package outline information.
*Specifications same as AD521JD.
**Specifications same as AD521KD.
Specifications subject to change without notice.

Applying the AD521

NOTES:

1. Gains below 1 and above 1000 are realized by simply adjusting the gain setting resistors. For best results, voltage at either input should be restricted to ±10V for gains equal to or less than 1.

2. Nonlinearity is defined as the ratio of the deviation from the "best straight line" through a full scale output range of ±9 volts. With a combination of high gain and ±10 volt output swing, distortion may increase to as much as 0.3%.

3. Full Peak Response is the frequency below which a typical amplifier will produce full output swing.

4. Differential Overload Recovery is the time it takes the amplifier to recover from a pulsed 30V differential input with 15V of common mode voltage, to within 10mV of final value. The test input is a 30V, 10µs pulse at a 1kHz rate. (When a differential signal of greater than 11V is applied between the inputs, transistor clamps are activated which drop the excess input voltage across internal input resistors. If a continuous overload is maintained, power dissipated in these resistors causes temperature gradients and a corresponding change in offset voltage, as well as added thermal time constant, but will not damage the device.)

5. Common Mode Step Recovery is the time it takes the amplifier to recover from a 30V common mode input with zero volts of differential signal to within 10mV of final value. The test input is 30V, 10µs pulse at a 1kHz rate. (When a common mode signal greater than V_S -0.5V is applied to the inputs, transistor clamps are activated which drop the excessive input voltage across internal input resistors. Power dissipated in these resistors causes temperature gradients and a corresponding change in offset voltage, as well as an added thermal time constant, but will not damage the device.)

6. Output Offset Voltage versus Power Supply Change is a constant 0.005 times the unnulled output offset per percent change in either power supply. If the output offset is nulled, the output offset change versus supply change is substantially reduced.

7. Differential Input Impedance is the impedance between the two inputs.

8. Common Mode Input Impedance is the impedance from *either* input to the power supplies.

9. Maximum Input Voltage (differential or at either input) is 30V when using ±15V supplies. A more general specification is that neither input may exceed either supply (even when V_S = 0) by more than 15V and that the difference between the two inputs must not exceed 30V. (See also Notes 4 and 5.)

10. 0.1Hz to 10Hz Peak-to-Peak Voltage Noise is defined as the maximum peak-to-peak voltage noise observed during 3 seperate 10 second periods with the test circuit of Figure 8.

DESIGN PRINCIPLE

Figure 1 is a simplified schematic of the AD521. A differential input voltage, V_{IN}, appears across R_G causing an imbalance in the currents through Q_1 and Q_2, $\Delta I = V_{IN}/R_G$. That imbalance is forced to flow in R_S because the collector currents of Q_3 and Q_4 are constrained to be equal by their biasing (current mirror). These conditions can only be satisfied if the differential voltage across R_S (and hence the output voltage of the AD521) is equal to $\Delta I \times R_S$. The feedback amplifier, A_{FB} performs that function. Therefore, $V_{OUT} = \frac{V_{IN}}{R_G} \times R_S$ or $\frac{V_{OUT}}{V_{IN}} = \frac{R_S}{R_G}$.

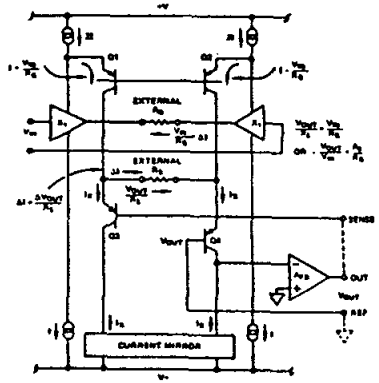


Figure 1. Simplified AD521 Schematic

Use the LM158/LM258/LM358 Dual, Single Supply Op Amp

National Semiconductor
Application Note 116
Jim Sherwin

INTRODUCTION

Use the LM158/LM258/LM358 dual op amp with a single supply in place of the LM1458/LM1558 with split supply and reap the profits in terms of:

a. Input and output voltage range down to the negative (ground) rail
b. Single supply operation
c. Lower standby power dissipation
d. Higher output voltage swing
e. Lower input offset current
f. Generally similar performance otherwise

The main advantage, of course, is that you can eliminate the negative supply in many applications and still retain equivalent op amp performance. Additionally, and in some cases more importantly, the input and output levels are permitted to swing down to ground (negative rail) potential. Table I shows the relative performance of the two in terms of guaranteed and/or typical specifications.

In many applications the LM158/LM258/LM358 can also be used directly in place of LM1558 for split supply operation.

SINGLE SUPPLY OPERATION

The LM1458/LM1558 or similar op amps exhibit several important limitations when operated from a single positive (or negative) supply. Chief among these is that input and output signal swing is severely limited for a given supply as shown in *Figure 1*. For linear operation, the input voltage must not reach within 3 volts of ground or of the supply, and output range is similarly limited to within 3–5 volts of ground or supply. This means that operation with a +12V supply could be limited as low as 2 Vp-p output swing. The LM358 however, allows a 10.5 Vp-p output swing for the same 12V supply. Admittedly these are worst case specification limits, but they serve to illustrate the problem.

TABLE I. Comparison of Dual Op Amps LM1458 and LM358

Characteristic	LM1458	LM358
V_{IO}	8 mV Max	7 mV Max
CM V_I	24 Vp-p*	0–28.5V*
I_{IO}	200 nA	50 nA
I_{OB}	500 nA	−500 nA
CMRR	60 dB Min @ 100 Hz 90 dB Typ	85 dB Typ @ DC
$\bar{e}_n$ @ 1 kHz, R_{GEN} 10 kΩ	45 nV/√Hz Typ	40 nV/√Hz Typ**
Z_{IN}	200 MΩ Typ	Typ 100 MΩ
A_{VOL}	20k Min 100k Typ	100k Typ
I_C	1.1 MHz Typ	1 MHz Typ**
P_{BW}	14 kHz Typ	11 kHz Typ**
dV_o/dt	0.6V/μs Typ	0.5V/μs Typ**
V_o @ R_L = 10k/2k	24/20 Vp-p*	28.5 Vp-p
I_{SC}	20 mA Typ	Source 20 mA Min (40 Typ) Sink 10 mA Min (20 Typ)
PSRR @ DC	37 dB Min 90 dB Typ	100 dB Typ
I_D (R_L = ∞)	8 mA Max	2 mA Max

†From laboratory measurement
*Based on V_S = 30V on LM358 only, or V_S = ±15V
**From data sheet typical curves

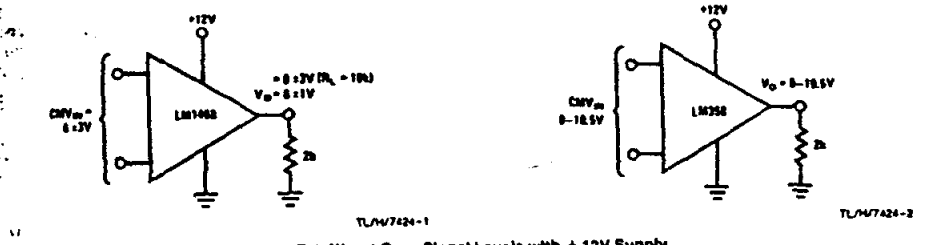


FIGURE 1. Worst Case Signal Levels with + 12V Supply

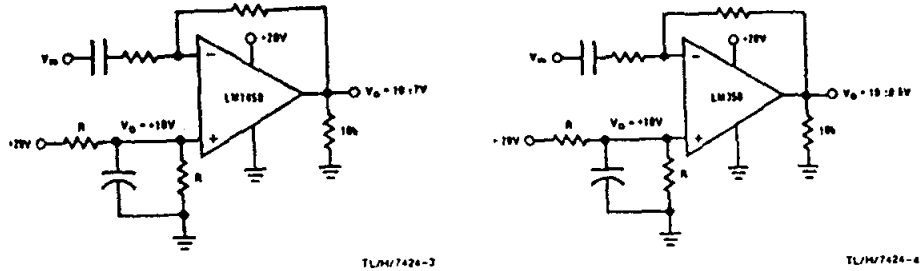


FIGURE 2. Operating with AC Signals

AC GAIN

For AC signals the input can be capacitor coupled. The input common mode and quiescent output voltages are fixed at one-half the supply voltage by a resistive divider at the non-inverting input as shown in *Figure 2*. This quiescent output could be set at a lower voltage to minimize power dissipation in the LM358, if desired, so long as $V_Q \geq V_{IN}$ pk. For the LM1458 the quiescent output must be higher, $V_Q \geq 3V + V_{IN}$ pk thus, for small signals, power dissipation is much greater with the LM1458. Example: Required $V_O = V_Q \pm 1V$ pk into 2k, V_{SUPPLY} = as required. Find quiescent dissipation in load and amplifier for LM1458 and LM358.

LM358	LM1458
V_Q = + 1V	V_Q = 4V
V_{SUPPLY} = + 3.5V	V_{SUPPLY} = 8V
$P_{LOAD} = \frac{E_L^2}{R_L} = \frac{1}{2k} = 0.5$ mW	$P_{LOAD} = \frac{4^2}{2k} = 8$ mW
$P_D = V_S I_S + (V_S - V_Q) I_L$	$P_D = P_{\bar{d}} + (V_S - V_Q)\, I_L$
$= 3.5V \times 0.7$ mA + $(3.5-1)\frac{1V}{2k}$	$= 22$ mW + $(8-4)\frac{4V}{2k}$
$P_D = 2.45 + 1.25 = 3.7$ mW	$P_D = 22 + 8 = 30$ mW
$P_{TOTAL} = 3.7 + 0.5 = 4.2$ mW	$P_{TOTAL} = 30 + 8 = 38$ mW
*From typical characteristics	*From typical characteristics

The LM1458 requires over twice the supply voltage and nearly 10 times the supply power of the LM358 in this application.

INVERTING DC GAIN

Connections and biasing for DC inverting gain are essentially the same as for the AC coupled case. Note, of course, that the output cannot swing negative when operated from a single positive supply. *Figure 3* shows the connections and signal limitations.

NON-INVERTING DC GAIN

The non-inverting gain connection does not require the V_Q biasing as before; the inverting input can be returned to ground in the usual manner for gains greater than unity, (see *Figure 4*). A tremendous advantage of the LM358 in this connection is that input signals and output may extend all the way to ground; therefore DC signals in the low-millivolt range can be handled. The LM1458 still requires that V_{IN} = 3–17V. Therefore maximum gain is limited to $A_V = (V_O - 3)/3$, or A_V max = 5.4 for a 20V supply.

There is no similar limitation for the LM358.

ZERO V.C. INPUT BIAS CURRENT

An interesting and unusual characteristic is that I_{IN} has a zero temperature coefficient. This means that matched resistance is not required at the input, allowing omission of one resistor per op amp from the circuit in most cases.

BALANCED SUPPLY OPERATION

The LM358 will operate satisfactorily in balanced supply operation so long as a load is maintained from output to the negative supply.

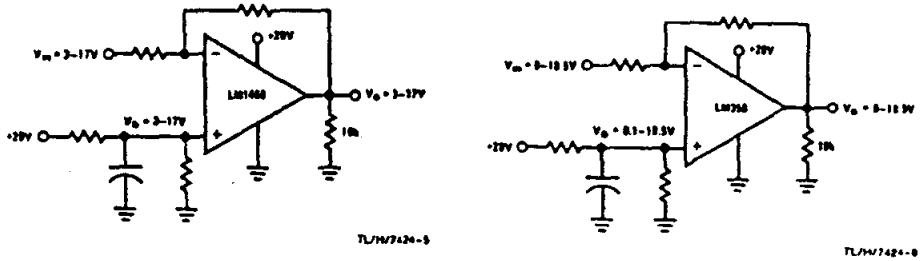


FIGURE 3. Typical DC Coupled Inverting Gain

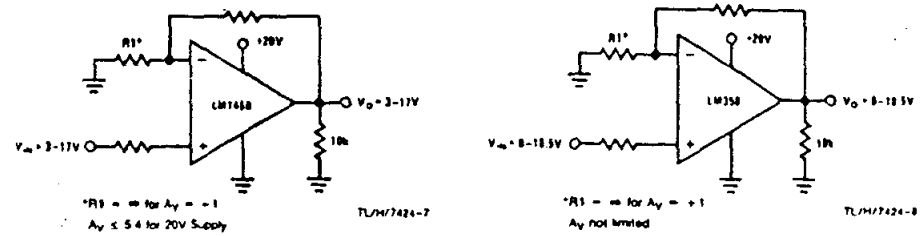


FIGURE 4. Typical DC Coupled Non-Inverting Gain

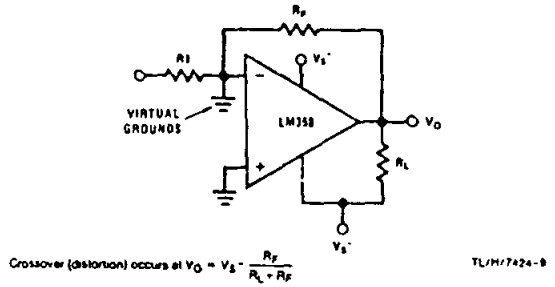


FIGURE 5. Split Supply Operation of LM358

The output load to negative supply forces the amplifier to source some minimum current at all times, thus eliminating crossover distortion. Crossover distortion without this load would be more severe than that expected with the normal op amp. Since the single supply design took notice of this normal load connection to ground, a class AB output stage was not included. Where ground referenced feedback resistors are used as in *Figure 5*, the required load to the negative supply depends upon the peak negative output signal level desired without exhibiting crossover distortion. R_L to the negative rail should be chosen small enough that the voltage divider formed by R_F and R_L will permit V_O to swing negative to the desired point according to the equation:

$$R_L = R_F \frac{V_S - V_O}{V_O}.$$

R_L could also be returned to the positive supply with the advantage that V_O max would never exceed (V_S^+ − 1.5V). Then with ±15V supplies $R_{L\ MIN}$ would be 0.12 R_F. The disadvantage would be that the LM358 can source twice as much current as it can sink, therefore R_L to negative supply can be one-half the value of R_L to positive supply.

The need for single or split supply is based on system requirements which may be other than op amp oriented. However if the only need for balanced supplies is to simplify the biasing of op amps, there are many systems which can find a cost effective benefit in operating LM358's from single supplies rather than standard op amps from balanced supplies. Of the usual op amp circuits, Table II shows those few which have limited function with single supply operation. Most are based on the premise that to operate from a single supply, a reference V_O at about one-half the supply be available for bias or (zero) signal reference. The basic circuits are those listed in AN-20.

TABLE II. Conventional Op Amp Circuits Suitable for Single Supply Operation

Application	Limitations
AC Coupled amp‡	V_O*
Inverting amp	V_O
Non-inverting amp	OK*
Unity gain buffer	OK
Summing amp	V_O
Difference amp	V_O
Differentiator	V_O
Integrator	V_O
LP Filter	V_O
I-V Connector	V_O
PE Cell Amp	OK
I Source	$I_{O\ MIN} = \frac{1.5}{R1}$
I sink	OK
Volt Ref	OK
FW Rectifier	V_O or modified circuit
Sine wave osc	V_O
Triangle generator	V_O
Threshold detector	OK
Tracking, regulator PS	Not practical
Programmable PS	OK
Peak Detector	OK to $V_{IN} = 0$

‡See AN20 for conventional circuits

*V_O denotes need for a reference voltage, usually at about $\frac{V_S}{2}$

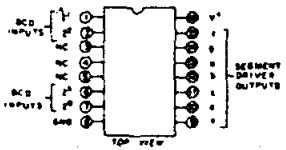
OK means no reference voltage required

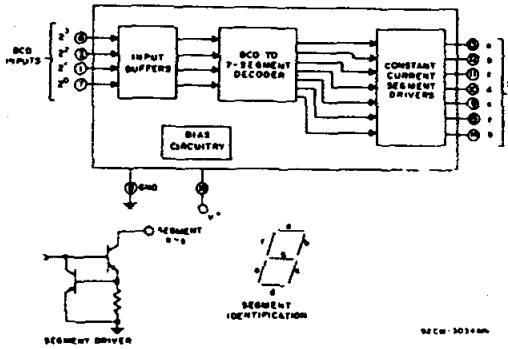
CA3161E
BCD-TO-SEVEN-SEGMENT DECODER/DRIVER

Features:

- *TTL-compatible input logic levels*
- *25-mA (typ.) constant-current segment outputs*
- *Eliminates need for output current-limiting resistors*
- *Pin compatible with other industry standard decoders*
- *Low standby power dissipation - 16 mW (typ.)*

PIN CONNECTION





Functional block diagram of the CA3151E

The RCA-CA3161E is a monolithic intergrated circuit that performs the BCD-to-seven-segment decoding function and features constant-current segment drivers. When used with the CA3162E A/D Converter* the CA3161E provides a complete digital readout system with a minimum number of external parts.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE (between terminals 1 and 10) ..... +7 V

INPUT VOLTAGE (terminals 1, 2, 6, 7) ..... +5.5 V

OUTPUT VOLTAGE

Output "Off" ..... +7 V

Output "On" (See note 1) ..... +10 V

DEVICE DISSIPATION

Up to T_A = +55°C ..... 1 W

Above T_A = +55°C ..... derate linearly at 10.5 mW/°C

AMBIENT TEMPERATURE RANGE

Operating ..... 0 to +75°C

Storage ..... −65 to +150°C

LEAD TEMPERATURE (DURING SOLDERING)

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max. ..... +265°C

NOTE 1: This is the maximum output voltage for any single output. The output voltage must be consistent with the maximum dissipation and derating curve for worst-case conditions. Example: All segments "on", 100% duty cycle.

ELECTRICAL CHARACTERISTICS at T_A = 25°C

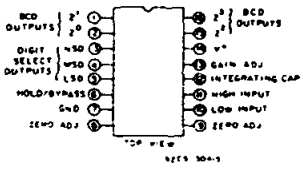
CHARACTERISTIC		LIMITS			UNITS
		Min.	Typ.	Max.	
Supply Voltage Operating Range, V^+		4.5	5	5.5	V
Supply Current, I^+ (all inputs high)		–	3.5	8	mA
Output Current Low (V_O = 2 V)		18	25	32	mA
Output Current High (V_O = 5.5 V)		–	–	250	µA
Input Voltage High (logic "1" level)		2	–	–	V
Input Voltage Low (logic "0" level)		–	–	0.8	V
Input Current High (logic "1")	2 V	−30	–	–	µA
Input Current Low (logic "0")	0 V	−40	–	–	µA
Propagation Delay Time	t_{PHL}	–	2.6	–	µs
	t_{PLH}	–	1.4	–	

CA3162
A/D CONVERTER FOR 3-DIGIT DISPLAY

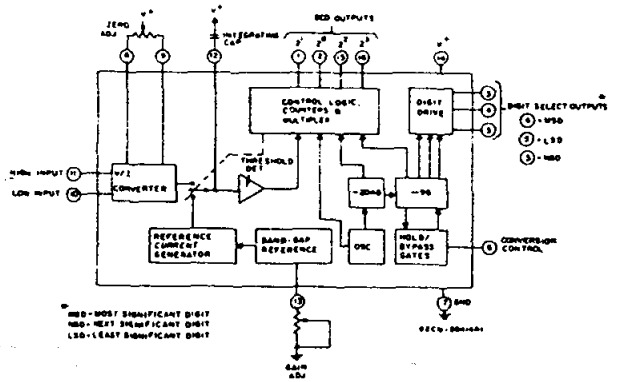
Features:

- *Dual-slope A/D conversion*
- *Multiplexed BCD display*
- *Ultra-stable internal band-gap voltage reference*
- *Capable of reading 99 mV below ground with single supply*
- *Differential input*
- *Internal timing - no external clock required*
- *Choice of low-speed (4-Hz) or high-speed (96-Hz) conversion rate*
- *"Hold" inhibits conversion but maintains delay*
- *Overrange indication - "EEE" for reading greater than + 999 mV, "-" for reading more negative than -99 mV when used with CA3161E BCD-to-Seven Segment Decoder/Driver*

PIN CONNECTION



The CA3162E is an I²L monolithic A/D converter that provides a 3-digit multiplexed BCD output. It is used with the CA3161E BCD-to-Seven-Segment Decoder/Driver* and a minimum of external parts to implement a complete 3-digit display.



Functional block diagram of the CA3162E

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE (between terminals 7 and 14) ..... + 7 V

INPUT VOLTAGE (terminal 10 or 11 to ground) ..... ± 15 V

DEVICE DISSIPATION:

Up to T_A = +55°C 750mW

Above T_A = +55°C ..... derate linearly at 7.9mW/°C

AMBIENT TEMPERATURE RANGE:

Operating ..... 0 to + 75°C

Storage ..... −65 to + 150°C

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max. ..... + 265°C

CA3162
A/D CONVERTER FOR 3-DIGIT DISPLAY

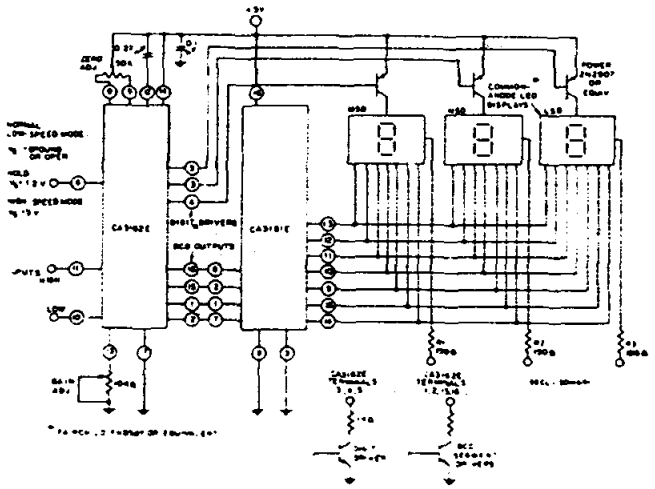


Fig. 2— Basic digital readout system using the CA3162E and the CA3161E.

Circuit Description

The functional block diagram of the CA3162E is shown in Fig. 1. The heart of the system is the V-I converter and reference current generator. The V-I converter converts the input voltage applied between terminals 10 and 11 to a current that charges the integrating capacitor on terminal 12 for a predetermined time interval. At the end of the charging interval, the V-I converter is disconnected from the integrating capacitor, and a band-gap reference constant-current source of opposite polarity is connected. The number of clock counts that elapse before the charge is restored to its original value is a direct measure of the signal induced current. The restoration is sensed by the comparator, which in turn latches the counter. The count is then multiplexed to the BCD outputs.

The timing for the CA3162E is supplied by a 786 Hz ring oscillator, and the input at terminal 6 determines the sampling rate. A 5-V input provides a high-speed sampling rate (196 Hz), and grounding or floating terminal 6 provides a low-speed (4 Hz) sampling rate. When terminal 6 is fixed at +1.2 V (by placing a 12 K resistor between terminal 6 and the +5 V supply) a "hold" feature is available. While the CA3162E is in the hold mode, sampling continues at 4 Hz but the display data are latched to the last reading prior to the application of the 1.2 V. Removal of the 1.2 V restores continuous display changes. Note, however, that the sampling rate remains at 4 Hz.

The "EEE" or "-EEE" displays indicate that the range of the system has been exceeded in the positive or negative direction, respectively. Negative voltages to −99 mV are displayed with the minus sign in the MSD. The BCD code is 1010 for a negative overrange (-EEE) and 1011 for a positive overrange (EEE).

TDA 1023
PROPORTIONAL-CONTROL TRIAC TRIGGERING CIRCUIT

GENERAL DESCRIPTION

The TDA1023 is a bipolar integrated circuit for controlling triacs in the time proportional or burst firing mode. It permits very precise temperatur control of heating equipment and is especially suited for the control of panel heaters. The circuit generates positive-going trigger pulses and complies with the regulations on radio interference and mains distortion.

Special features are:

- adjustable proportional range width
- adjustable hysteresis
- adjustable trigger pulse width
- adjustable firing burst repetition time
- control range translation facility
- failsafe operation
- supplied from the mains
- provides supply for external temperature bridge

Table 2. Timing capacitor C_T values.

effective d.c. value	marked a.c. specification	
μF	μF	V
68	47	25
47	33	40
33	22	25
22	15	40
15	10	25
10	6,8	40

QUICK REFERENCE DATA

Supply voltage (derived from mains voltage)	V_{CC}	typ.	13,7 V
Stabilized supply voltage for temperature bridge	V_Z*	typ.	8 V
Supply current (average value)	$I_{16(AV)}$	typ.	10 mA
Trigger pulse width	t_w	typ.	200 μs
Firing burst repetition time at C_T = 68 μF	T_b	typ.	41 s
Output current	$-I_{OH}$*	max.	150 mA
Operating ambient temperature range	T_{amb}	−20 to + 75	°C

* Negative current is defined as conventional current flow out of a device. A negative output current is suited for positive triac triggering.

Table 1. Adjustment of proportional range and hysteresis.
Combinations of resistor values giving hysteresis > ¼ proportional range.

proportional range mV	*proportional* range resistor R5 kΩ	*minimum* hysteresis mV	*maximum* hysteresis resistor R4 kΩ
80	open	20	open
160	3,3	40	9,1
240	1,1	60	4,3
320	0,43	80	2,7
400	0	100	1,8

MOTOROLA

SN54/74LS373
SN54/74LS374

OCTAL TRANSPARENT LATCH WITH 3-STATE OUTPUTS;

OCTAL D-TYPE FLIP-FLOP WITH 3-STATE OUTPUT

LOW POWER SCHOTTKY

DESCRIPTION — The SN54LS/74LS373 consists of eight latches with 3-state outputs for bus organized system applications. The flip-flops appear transparent to the data (data changes asynchronously) when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup times is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH the bus output is in the high impedence state.

The SN54LS/74LS374 is a high-speed, low-power Octal D-type Flip-Flop featuring separate D-type inputs for each flip-flop and 3-state outputs for bus oriented applications. A buffered Clock (CP) and Output Enable (OE) is common to all flip-flops. The SN54LS/74LS374 is manufactured using advanced Low Power Schottky technology and is compatible with all Motorola TTL families.

- EIGHT LATCHES IN A SINGLE PACKAGE
- 3-STATE OUTPUTS FOR BUS INTERFACING
- HYSTERESIS ON LATCH ENABLE
- EDGE-TRIGGERED D-TYPE INPUTS
- BUFFERED POSITIVE EDGE-TRIGGERED CLOCK
- HYSTERESIS ON CLOCK INPUT TO IMPROVE NOISE MARGIN
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS

PIN NAMES

		LOADING (Note a)	
		HIGH	LOW
D_0-D_7	Data Inputs	0.5 U.L.	0.25 U.L.
LE	Latch Enable (Active HIGH) Input	0.5 U.L.	0.25 U.L.
CP	Clock (Active HIGH going edge) Input	0.5 U.L.	0.25 U.L.
$\overline{OE}$	Output Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
O_0—O_7	Outputs (Note b)	65(25) U.L.	15 (7.5) U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 7.5 U.L. for Military and 25 U.L. for Commercial (74) Temperature Ranges. The Output HIGH drive factor is 25 U.L. for Military (54) and 65 U.L. for Commercial (74) Temperature Ranges.

TRUTH TABLE

LS373

Dn	LE	$\overline{OE}$	On
H	H	L	H
L	H	L	L
X	X	H	Z*

LS374

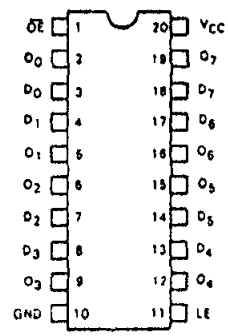
Dn	CP	$\overline{OE}$	On
H	⌐	L	H
L	⌐	L	L
X	X	H	Z*

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedence

*Note: Contents of flip-flops unaffected by the state of the Output Enable input ($\overline{OE}$)

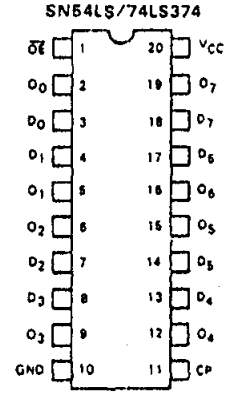
CONNECTION DIAGRAM
DIP (TOP VIEW)

SN54LS/74LS373



CONNECTION DIAGRAM
DIP (TOP VIEW)

SN54LS/74LS374

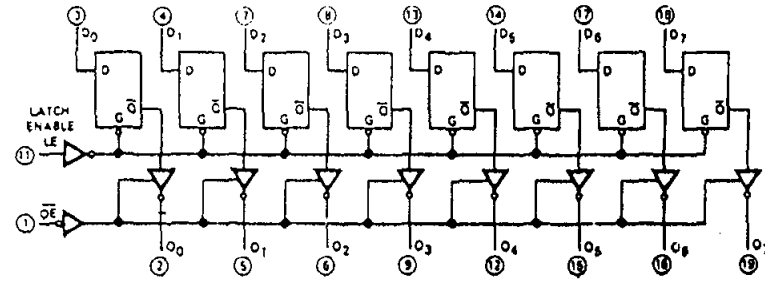


J Suffix — Case 732-03 (Ceramic)
N Suffix — Case 738-03 (Plastic)

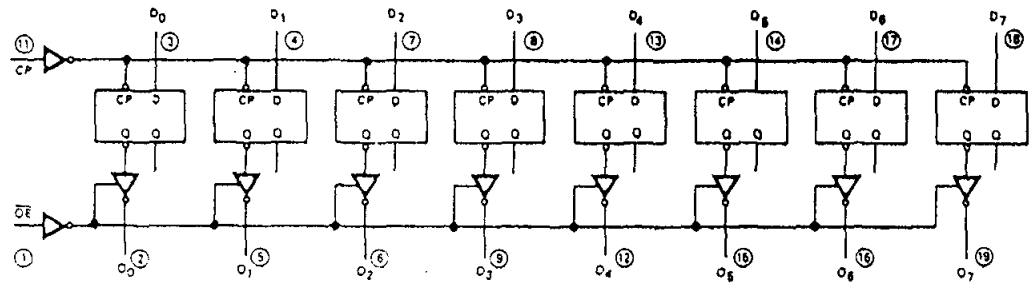
NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

LOGIC DIAGRAMS

SN54LS/74LS373



SN54LS/74LS374



V_{CC} = Pin 20
GND = Pin 10
◯ = Pin Numbers

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54 74			−1.0 −2.6	mA
I_{OL}	Output Current — Low	54 74			12 24	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.4	3.4		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.4	3.1		V		
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 12 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 24 mA	
I_{OZH}	Output Off Current HIGH				20	μA	V_{CC} = MAX, V_{OUT} = 2.7 V	
I_{OZL}	Output Off Current LOW				−20	μA	V_{CC} = MAX, V_{OUT} = 0.4 V	
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Short Circuit Current		−30		−130	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current				40	mA	V_{CC} = MAX	

AC CHARACTERISTICS: T_A = 25°C, V_{CC} = 5.0 V

SYMBOL	PARAMETER	LIMITS LS373 MIN	LS373 TYP	LS373 MAX	LS374 MIN	LS374 TYP	LS374 MAX	UNITS	TEST CONDITIONS
f_{MAX}	Maximum Clock Frequency				35	50		MHz	C_L = 45 pF, R_L = 667 Ω
t_{PLH} t_{PHL}	Propagation Delay, Data to Output		12 12	18 18				ns	
t_{PLH} t_{PHL}	Clock or Enable to Output		20 18	30 30		15 19	28 28	ns	
t_{PZH} t_{PZL}	Output Enable Time		15 25	28 36		20 21	28 28	ns	
t_{PHZ} t_{PLZ}	Output Disable Time		12 15	20 25		12 15	20 25	ns	C_L = 5.0 pF

AC SETUP REQUIREMENTS: T_A = 25°C, V_{CC} = 5.0 V

SYMBOL	PARAMETER	LIMITS LS373 MIN	LS373 MAX	LS374 MIN	LS374 MAX	UNITS
t_W	Clock Pulse Width	15		15		ns
t_s	Setup Time	5.0		20		ns
t_h	Hold Time	20		0		ns

DEFINITION OF TERMS:

SETUP TIME (t_s) — is defined as the minimum time required for the correct logic level to be present at the logic input prior to LE transition from HIGH-to-LOW in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) — is defined as the minimum time following the LE transition from HIGH-to-LOW that the logic level must be maintained at the input in order to ensure continued recognition.

AC WAVEFORMS

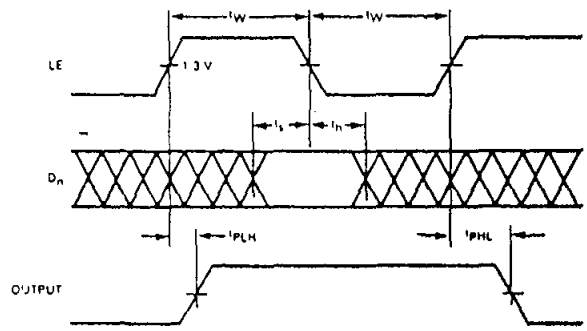


Fig. 1

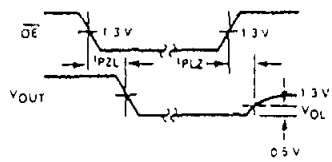


Fig. 2

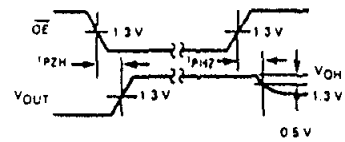
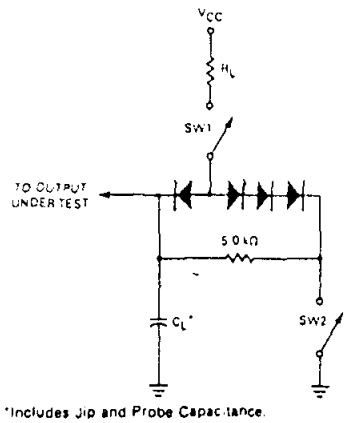


Fig. 3

AC LOAD CIRCUIT



*Includes Jig and Probe Capacitance.

SWITCH POSITIONS

SYMBOL	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

Fig. 4

AC WAVEFORMS

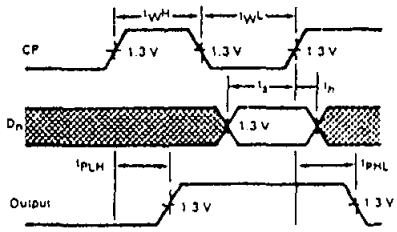


Fig. E

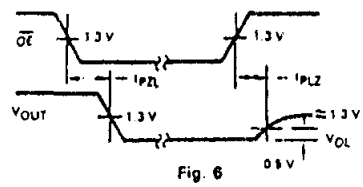


Fig. 6

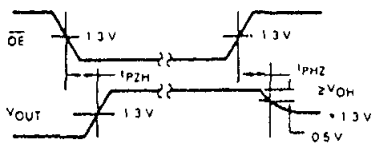
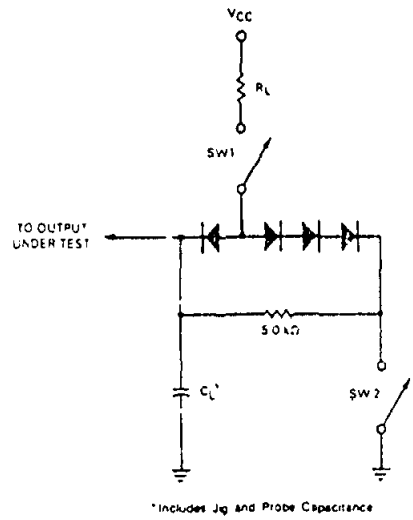


Fig. 7

SWITCH POSITIONS

SYMBOL	SW1	SW2
t_{PZH}	Open	Closed
t_{PZL}	Closed	Open
t_{PLZ}	Closed	Closed
t_{PHZ}	Closed	Closed

AC LOAD CIRCUIT



*Includes Jig and Probe Capacitance

Fig. 8

MOTOROLA

SN54/74LS75
SN54/74LS77

4-BIT D LATCH

LOW POWER SCHOTTKY

DESCRIPTION — The TTL/MSI SN54LS/74LS75 and SN54LS/74LS77 are latches used as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data (D) input is transferred to the Q output when the Enable is HIGH and the Q output will follow the data input as long as the Enable remains HIGH. When the Enable goes LOW, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the Enable is permitted to go HIGH.

The SN54LS/74LS75 features complementary Q and $\overline{Q}$ output from a 4-bit latch and is available in the 16-pin packages. For higher component density applications the SN54LS/74LS77 4-bit latch is available in the 14-pin package with $\overline{Q}$ outputs omitted.

PIN NAMES		LOADING (Note a) HIGH	LOW
$D_1 - D_4$	Data Inputs	0.5 U.L.	0.25 U.L.
E_{0-1}	Enable Input Latches 0, 1	2.0 U.L.	1.0 U.L.
E_{2-3}	Enable Input Latches 2, 3	2.0 U.L.	1.0 U.L.
$Q_1 - Q_4$	Latch Outputs (Note b)	10 U.L.	5(2.5) U.L.
$\overline{Q}_1 - \overline{Q}_4$	Complimentary Latch Outputs (Note b)	10 U.L.	5(2.5) U.L.

Notes:
a. 1 Unit Load (U.L.) = 40 μA HIGH
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

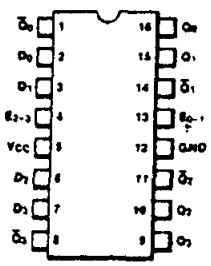
TRUTH TABLE
(Each latch)

t_n	t_{n+1}
D	Q
H	H
L	L

NOTES
t_n = bit time before enable negative-going transition
t_{n+1} = bit time after enable negative-going transition

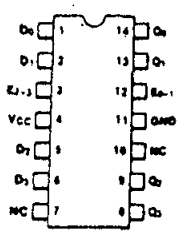
CONNECTION DIAGRAMS
DIP (TOP VIEW)

SN54LS/74LS75



J Suffix — Case 620-09 (Ceramic)
N Suffix — Case 648-08 (Plastic)

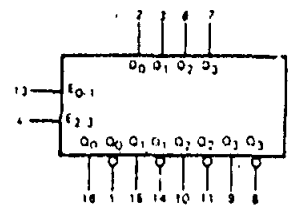
SN54LS/74LS77



J Suffix — Case 632-08 (Ceramic)
N Suffix — Case 646-06 (Plastic)

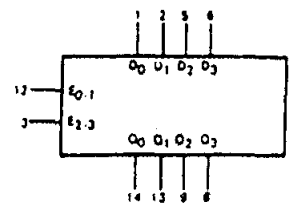
LOGIC SYMBOLS

SN54LS/74LS75



V_{CC} = Pin 5
GND = Pin 12

SN54LS/74LS77



V_{CC} = Pin 4
GND = Pin 11
NC = Pin 7,10

5

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.7	3.5		V	
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current	D Input E Input			20 80	μA	V_{CC} = MAX, V_{IN} = 2.7 V
		D Input E Input			0.1 0.4	mA	V_{CC} = MAX, V_{IN} = 7.0 V
I_{IL}	Input LOW Current	D Input E Input			−0.4 −1.6	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Short Circuit Current		−20		−100	mA	V_{CC} = MAX
I_{CC}	Power Supply Current				12	mA	V_{CC} = MAX

AC CHARACTERISTICS: T_A = 25°C, V_{CC} = 5.0 V

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_{PLH} t_{PHL}	Propagation Delay, Data to Q		15 9.0	27 17	ns	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH} t_{PHL}	Propagation Delay, Data to $\overline{Q}$		12 7.0	20 15	ns	
t_{PLH} t_{PHL}	Propagation Delay, Enable to Q		15 14	27 25	ns	
t_{PLH} t_{PHL}	Propagation Delay, Enable to $\overline{Q}$		16 7.0	30 15	ns	

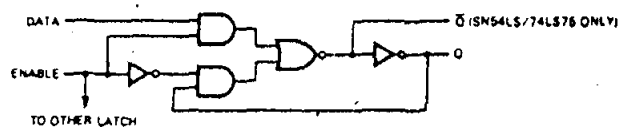
DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.7	3.5		V		
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current	D Input			20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
		E Input			80			
		D Input			0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
		E Input			0.4			
I_{IL}	Input LOW Current	D Input			−0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
		E Input			−1.6			
I_{OS}	Short Circuit Current		−20		−100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current				13	mA	V_{CC} = MAX	

AC CHARACTERISTICS: T_A = 25°C, V_{CC} = 5.0 V

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_{PLH}	Propagation Delay, Data to Q		11	19	ns	V_{CC} = 5.0 V, C_L = 15 pF
t_{PHL}			9.0	17		
t_{PLH}	Propagation Delay, Enable to Q		10	18	ns	
t_{PHL}			10	18		

LOGIC DIAGRAM



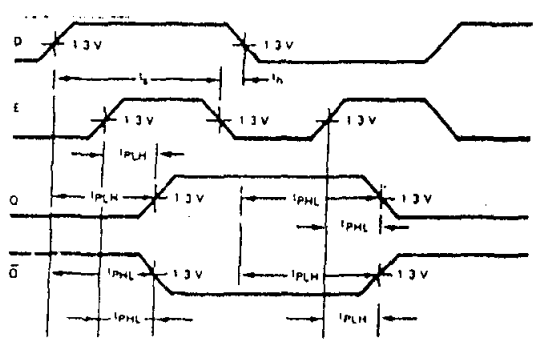
GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

AC SETUP REQUIREMENTS: $T_A = 25°C$, $V_{CC} = 5.0\ V$

SYMBOL	PARAMETER	LIMITS			UNITS	TEST CONDITIONS
		MIN	TYP	MAX		
t_W	Enable Pulse Width High	20			ns	$V_{CC} = 5.0\ V$
t_s	Setup Time	20			ns	
t_h	Hold Time	0			ns	

AC WAVE FORMS



DEFINITION OF TERMS:

SETUP TIME (t_s) — is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from HIGH-to-LOW in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) — is defined as the minimum time following the clock transition from HIGH-to-LOW that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from HIGH-to-LOW and still be recognized.

MOTOROLA

SN54/74LS47

BCD TO 7-SEGMENT DECODER/DRIVER

LOW POWER SCHOTTKY

DESCRIPTION — The SN54LS/74LS47 are Low Power Schottky BCD to 7-Segment Decoder/Drivers consisting of NAND gates, input buffers and seven AND-OR-INVERT gates. They offer active LOW, high sink current outputs for driving indicators directly. Seven NAND gates and one driver are connected in pairs to make BCD data and its complement available to the seven decoding AND-OR-INVERT gates. The remaining NAND gate and three input buffers provide lamp test, blanking input/ripple-blanking output and ripple-blanking input.

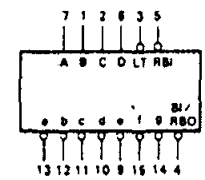
The circuits accept 4-bit binary-coded-decimal (BCD) and, depending on the state of the auxiliary inputs, decodes this data to drive a 7-segment display indicator. The relative positive-logic output levels, as well as conditions required at the auxiliary inputs, are shown in the truth tables. Output configurations of the SN54LS/74LS47 are designed to withstand the relatively high voltages required for 7-segment indicators.

These outputs will withstand 15 V with a maximum reverse current of 250 μA. Indicator segments requiring up to 24 mA of current may be driven directly from the SN74LS47 high performance output transistors. Display patterns for BCD input counts above nine are unique symbols to authenticate input conditions.

The SN54LS/74LS47 incorporates automatic leading and/or trailing-edge zero-blanking control (RBI and RBO). Lamp test (LT) may be performed at any time which the BI/RBO node is a HIGH level. This device also contains an overriding blanking input (BI) which can be used to control the lamp intensity or to inhibit the outputs.

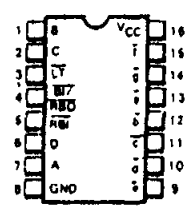
- LAMP INTENSITY MODULATION CAPABILITY
- OPEN COLLECTOR OUTPUTS
- LAMP TEST PROVISION
- LEADING/TRAILING ZERO SUPPRESSION
- INPUT CLAMP DIODES LIMIT HIGH-SPEED TERMINATION EFFECTS

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



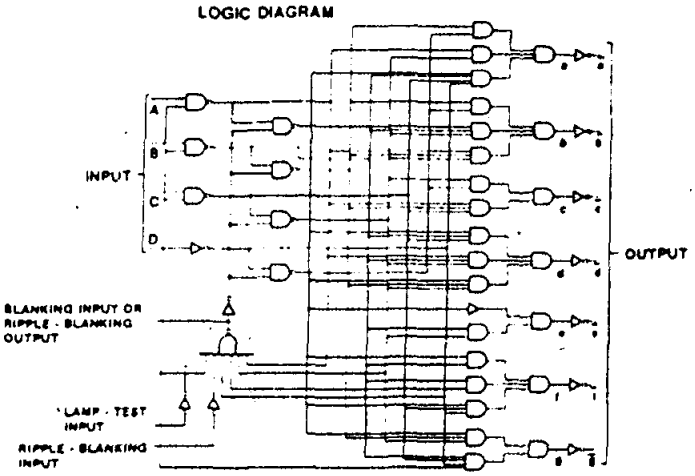
J Suffix — Case 620-09 (Ceramic)
N Suffix — Case 648-08 (Plastic)

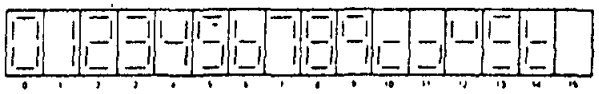
PIN NAMES

		LOADING (Note a) HIGH	LOW
A, B, C, D	BCD Inputs	0.5 U.L.	0.25 U.L.
$\overline{RBI}$	Ripple Blanking Input	0.5 U.L.	0.25 U.L.
$\overline{LT}$	Lamp Test Input	0.5 U.L.	0.25 U.L.
$\overline{BI/RBO}$	Blanking Input or Ripple Blanking Output	0.5 U.L. / 1.2 U.L.	0.75 U.L. / 2.0 U.L.
$\bar{a}$, to $\bar{g}$	Outputs	Open-Collector	15 (7.5) U.L.

Notes:
a) 1 Unit Load (U.L.) = 40 μA HIGH, 1.6 mA LOW
b) Output current measured at V_{OUT} = 0.5 V
Output LOW drive factor is 7.5 U.L. for Military (54) and 15 U.L. for Commercial (74) Temperature Ranges.

LOGIC DIAGRAM





NUMERICAL DESIGNATIONS – RESULTANT DISPLAYS

TRUTH TABLE

DECIMAL OR FUNCTION	INPUTS $\overline{LT}$	$\overline{RBI}$	D	C	B	A	$\overline{BI}/\overline{RBO}$	OUTPUTS a	b	c	d	e	f	g	NOTE
0	H	H	L	L	L	L	H	L	L	L	L	L	L	H	A
1	H	X	L	L	L	H	H	H	L	L	H	H	H	H	A
2	H	X	L	L	H	L	H	L	L	H	L	L	H	L	
3	H	X	L	L	H	H	H	L	L	L	L	H	H	L	
4	H	X	L	H	L	L	H	H	L	L	H	H	L	L	
5	H	X	L	H	L	H	H	L	H	L	L	H	L	L	
6	H	X	L	H	H	L	H	H	H	L	L	L	L	L	
7	H	X	L	H	H	H	H	L	L	L	H	H	H	H	
8	H	X	H	L	L	L	H	L	L	L	L	L	L	L	
9	H	X	H	L	L	H	H	L	L	L	H	H	L	L	
10	H	X	H	L	H	L	H	H	H	H	L	L	H	L	
11	H	X	H	L	H	H	H	H	H	L	L	H	H	L	
12	H	X	H	H	L	L	H	H	L	H	H	H	L	L	
13	H	X	H	H	L	H	H	L	H	H	L	H	L	L	
14	H	X	H	H	H	L	H	H	H	H	L	L	L	L	
15	H	X	H	H	H	H	H	H	H	H	H	H	H	H	
$\overline{BI}$	X	X	X	X	X	X	L	H	H	H	H	H	H	H	B
$\overline{RBI}$	H	L	L	L	L	L	L	H	H	H	H	H	H	H	C
$\overline{LT}$	L	X	X	X	X	X	H	L	L	L	L	L	L	L	D

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

NOTES:

(A) $\overline{BI}/\overline{RBO}$ is wire-AND logic serving as blanking input ($\overline{BI}$) and/or ripple-blanking output ($\overline{RBO}$). The blanking out ($\overline{BI}$) must be open or held at a HIGH level when output functions 0 through 15 are desired, and ripple-blanking input ($\overline{RBI}$) must be open or at a HIGH level if blanking of a decimal 0 is not desired. X = input may be HIGH or LOW.

(B) When a LOW level is applied to the blanking input (forced condition) all segment outputs go to a LOW level regardless of the state of any other input condition.

(C) When ripple-blanking input ($\overline{RBI}$) and inputs A, B, C, and D are at LOW level, with the lamp test input at HIGH level, all segment outputs go to a HIGH level and the ripple-blanking output ($\overline{RBO}$) goes to a LOW level (response condition).

(D) When the blanking input/ripple-blanking output ($\overline{BI}/\overline{RBO}$) is open or held at a HIGH level, and a LOW level is applied to lamp test input, all segment outputs go to a LOW level.

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High $\overline{BI/RBO}$	54,74			−50	μA
I_{OL}	Output Current — Low $\overline{BI/RBO}$ $\overline{BI/RBO}$	54 74			1.6 3.2	mA
$V_{O(off)}$	Off-State Output Voltage $\bar{a}$ to $\bar{g}$	54,74			15	V
$I_{O(on)}$	On-State Output Current $\bar{a}$ to $\bar{g}$ $\bar{a}$ to $\bar{g}$	54 74			12 24	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Threshold Voltage for All Inputs
V_{IL}	Input LOW Voltage	54 74			0.7 0.8	V	Guaranteed Input LOW Threshold Voltage for All Inputs
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage, $\overline{BI/RBO}$		2.4	4.2		V	V_{CC} = MIN, I_{OH} = −50 μA, V_{IN} = V_{IH} or V_{IL} per Truth Table
V_{OL}	Output LOW Voltage $\overline{BI/RBO}$	54,74		0.25	0.4	V	I_{OL} = 1.6 mA; V_{CC} = MIN, V_{IN} = V_{IH}
		74		0.35	0.5	V	I_{OL} = 3.2 MA; or V_{IL} per Truth Table
$I_{O(off)}$	Off-State Output Current $\bar{a}$ thru $\bar{g}$				250	μA	V_{CC} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table, V_O (off) = 15 V
$V_{O(on)}$	On-State Output Voltage $\bar{a}$ thru $\bar{g}$	54,74		0.25	0.4	V	$I_{O(on)}$ = 12 mA; V_{CC} = MAX, V_{IN} = V_{IH}
		74		0.35	0.5	V	$I_{O(on)}$ = 24 MA; or V_{IL} per Truth Table
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V
I_{IL}	Input LOW Current $\overline{BI/RBO}$ Any Input except $\overline{BI/RBO}$				−1.2 −0.4	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS} $\overline{BI/RBO}$	Output Short Circuit Current		−0.3		−2.0	mA	V_{CC} = MAX, V_{OUT} = 0 V
I_{CC}	Power Supply Current			7.0	13	mA	V_{CC} = MAX

AC CHARACTERISTICS: T_A = 25°C

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_{PHL} t_{PLH}	Propagation Delay, Address Input to Segment Output			100 100	ns ns	V_{CC} = 5.0 V C_L = 15 pF
t_{PHL} t_{PLH}	Propagation Delay, $\overline{RBI}$ Input To Segment Output			100 100	ns ns	

AC WAVEFORMS

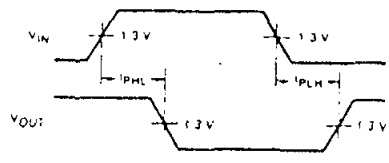


Fig 1

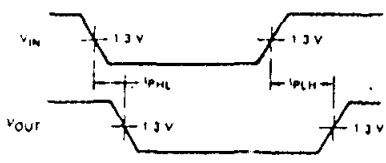


Fig 2

MOTOROLA

SN54/74LS85

4-BIT MAGNITUDE COMPARATOR

LOW POWER SCHOTTKY

DESCRIPTION — The SN54LS/74LS85 is a 4-Bit Magnitude Comparator which compares two 4-bit words (A, B), each word having four Parallel Inputs (A_0-A_3, B_0-B_3); A_3, B_3 being the most significant inputs. Operation is not restricted to binary codes, the device will work with any monotonic code. Three Outputs are provided: "A greater than B" ($O_{A>B}$), "A less than B" ($O_{A<B}$), "A equal to B" ($O_{A=B}$). Three Expander Inputs, $I_{A>B}$, $I_{A<B}$, $I_{A=B}$, allow cascading without external gates. For proper compare operation, the Expander Inputs to the least significant position must be connected as follows: $I_{A<B} = I_{A>B} = L$, $I_{A=B} = H$. For serial (ripple) expansion, the $O_{A>B}$, $O_{A<B}$ and $O_{A=B}$ Outputs are connected respectively to the $I_{A>B}$ $I_{A<B}$, and $I_{A=B}$ inputs of the next most significant comparator, as shown in Figure 1. Refer to Applications section of data sheet for high speed method of comparing large words.

The Truth Table on the following page describes the operation of the SN54LS/74LS85 under all possible logic conditions. The upper 11 lines describe the normal operation under all conditions that will occur in a single device or in a series expansion scheme. The lower five lines describe the operation under abnormal conditions on the cascading inputs. These conditions occur when the parallel expansion technique is used.

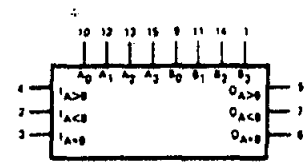
- **EASILY EXPANDABLE**
- **BINARY OR BCD COMPARISON**
- **$O_{A>B}$, $O_{A<B}$, AND $O_{A=B}$ OUTPUTS AVAILABLE**

PIN NAMES

		LOADING (Note a) HIGH	LOW
A_0-A_3, B_0-B_3	Parallel Inputs	1.5 U.L.	0.75 U.L.
$I_{A=B}$	A = B Expander Inputs	1.5 U.L.	0.75 U.L.
$I_{A<B}$, $I_{A>B}$	A < B, A > B, Expander Inputs	0.5 U.L.	0.25 U.L.
$O_{A>B}$	A Greater Than B Output (Note b)	10 U.L.	5 (2.5) U.L.
$O_{A<B}$	B Greater Than A Output (Note b)	10 U.L.	5 (2.5) U.L.
$O_{A=B}$	A Equal to B Output (Note b)	10 U.L.	5 (2.5) U.L.

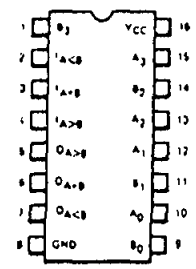
Notes:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

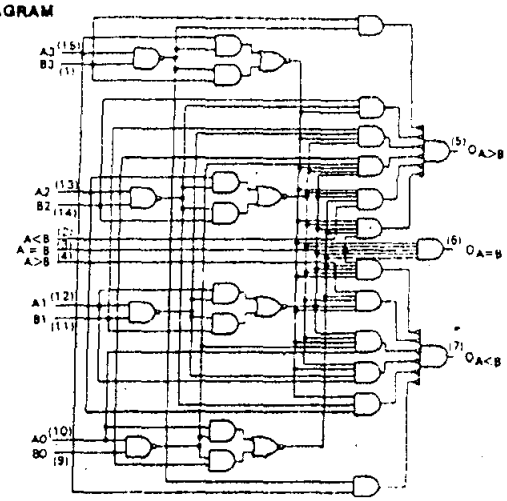
CONNECTION DIAGRAM DIP (TOP VIEW)



J Suffix — Case 620-09 (Ceramic)
N Suffix — Case 648-08 (Plastic)

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

LOGIC DIAGRAM



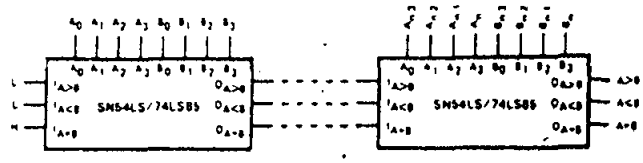
TRUTH TABLE

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A_3,B_3	A_2,B_2	A_1,B_1	A_0,B_0	$I_{A>B}$	$I_{A<B}$	$I_{A=B}$	$O_{A>B}$	$O_{A<B}$	$O_{A=B}$
$A_3>B_3$	X	X	X	X	X	X	H	L	L
$A_3<B_3$	X	X	X	X	X	X	L	H	L
$A_3=B_3$	$A_2>B_2$	X	X	X	X	X	H	L	L
$A_3=B_3$	$A_2<B_2$	X	X	X	X	X	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1>B_1$	X	X	X	X	H	L	L
$A_3=B_3$	$A_2=B_2$	$A_1<B_1$	X	X	X	X	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0>B_0$	X	X	X	H	L	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0<B_0$	X	X	X	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	H	L	L	H	L	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	L	H	L	L	H	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	X	X	H	L	L	H
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	H	H	L	L	L	L
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	L	L	L	H	H	L

H = HIGH Level
L = LOW Level
X = IMMATERIAL

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA



L = LOW Level
H = HIGH Level

Fig. 1. COMPARING TWO n-BIT WORDS

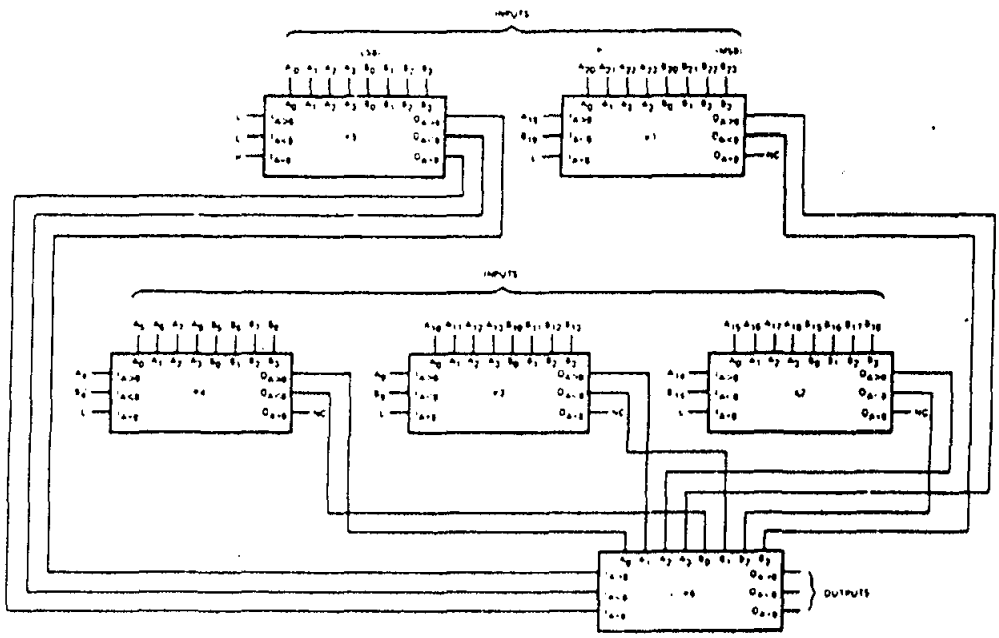
APPLICATIONS

Figure 2 shows a high speed method of comparing two 24-bit words with only two levels of device delay. With the technique shown in Figure 1, six levels of device delay result when comparing two 24-bit words. The parallel technique can be expanded to any number of bits, see Table I.

TABLE I

WORD LENGTH	NUMBER OF PKGS.
1-4 Bits	1
5-24 Bits	2 - 6
25-120 Bits	8 - 31

NOTE
The SN54LS/74LS85 can be used as a 5-bit comparator only when the outputs are used to drive the A_0-A_3 and B_0-B_3 inputs of another SN54LS/74LS85 as shown in Figure 2 in positions #1, 2, 3, and 4



MSB = Most Significant Bit
LSB = Least Significant Bit

L = LOW Level
H = HIGH Level
NC = No Connection

Fig. 2. COMPARISON OF TWO 24-BIT WORDS

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs
		74			0.8		
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table
		74	2.7	3.5		V	
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA; V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA
I_{IH}	Input HIGH Current A < B, A > B Other Inputs				20 60	μA	V_{CC} = MAX, V_{IN} = 2.7 V
	A < B, A > B Other Inputs				0.1 0.3	mA	V_{CC} = MAX, V_{IN} = 7.0 V
I_{IL}	Input LOW Current A < B, A > B Other Inputs				−0.4 −1.2	mA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{OS}	Output Short Circuit Current		−20		−100	mA	V_{CC} = MAX
I_{CC}	Power Supply Current				20	mA	V_{CC} = MAX

AC CHARACTERISTICS: T_A = 25°C, V_{CC} = 5.0 V

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
t_{PLH} t_{PHL}	Any A or B to A < B, A > B		24 20	36 30	ns	V_{CC} = 5.0 V C_L = 15 pF
t_{PLH} t_{PHL}	Any A or B to A = B		27 23	45 45	ns	
t_{PLH} t_{PHL}	A < B or A = B to A > B		14 11	22 17	ns	
t_{PLH} t_{PHL}	A = B to A = B		13 13	20 26	ns	
t_{PLH} t_{PHL}	A > B or A = B to A < B		14 11	22 17	ns	

AC WAVEFORMS

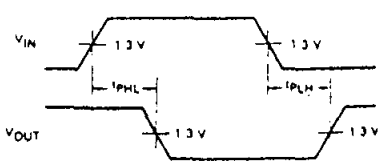


Fig. 3

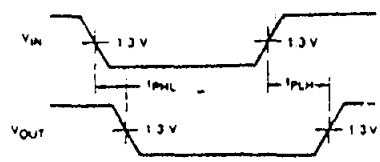


Fig. 4

MOTOROLA

SN54/74LS90
SN54/74LS92
SN54/74LS93

DECADE COUNTER; DIVIDE-BY-TWELVE COUNTER; 4-BIT BINARY COUNTER

LOW POWER SCHOTTKY

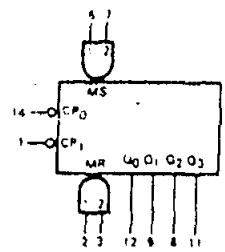
DESCRIPTION — The SN54LS/74LS90, SN54LS/74LS92 and SN54LS/74LS93 are high-speed 4-bit ripple type counters partitioned into two sections. Each counter has a divide-by-two section and either a divide-by-five (LS90), divide-by-six (LS92) or divide-by-eight (LS93) section which are triggerd by a HIGH-to-LOW transition on the clock inputs. Each section can be used separately or tied together (Q to $\overline{CP}$) to form BCD, bi-quinary, modulo-12, or modulo-16 counters. All of the counters have a 2-input gated Master Reset (Clear), and the LS90 also has a 2-input gated Master Set (Preset 9).

J Suffix — Case 632-08 (Ceramic)
N Suffix — Case 646-06 (Plastic)

- LOW POWER CONSUMPTION . . . TYPICALLY 45 mW
- HIGH COUNT RATES . . . TYPICALLY 42 MHz
- CHOICE OF COUNTING MODES . . . BCD, BI-QUINARY, DIVIDE-BY-TWELVE, BINARY
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS

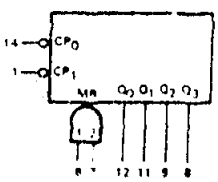
LOGIC SYMBOL

LS90



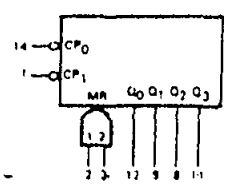
V_{CC} = Pin 5
GND = Pin 10
NC = Pins 4, 13

LS92



V_{CC} = Pin 5
GND = Pin 10
NC = Pins 7, 3, 4, 13

LS93



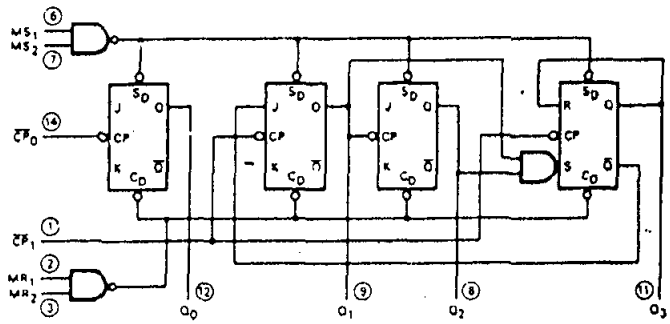
V_{CC} = Pin 5
GND = Pin 10
NC = Pins 4, 6, 7, 13

PIN NAMES		LOADING (Note a) HIGH	LOW
$\overline{CP}_0$	Clock (Active LOW going edge) Input to ÷2 Section	0.5 U.L.	1.5 U.L.
$\overline{CP}_1$	Clock (Active LOW going edge) Input to ÷5 Section (LS90), ÷6 Section (LS92)	0.5 U.L.	2.0 U.L.
$\overline{CP}_1$	Clock (Active LOW going edge) Input to ÷8 Section (LS93)	0.5 U.L.	1.0 U.L.
MR_1, MR_2	Master Reset (Clear) Inputs	0.5 U.L.	0.25 U.L.
MS_1, MS_2	Master Set (Preset-9, LS90) Inputs	0.5 U.L.	0.25 U.L.
Q_0	Output from ÷2 Section (Notes b & c)	10 U.L.	5(2.5) U.L.
Q_1, Q_2, Q_3	Outputs from ÷5 (LS90), ÷6 (LS92), ÷8 (LS93) Sections (Note b)	10 U.L.	5(2.5) U.L.

Notes:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military, (54) and 5 U.L. for commercial (74) Temperature Ranges.
c. The Q_0 Outputs are guaranteed to drive the full fan-out plus the $\overline{CP}_1$ input of the device.
d. To insure proper operation the rise (t_r) and fall time (t_f) of the clock must be less than 100 ns.

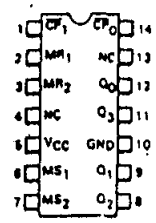
LOGIC DIAGRAM

LS90



○ = Pin Numbers
V_{CC} = Pin 5
GND = Pin 10

CONNECTION DIAGRAM
DIP (TOP VIEW)

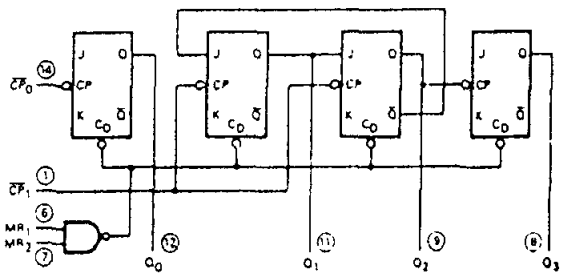


NC = No Internal Connection

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

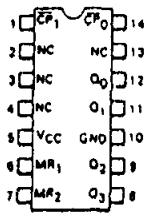
LOGIC DIAGRAM

LS92



○ = Pin Numbers
V_{CC} = Pin 5
GND = Pin 10

CONNECTION DIAGRAM
DIP (TOP VIEW)

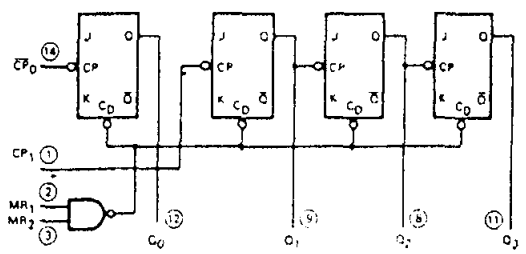


NC = No Internal Connection

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package

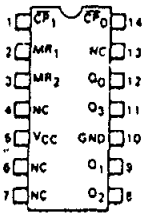
LOGIC DIAGRAM

LS93



○ = Pin Numbers
V_{CC} = Pin 5
GND = Pin 10

CONNECTION DIAGRAM
DIP (TOP VIEW)



NC = No Internal Connection

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package

FUNCTIONAL DESCRIPTION — The LS90, LS92, and LS93 are 4-bit ripple type Decade, Divide-By-Twelve, and Binary Counters respectively. Each device consists of four master/slave flip-flops which are internally connected to provide a divide-by-two section and a divide-by-five (LS90), divide-by-six (LS92), or divide-by-eight (LS93) section. Each section has a separate clock input which initiates state changes of the counter on the HIGH-to-LOW clock transition. State changes of the Q outputs do not occur simultaneously because of internal ripple delays. Therefore, decoded output signals are subject to decoding spikes and should not be used for clocks or strobes. The Q_0 output of each device is designed and specified to drive the rated fan-out plus the $\overline{CP}_1$ input of the device.

A gated AND asynchronous Master Reset ($MR_1 \bullet MR_2$) is provided on all counters which overrides and clocks and resets (clears) all the flip-flops. A gated AND asynchronous Master Set ($MS_1 \bullet MS_2$) is provided on the LS90 which overrides the clocks and the MR inputs and sets the outputs to nine (HLLH).

Since the output from the divide-by-two section is not internally connected to the succeeding stages, the devices may be operated in various counting modes.

LS90

A. BCD Decade (8421) Counter — The $\overline{CP}_1$ input must be externally connected to the Q_0 output. The $\overline{CP}_0$ input receives the incoming count and a BCD count sequence is produced.

B. Symmetrical Bi-quinary Divide-By-Ten Counter — The Q_3 output must be externally connected to the $\overline{CP}_0$ input. The input count is then applied to the $\overline{CP}_1$ input and a divide-by-ten square wave is obtained at output Q_0.

C. Divide-By-Two and Divide-By-Five Counter — No external interconnections are required. The first flip-flop is used as a binary element for the divide-by-two function ($\overline{CP}_0$ as the input and Q_0 as the output). The $\overline{CP}_1$ input is used to obtain binary divide-by-five operation at the Q_3 output.

LS92

A. Modulo 12, Divide-By-Twelve Counter — The $\overline{CP}_1$ input must be externally connected to the Q_0 output. The $\overline{CP}_0$ input receives the incoming count and Q_3 produces a symmetrical divide-by-twelve square wave output.

B. *Divide-By-Two and Divide-By-Six Counter — No external interconnections are required. The first flip-flop is used as a binary* element for the divide-by-two function. The $\overline{CP}_1$ input is used to obtain divide-by-three operation at the Q_1 and Q_2 outputs and divide-by-six operation at the Q_3 output.

LS93

A. 4-Bit Ripple Counter — The output Q_0 must be externally connected to input $\overline{CP}_1$. The input count pulses are applied to input $\overline{CP}_0$. Simultaneous divisions of 2, 4, 8, and 16 are performed at the Q_0, Q_1, Q_2, and Q_3 outputs as shown in the truth table.

B. 3-Bit Ripple Counter — The input count pulses are applied to input $\overline{CP}_1$. Simultaneous frequency divisions of 2, 4, and 8 are available at the Q_1, Q_2, and Q_3 outputs. Independent use of the first flip-flop is available if the reset function coincides with reset of the 3-bit ripple-through counter.

LS90
MODE SELECTION

RESET/SET INPUTS				OUTPUTS			
MR_1	MR_2	MS_1	MS_2	Q_0	Q_1	Q_2	Q_3
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	H
L	X	L	X	Count			
X	L	X	L	Count			
L	X	X	L	Count			
X	L	L	X	Count			

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

LS92 AND LS93
MODE SELECTION

RESET INPUTS		OUTPUTS			
MR_1	MR_2	Q_0	Q_1	Q_2	Q_3
H	H	L	L	L	L
L	H	Count			
H	L	Count			
L	L	Count			

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

LS90
BCD COUNT SEQUENCE

COUNT	OUTPUT			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

NOTE: Output Q_0 is connected to input $\overline{CP}_1$ for BCD count.

LS92
TRUTH TABLE

COUNT	OUTPUT			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	L	L	H
7	H	L	L	H
8	L	H	L	H
9	H	H	L	H
10	L	L	H	H
11	H	L	H	H

Note: Output Q_0 connected to input $\overline{CP}_1$.

LS93
TRUTH TABLE

COUNT	OUTPUT			
	Q_0	Q_1	Q_2	Q_3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H
10	L	H	L	H
11	H	H	L	H
12	L	L	H	H
13	H	L	H	H
14	L	H	H	H
15	H	H	H	H

Note: Output Q_0 connected to input $\overline{CP}_1$.

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage	54			0.7	V	Guaranteed Input LOW Voltage for All Inputs	
		74			0.8			
V_{IK}	Input Clamp Diode Voltage			−0.65	−1.5	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54	2.5	3.5		V	V_{CC} = MIN, I_{OH} = MAX, V_{IN} = V_{IH} or V_{IL} per Truth Table	
		74	2.7	3.5		V		
V_{OL}	Output LOW Voltage	54,74		0.25	0.4	V	I_{OL} = 4.0 mA	V_{CC} = V_{CC} MIN, V_{IN} = V_{IL} or V_{IH} per Truth Table
		74		0.35	0.5	V	I_{OL} = 8.0 mA	
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current MS, MR $\overline{CP}_0$ $\overline{CP}_1$ (LS90, LS92) $\overline{CP}_1$ (LS93)				−0.4 −2.4 −3.2 −1.6	mA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{OS}	Short Circuit Current		−20		−100	mA	V_{CC} = MAX	
I_{CC}	Power Supply Current				15	mA	V_{CC} = MAX	

AC CHARACTERISTICS: T_A = 25°C, V_{CC} = 5.0 V, C_L = 15 pF

SYMBOL	PARAMETER	LIMITS									UNITS
		LS90			LS92			LS93			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
f_{MAX}	$\overline{CP}_0$ Input Clock Frequency	32			32			32			MHz
f_{MAX}	$\overline{CP}_1$ Input Clock Frequency	16			16			16			MHz
t_{PLH} t_{PHL}	Propagation Delay, $\overline{CP}_0$ Input to Q_0 Output		10 12	16 18		10 12	16 18		10 12	16 18	ns
t_{PLH} t_{PHL}	$\overline{CP}_0$ Input to Q_3 Output		32 34	48 50		32 34	48 50		46 46	70 70	ns
t_{PLH} t_{PHL}	$\overline{CP}_1$ Input to Q_1 Output		10 14	16 21		10 14	16 21		10 14	16 21	ns
t_{PLH} t_{PHL}	$\overline{CP}_1$ Input to Q_2 Output		21 23	32 35		10 14	16 21		21 23	32 35	ns
t_{PLH} t_{PHL}	$\overline{CP}_1$ Input to Q_3 Output		21 23	32 35		21 23	32 35		34 34	51 51	ns
t_{PLH}	MS Input to Q_0 and Q_3 Outputs		20	30							ns
t_{PHL}	MS Input to Q_1 and Q_2 Outputs		26	40							ns
t_{PHL}	MR Input to Any Output		26	40		26	40		26	40	ns

AC SETUP REQUIREMENTS: T_A = 25°C, V_{CC} = 5.0 V

SYMBOL	PARAMETER	LIMITS						UNITS
		LS90		LS92		LS93		
		MIN	MAX	MIN	MAX	MIN	MAX	
t_W	$\overline{CP}_0$ Pulse Width	15		15		15		ns
t_W	$\overline{CP}_1$ Pulse Width	30		30		30		ns
t_W	MS Pulse Width	15						ns
t_W	MR Pulse Width	15		15		15		ns
t_{rec}	Recovery Time MR to $\overline{CP}$	25		25		25		ns

RECOVERY TIME (t_{rec}) is defined as the minimum time required between the end of the reset pulse and the clock transition from HIGH-to-LOW in order to recognize and transfer HIGH data to the Q outputs.

AC WAVE FORMS

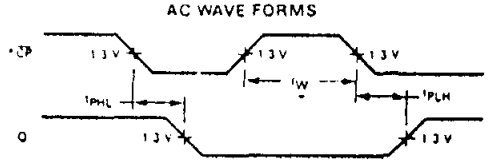


Fig. 1

*The number of Clock Pulses required between the t_{PHL} and t_{PLH} measurements can be determined from the appropriate Truth Tables.

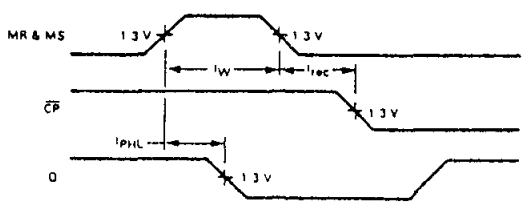


Fig. 2

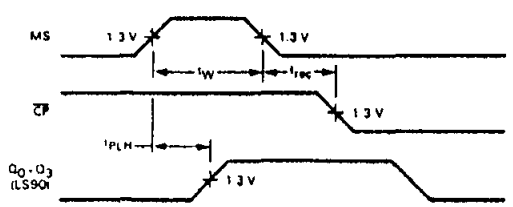
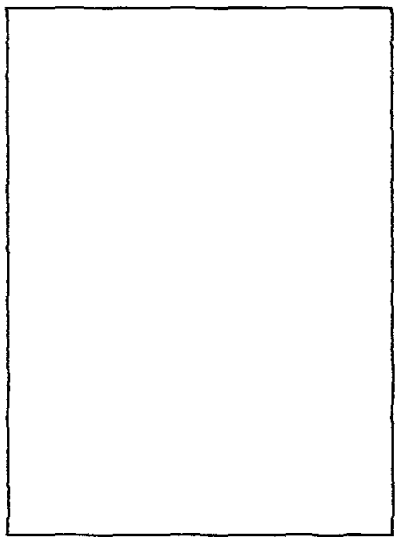


Fig. 3

BIODATA



Nama	:Maria Vironika Trimuriana
NRP	: 5103096029
NIRM	: 96.7.003.31073.44913
Tempat, Tanggal Lahir	: Surabaya, 23 Maret 1978
Agama	: Katolik
Alamat	: Jl. Ngeni Jaya No.1 Kepuhkiriman - Waru Sidoarjo

Riwayat Pendidikan :

- Tahun 1990 Lulus SD Kemala Bhayangkari 1 Surabaya
- Tahun 1993 Lulus SMP Negeri I Waru Sidoarjo
- Tahun 1996 Lulus SMA Negeri 10 Surabaya
- Tahun 2001 Lulus Sarjana Fakultas Teknik Jurusan Teknik Elektro Universitas Katolik Widya Mandala Surabaya.