LAMPIRAN

LAMPIRAN

Listing Program

```
;-------------------------------------------------------------
;                  Program Mesin Pengatur Antrian
;                  oleh Galih Wibowo Koselan
;                        5103094033
;                        30 Juli 2002
;-------------------------------------------------------------


            .DATA
            ORG    30H
ANTRIAN     DS     1
DIGIT01     DS     1            ;Digit 7 Segment untuk tampilan
DIGIT02     DS     1            ;Tanggal dan Bulan
DIGIT03     DS     1
DIGIT04     DS     1
DIGIT05     DS     1            ;Digit Printer Antrian
DIGIT06     DS     1            ;Digit Printer Antrian
DIGIT07     DS     1            ;Digit 7 Segment untuk nomor antrian
DIGIT08     DS     1
DIGIT09     DS     1
DIGIT10     DS     1
DIGIT11     DS     1            ;Digit Printer Pemenuhan
DIGIT12     DS     1            ;Digit Printer Pemenuhan
DIGIT13     DS     1            ;Digit 7 Segment untuk tampilan
DIGIT14     DS     1            ;Tahun
TANGGAL     DS     1            ;Untuk Variabel Tanggal
BULAN       DS     1            ;Untuk Variabel Bulan
TAHUN       DS     1            ;Untuk Variabel Tahun
TAMPUNG01   DS     1            ;Untuk Variabel Jumlah Antrian
TAMPUNG02   DS     1            ;Untuk Variabel Jumlah Pelayanan
TAMPUNG03   DS     1            ;Untuk Variabel Jumlah Pemenuhan
TAMPUNG04   DS     1
TAMPUNG05   DS     1
TAMPUNG06   DS     1
TAMPUNG07   DS     1

            .CODE
            ORG    00H
            AJMP   START

            ORG    50H

;-------------------------
;     Inisialisasi Awal
;-------------------------
IA          CLR    P3.6         ;Matikan Speaker
            MOV    R0,#TANGGAL
            MOV    BULAN,#1
```

```
            MOV   TANGGAL,#1
            MOV   TAHUN,#1
            MOV   TAMPUNG01,#0
            MOV   TAMPUNG02,#0
            MOV   TAMPUNG03,#0
            MOV   ANTRIAN,#0
            MOV   DIGIT01,#17H
            MOV   DIGIT02,#0BH
            MOV   DIGIT03,#1DH
            MOV   DIGIT04,#0EH
            MOV   DIGIT05,#0
            MOV   DIGIT06,#0
            MOV   DIGIT07,#07H
            MOV   DIGIT08,#0BH
            MOV   DIGIT09,#0DH
            MOV   DIGIT10,#0EH
            MOV   DIGIT11,#0
            MOV   DIGIT12,#0
            MOV   DIGIT13,#0BH
            MOV   DIGIT14,#17H
            MOV   TAMPUNG07,DIGIT04
            MOV   TAMPUNG06,DIGIT03
            MOV   TAMPUNG05,DIGIT02
            MOV   TAMPUNG04,DIGIT01
            RET

;--------------
;     Strobe
;--------------
STROBE      SETB  P0.7        ;Mengirim Sinyal High
            NOP               ;Mengirim Delay
            NOP
            CLR   P0.7        ;Mengirim Sinyal Low
            NOP               ;Mengirim Delay
            NOP
            JB    P0.6,$      ;Mengirim Sinyal Low ke Kaki Busy
            RET

;----------------------------
;     Inisialisasi Printer
;----------------------------
IP          MOV   A,#27       ;command mode
            ACALL   STROBE
            MOV   A,#64       ;reset printer
            ACALL   STROBE
            RET

;--------------------
;     Mode Printer
;--------------------
BK          MOV   P2,#1BH     ;Batas Kiri
            ACALL   STROBE
            MOV   P2,#6CH
            ACALL   STROBE
            MOV   P2,#10
            ACALL   STROBE
```

```
            RET

BS          MOV   P2,#1BH     ;Huruf Besar
            ACALL   STROBE
            MOV   P2,#45H
            ACALL   STROBE
            RET

DBS         MOV   P2,#1BH     ;Double Besar
            ACALL   STROBE
            MOV   P2,#0EH
            ACALL   STROBE
            RET

RESET       MOV   P2,#1BH     ;Reset Double Besar
            ACALL   STROBE
            MOV   P2,#46H
            ACALL   STROBE
            RET

LF          MOV   P2,#0AH     ;Line Feed
            ACALL STROBE
            RET

;-------------
;     Delay
;-------------
DELAY       MOV   R7,#0FFH    ;Melakukan Perhitungan sebagai
D01         MOV   R6,#0FFH    ;Delay
            DJNZ  R6,$
            DJNZ  R7,D01
            RET

;----------------------------
;     Cetak Nomor Antrian
;----------------------------
CNA         MOV   A,TAMPUNG01
            MOV   B,#10
            CLR   C
            DIV   AB
            ADD   A,#30H
            MOV   DIGIT06,A
            MOV   A,B
            ADD   A,#30H
            MOV   DIGIT05,A
EscCNA      RET

;----------------------
;     Cetak
;----------------------
C           MOV   A,#0
            MOVC  A,@A+DPTR
            JZ    EscC
            MOV   P2,A
            ACALL STROBE
            INC   DPTR
```

```
            SJMP  C
EscC        RET

;-------------------
;     Cetak Huruf
;-------------------
CH          ADD   A,#30H
            MOV   P2,A
            ACALL STROBE
            RET

;-------------------------
;     Cetak Spasi Dan -
;-------------------------
CS          MOV   P2,#20H
            ACALL STROBE
            MOV   P2,#2DH
            ACALL STROBE
            MOV   P2,#20H
            ACALL STROBE
            RET

;-------------------
;     Cetak Tahun
;-------------------
CThn        MOV   P2,#32H
            ACALL STROBE
            MOV   P2,#30H
            ACALL STROBE
            MOV   A,DIGIT13
            SWAP  A
            ANL   A,#0FH
            ADD   A,#30H
            MOV   P2,A
            ACALL STROBE
            MOV   A,DIGIT14
            SWAP  A
            ANL   A,#0FH
            ADD   A,#30H
            MOV   P2,A
            ACALL STROBE
            RET

KATA1       DB    'Tanggal : ',0
KATA2       DB    'Anda berada pada antrian',0
KATA3       DB    'NO : ',0

;--------------------------
;     Print Nomor Antrian
;--------------------------
PNA         ACALL BK          ;Batas Kiri
            MOV   DPTR,#KATA1
            ACALL C           ;Cetak
            MOV   A,DIGIT04
            SWAP  A
            ANL   A,#0FH
```

```
            ACALL CH
            MOV   A,DIGIT03
            SWAP  A
            ANL   A,#0FH
            ACALL CH
            ACALL CS
            MOV   A,DIGIT02
            SWAP  A
            ANL   A,#0FH
            ACALL CH
            MOV   A,DIGIT01
            SWAP  A
            ANL   A,#0FH
            ACALL CH
            ACALL CS
            ACALL CThn

            ACALL LF          ;Line Feed
            MOV   DPTR,#KATA2
            ACALL C           ;Cetak

            ACALL LF          ;Line Feed
            MOV   DPTR,#KATA3
            ACALL BS
            ACALL DBS
            ACALL C           ;Cetak
            MOV   P2,DIGIT06
            ACALL STROBE
            MOV   P2,DIGIT05
            ACALL STROBE
            ACALL RESET

            MOV   R5,#5
PNA01       ACALL LF          ;Line Feed
            DJNZ  R5,PNA01
            RET

;-------------------------------------
;     Cetak Nomor Antrian yg Dilayani
;-------------------------------------
CNAYD       INC   ANTRIAN
            MOV   R5,ANTRIAN
            CJNE  R5,#100,CNAYD01
            MOV   ANTRIAN,#01
CNAYD01     MOV   A,ANTRIAN
            MOV   B,#10
            DIV   AB
            SWAP  A
            ORL   A,#0EH
            MOV   DIGIT10,A
            MOV   A,B
            SWAP  A
            ORL   A,#0DH
            MOV   DIGIT09,A
            RET
```

```
;-------------------------------
;     Menampilkan Ke 7 Segmen
;-------------------------------
SEVEN       MOV   P1,DIGIT07
            SETB  P1.3
            MOV   P1,DIGIT08
            SETB  P1.2
            MOV   P1,DIGIT09
            SETB  P1.1
            MOV   P1,DIGIT10
            SETB  P1.0
            RET

;-------------------------------
;     Menampilkan Ke 7 Segmen
;-------------------------------
SEVEN02     MOV   P1,TAMPUNG04
            SETB  P1.3
            MOV   P1,TAMPUNG05
            SETB  P1.2
            MOV   P1,TAMPUNG06
            SETB  P1.1
            MOV   P1,TAMPUNG07
            SETB  P1.0
            RET

;---------------
;     Speaker
;---------------
SPK         SETB  P3.6
            MOV   R5,#7
SPK01       ACALL DELAY
            DJNZ  R5,SPK01
            CLR   P3.6
            RET

;--------------------------------------
;     Costumer Servis Menekan Tombol
;--------------------------------------
CSMT        INC   TAMPUNG02
            CLR   C
            MOV   A,TAMPUNG01
            MOV   R1,TAMPUNG02
            SUBB  A,R1
            JNC   CSMT01
            DEC   TAMPUNG02
            SJMP  EscCSMT
CSMT01      ACALL CNAYD       ;Cetak Nomor Antrian yg Dilayani
            ACALL SPK
EscCSMT     RET

;------------------------
;     Cek Tombol Bawah
;------------------------
CTB         JB    P0.2,EscCTB       ;BAWAH
            DEC   @R0
```

```
            CJNE   R0,#TANGGAL,CTB02
            CJNE   @R0,#0,CTB01
            MOV    @R0,#31
CTB01       MOV    A,@R0
            MOV    B,#10
            DIV    AB
            SWAP   A
            ORL    A,#0EH
            MOV    DIGIT04,A
            MOV    A,B
            SWAP   A
            ORL    A,#0DH
            MOV    DIGIT03,A
            MOV    TAMPUNG07,DIGIT04
            MOV    TAMPUNG06,DIGIT03
            MOV    TAMPUNG05,DIGIT02
            MOV    TAMPUNG04,DIGIT01
            SJMP   CTB06

CTB02       CJNE   R0,#BULAN,CTB04
            CJNE   @R0,#0,CTB03
            MOV    @R0,#12
CTB03       MOV    A,@R0
            MOV    B,#10
            DIV    AB
            SWAP   A
            ORL    A,#0BH
            MOV    DIGIT02,A
            MOV    A,B
            SWAP   A
            ORL    A,#07H
            MOV    DIGIT01,A
            MOV    TAMPUNG07,DIGIT04
            MOV    TAMPUNG06,DIGIT03
            MOV    TAMPUNG05,DIGIT02
            MOV    TAMPUNG04,DIGIT01
            SJMP   CTB06

CTB04       CJNE   @R0,#0,CTB05
            MOV    @R0,#99
CTB05       MOV    A,@R0
            MOV    B,#10
            DIV    AB
            SWAP   A
            ORL    A,#0BH
            MOV    DIGIT13,A
            MOV    A,B
            SWAP   A
            ORL    A,#07H
            MOV    DIGIT14,A
            MOV    TAMPUNG07,#2EH
            MOV    TAMPUNG06,#0DH
            MOV    TAMPUNG05,DIGIT13
            MOV    TAMPUNG04,DIGIT14

CTB06       JNB    P0.2,*       ;Switch dilepas ?
```

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            ACALL DELAY
EscCTB      RET

;-----------------------
;     Cek Tombol Atas
;-----------------------
CTA         JB    P0.1,EscCTA       ;ATAS
            INC   @R0
            CJNE  R0,#TANGGAL,CTA02
            CJNE  @R0,#32,CTA01
            MOV   @R0,#1
CTA01       MOV   A,@R0
            MOV   B,#10
            DIV   AB
            SWAP  A
            ORL   A,#0EH
            MOV   DIGIT04,A
            MOV   A,B
            SWAP  A
            ORL   A,#0DH
            MOV   DIGIT03,A
            MOV   TAMPUNG07,DIGIT04
            MOV   TAMPUNG06,DIGIT03
            MOV   TAMPUNG05,DIGIT02
            MOV   TAMPUNG04,DIGIT01
            SJMP  CTA06

CTA02       CJNE  R0,#BULAN,CTA04
            CJNE  @R0,#13,CTA03
            MOV   @R0,#1
CTA03       MOV   A,@R0
            MOV   B,#10
            DIV   AB
            SWAP  A
            ORL   A,#0BH
            MOV   DIGIT02,A
            MOV   A,B
            SWAP  A
            ORL   A,#07H
            MOV   DIGIT01,A
            MOV   TAMPUNG07,DIGIT04
            MOV   TAMPUNG06,DIGIT03
            MOV   TAMPUNG05,DIGIT02
            MOV   TAMPUNG04,DIGIT01
            SJMP  CTA06

CTA04       CJNE  @R0,#100,CTA05
            MOV   @R0,#1
CTA05       MOV   A,@R0
            MOV   B,#10
            DIV   AB
            SWAP  A
            ORL   A,#0BH
            MOV   DIGIT13,A
            MOV   A,B
            SWAP  A
```

```
            ORL   A,#07H
            MOV   DIGIT14,A
            MOV   TAMPUNG07,#2EH
            MOV   TAMPUNG06,#0DH
            MOV   TAMPUNG05,DIGIT13
            MOV   TAMPUNG04,DIGIT14

CTA06       JNB   P0.1,*      ;Switch dilepas ?
            ACALL DELAY
EscCTA      RET

;-------------------------
;     Cek Tombol Enter
;-------------------------
CTE         JB    P0.0,EscCTE       ;Cek Tombol Enter
            INC   R0
            CJNE  R0,#TAHUN+1,CTE02
            MOV   R0,#TANGGAL

CTE02       CJNE  R0,#TAHUN,CTE03
            MOV   TAMPUNG07,#2EH
            MOV   TAMPUNG06,#0DH
            MOV   TAMPUNG05,DIGIT13
            MOV   TAMPUNG04,DIGIT14
            SJMP  CTE04

CTE03       MOV   TAMPUNG07,DIGIT04
            MOV   TAMPUNG06,DIGIT03
            MOV   TAMPUNG05,DIGIT02
            MOV   TAMPUNG04,DIGIT01

CTE04       JNB   P0.0,*                    ;Switch dilepas ?
            ACALL DELAY
EscCTE      RET

;------------------------------
;     Cetak Jumlah Pemenuhan
;------------------------------
CJP         MOV   A,TAMPUNG03
            MOV   B,#10
            CLR   C
            DIV   AB
            ADD   A,#30H
            MOV   DIGIT12,A
            MOV   A,B
            ADD   A,#30H
            MOV   DIGIT11,A
EscCJP      RET

;--------------------------------
;     Pengantri Menekan Tombol
;--------------------------------
PMT         INC   TAMPUNG03
            CLR   C
            MOV   A,TAMPUNG02
            MOV   R1,TAMPUNG03
```

```
            SUBB  A,R1
            JNC   EscPMT
            DEC   TAMPUNG03
EscPMT      RET

KATA4       DB    'Antrian yang Memenuhi Panggilan',0
KATA5       DB    'Sebanyak : ',0

;-------------------------------
;     Print Jumlah Pemenuhan
;-------------------------------
PJP         ACALL BK                ;Batas Kiri
            MOV   DPTR,#KATA1
            ACALL C                 ;Cetak
            MOV   A,DIGIT04
            SWAP  A
            ANL   A,#0FH
            ACALL CH
            MOV   A,DIGIT03
            SWAP  A
            ANL   A,#0FH
            ACALL CH
            ACALL CS
            MOV   A,DIGIT02
            SWAP  A
            ANL   A,#0FH
            ACALL CH
            MOV   A,DIGIT01
            SWAP  A
            ANL   A,#0FH
            ACALL CH
            ACALL CS
            ACALL CThn

            ACALL LF                ;Line Feed
            MOV   DPTR,#KATA4
            ACALL C                 ;Cetak

            ACALL LF                ;Line Feed
            MOV   DPTR,#KATA5
            ACALL BS
            ACALL DBS
            ACALL C                 ;Cetak
            MOV   P2,DIGIT12
            ACALL STROBE
            MOV   P2,DIGIT11
            ACALL STROBE
            ACALL RESET

            MOV   R5,#5
PJP01       ACALL LF                ;Line Feed
            DJNZ  R5,PJP01
            RET

;------------------
;     Cek Tombol
```

```
;------------------
CT          JB    P0.5,S02          ;Cek tombol printer
            INC   TAMPUNG01
            ACALL CNA               ;Cetak Nomor Antrian
            ACALL PNA               ;Print Nomor Antrian
            JNB   P0.5,*            ;Switch dilepas ?
            ACALL DELAY

S02         JB    P0.4,S03          ;Cek tombol Costumer Servis 1
            ACALL DELAY
            ACALL CSMT
            MOV   DIGIT07,#17H      ;Menampilkan ruang
            MOV   DIGIT08,#0BH
            JNB   P0.4,*            ;Switch dilepas ?
            ACALL DELAY

S03         JB    P0.3,S04          ;Cek tombol Costumer Servis 2
            ACALL DELAY
            ACALL CSMT
            MOV   DIGIT07,#27H      ;Menampilkan ruang
            MOV   DIGIT08,#0BH
            JNB   P0.3,*            ;Switch dilepas ?
            ACALL DELAY

S04         JB    P3.1,S05          ;Cek tombol Pemenuhan 1
            ACALL DELAY
            ACALL PMT
            JNB   P3.1,*            ;Switch dilepas ?
            ACALL DELAY

S05         JB    P3.2,S06          ;Cek tombol Pemenuhan 2
            ACALL DELAY
            ACALL PMT
            JNB   P3.2,*            ;Switch dilepas ?
            ACALL DELAY

S06         JB    P3.3,EscCT        ;Cek tombol Cetak Jumlah
            ACALL DELAY             ;Pemenuhan
            ACALL CJP
            ACALL PJP
            JNB   P0.3,*            ;Switch dilepas ?
            ACALL DELAY

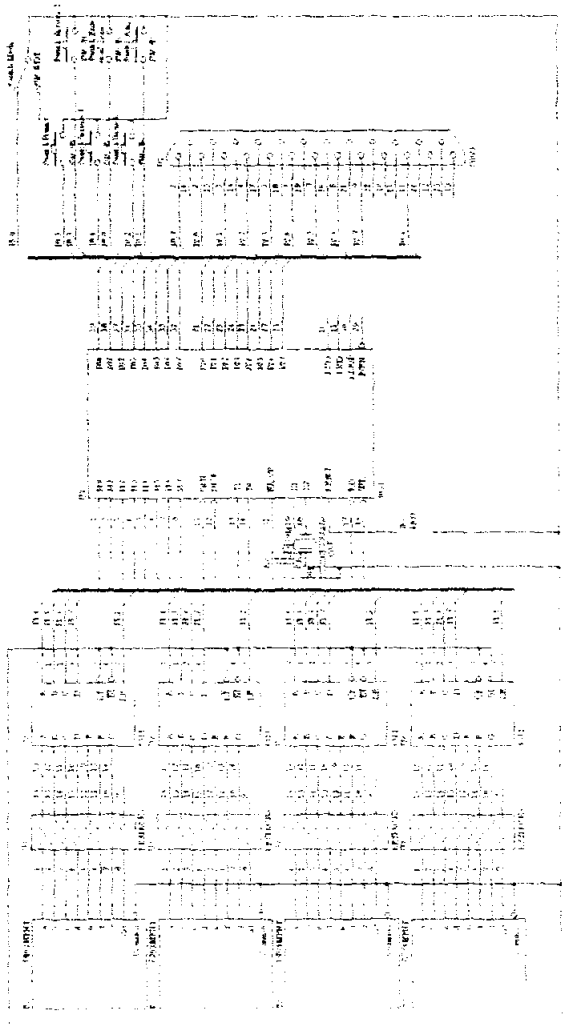
EscCT       RET

;---------------------
;     Program Utama
;---------------------
START       ACALL IA
            ACALL IP
            ACALL DELAY
            ACALL DELAY

START01     JB    P3.0,START02
            ACALL CTB
            ACALL CTA
```

```
            ACALL CTE
            ACALL SEVEN02
            SJMP  START01

START02     ACALL CT
            ACALL SEVEN
            SJMP  START01
```



MC14511B

BCD-To-Seven Segment Latch/Decoder/Driver

The MC14511B BCD–to–seven segment latch/decoder/driver is constructed with complementary MOS (CMOS) enhancement mode devices and NPN bipolar output drivers in a single monolithic structure. The circuit provides the functions of a 4–bit storage latch, an 8421 BCD–to–seven segment decoder, and an output drive capability. Lamp test ($\overline{LT}$), blanking ($\overline{BI}$), and latch enable (LE) inputs are used to test the display, to turn–off or pulse modulate the brightness of the display, and to store a BCD code, respectively. It can be used with seven–segment light–emitting diodes (LED), incandescent, fluorescent, gas discharge, or liquid crystal readouts either directly or indirectly.

Applications include instrument (e.g., counter, DVM, etc.) display driver, computer/calculator display driver, cockpit display driver, and various clock, watch, and timer uses.

- Low Logic Circuit Power Dissipation
- High–Current Sourcing Outputs (Up to 25 mA)
- Latch Storage of Code
- Blanking Input
- Lamp Test Provision
- Readout Blanking on all Illegal Input Combinations
- Lamp Intensity Modulation Capability
- Time Share (Multiplexing) Facility
- Supply Voltage Range = 3.0 V to 18 V
- Capable of Driving Two Low–power TTL Loads, One Low–power Schottky TTL Load or Two HTL Loads Over the Rated Temperature Range
- Chip Complexity: 216 FETs or 54 Equivalent Gates
- Triple Diode Protection on all Inputs

MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	– 0.5 to + 18	V
Input Voltage, All Inputs	V_{in}	– 0.5 to V_{DD} + 0.5	V
DC Current Drain per Input Pin	I	10	mA
Operating Temperature Range	T_A	– 55 to + 125	°C
Power Dissipation per Package†	P_D	500	mW
Storage Temperature Range	T_{stg}	– 65 to + 150	°C
Maximum Output Drive Current (Source) per Output	I_{OHmax}	25	mA
Maximum Continuous Output Power (Source) per Output ‡	P_{OHmax}	50	mW

‡$P_{OHmax} = I_{OH} (V_{DD} - V_{OH})$

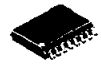
* Maximum Ratings are those values beyond which damage to the device may occur.

†Temperature Derating:
Plastic "P and D/DW" Packages: – 7.0 mW/°C From 65°C To 125°C
Ceramic "L" Packages: – 12 mW/°C From 100°C To 125°C

L SUFFIX
CERAMIC
CASE 620

P SUFFIX
PLASTIC
CASE 648

D SUFFIX
SOIC
CASE 751B



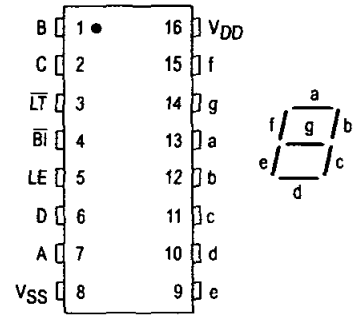
DW SUFFIX
SOIC
CASE 751G

ORDERING INFORMATION

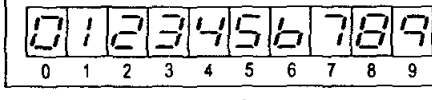
MC14XXXBCP	Plastic
MC14XXXBCL	Ceramic
MC14XXXBDW	SOIC
MC14XXXBD	SOIC

T_A = – 55° to 125°C for all packages.

PIN ASSIGNMENT



DISPLAY



TRUTH TABLE

Inputs							Outputs							
LE	BI	LT	D	C	B	A	a	b	c	d	e	f	g	Display
X	X	0	X	X	X	X	1	1	1	1	1	1	1	8
X	0	1	X	X	X	X	0	0	0	0	0	0	0	Blank
0	1	1	0	0	0	0	1	1	1	1	1	1	0	0
0	1	1	0	0	0	1	0	1	1	0	0	0	0	1
0	1	1	0	0	1	0	1	1	0	1	1	0	1	2
0	1	1	0	0	1	1	1	1	1	1	0	0	1	3
0	1	1	0	1	0	0	0	1	1	0	0	1	1	4
0	1	1	0	1	0	1	1	0	1	1	0	1	1	5
0	1	1	0	1	1	0	0	0	1	1	1	1	1	6
0	1	1	0	1	1	1	1	1	1	0	0	0	0	7
0	1	1	1	0	0	0	1	1	1	1	1	1	1	8
0	1	1	1	0	0	1	1	1	1	0	0	1	1	9
0	1	1	1	0	1	0	0	0	0	0	0	0	0	Blank
0	1	1	1	0	1	1	0	0	0	0	0	0	0	Blank
0	1	1	1	1	0	0	0	0	0	0	0	0	0	Blank
0	1	1	1	1	0	1	0	0	0	0	0	0	0	Blank
0	1	1	1	1	1	0	0	0	0	0	0	0	0	Blank
0	1	1	1	1	1	1	0	0	0	0	0	0	0	Blank
1	1	1	X	X	X	X								*

X = Don't Care
* Depends upon the BCD code previously applied when LE = 0

REV 3
1/94

ELECTRICAL CHARACTERISTICS *(Voltages Referenced to V_{SS})*

Characteristic	Symbol	V_{DD} Vdc	−55°C Min	−55°C Max	25°C Min	25°C Typ #	25°C Max	125°C Min	125°C Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
V_{in} = V_{DD} or 0		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
"1" Level	V_{OH}	5.0	4.1	—	4.1	4.57	—	4.1	—	Vdc
V_{in} = 0 or V_{DD}		10	9.1	—	9.1	9.58	—	9.1	—	
		15	14.1	—	14.1	14.59	—	14.1	—	
Input Voltage # "0" Level	V_{IL}									Vdc
(V_O = 3.8 or 0.5 Vdc)		5.0	—	1.5	—	2.25	1.5	—	1.5	
(V_O = 8.8 or 1.0 Vdc)		10	—	3.0	—	4.50	3.0	—	3.0	
(V_O = 13.8 or 1.5 Vdc)		15	—	4.0	—	6.75	4.0	—	4.0	
"1" Level	V_{IH}									Vdc
(V_O = 0.5 or 3.8 Vdc)		5.0	3.5	—	3.5	2.75	—	3.5	—	
(V_O = 1.0 or 8.8 Vdc)		10	7.0	—	7.0	5.50	—	7.0	—	
(V_O = 1.5 or 13.8 Vdc)		15	11	—	11	8.25	—	11	—	
Output Drive Voltage	V_{OH}									Vdc
(I_{OH} = 0 mA) Source		5.0	4.1	—	4.1	4.57	—	4.1	—	
(I_{OH} = 5.0 mA)			—	—	—	4.24	—	—	—	
(I_{OH} = 10 mA)			3.9	—	3.9	4.12	—	3.5	—	
(I_{OH} = 15 mA)			—	—	—	3.94	—	—	—	
(I_{OH} = 20 mA)			3.4	—	3.4	3.70	—	3.0	—	
(I_{OH} = 25 mA)			—	—	—	3.54	—	—	—	
(I_{OH} = 0 mA)		10	9.1	—	9.1	9.58	—	9.1	—	Vdc
(I_{OH} = 5.0 mA)			—	—	—	9.26	—	—	—	
(I_{OH} = 10 mA)			9.0	—	9.0	9.17	—	8.6	—	
(I_{OH} = 15 mA)			—	—	—	9.04	—	—	—	
(I_{OH} = 20 mA)			8.6	—	8.6	8.90	—	8.2	—	
(I_{OH} = 25 mA)			—	—	—	8.70	—	—	—	
(I_{OH} = 0 mA)		15	14.1	—	14.1	14.59	—	14.1	—	Vdc
(I_{OH} = 5.0 mA)			—	—	—	14.27	—	—	—	
(I_{OH} = 10 mA)			14	—	14	14.18	—	13.6	—	
(I_{OH} = 15 mA)			—	—	—	14.07	—	—	—	
(I_{OH} = 20 mA)			13.6	—	13.6	13.95	—	13.2	—	
(I_{OH} = 25 mA)			—	—	—	13.70	—	—	—	
Output Drive Current	I_{OL}									mAdc
(V_{OL} = 0.4 V) Sink		5.0	0.64	—	0.51	0.88	—	0.36	—	
(V_{OL} = 0.5 V)		10	1.6	—	1.3	2.25	—	0.9	—	
(V_{OL} = 1.5 V)		15	4.2	—	3.4	8.8	—	2.4	—	
Input Current	I_{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	µAdc
Input Capacitance	C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current	I_{DD}	5.0	—	5.0	—	0.005	5.0	—	150	µAdc
(Per Package) V_{in} = 0 or V_{DD},		10	—	10	—	0.010	10	—	300	
I_{out} = 0 µA		15	—	20	—	0.015	20	—	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (1.9 µA/kHz) f + I_{DD}							µAdc
		10	I_T = (3.8 µA/kHz) f + I_{DD}							
		15	I_T = (5.7 µA/kHz) f + I_{DD}							

#Noise immunity specified for worst–case input combination.
Noise Margin for both "1" and "0" level =
1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

**The formulas given are for the typical characteristics only at 25°C.

†To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + 3.5 \times 10^{-3} (C_L - 50) V_{DD} f$$

where: I_T is in µA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.

SWITCHING CHARACTERISTICS* (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (0.40 ns/pF) C_L + 20 ns		5.0	—	40	80	
t_{TLH} = (0.25 ns/pF) C_L + 17.5 ns		10	—	30	60	
t_{TLH} = (0.20 ns/pF) C_L + 15 ns		15	—	25	50	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 50 ns		5.0	—	125	250	
t_{THL} = (0.75 ns/pF) C_L + 37.5 ns		10	—	75	150	
t_{THL} = (0.55 ns/pF) C_L + 37.5 ns		15	—	65	130	
Data Propagation Delay Time	t_{PLH}					ns
t_{PLH} = (0.40 ns/pF) C_L + 620 ns		5.0	—	640	1280	
t_{PLH} = (0.25 ns/pF) C_L + 237.5 ns		10	—	250	500	
t_{PLH} = (0.20 ns/pF) C_L + 165 ns		15	—	175	350	
t_{PHL} = (1.3 ns/pF) C_L + 655 ns	t_{PHL}	5.0	—	720	1440	
t_{PHL} = (0.60 ns/pF) C_L + 260 ns		10	—	290	580	
t_{PHL} = (0.35 ns/pF) C_L + 182.5 ns		15	—	200	400	
$\overline{\text{Blank}}$ Propagation Delay Time	t_{PLH}					ns
t_{PLH} = (0.30 ns/pF) C_L + 585 ns		5.0	—	600	750	
t_{PLH} = (0.25 ns/pF) C_L + 187.5 ns		10	—	200	300	
t_{PLH} = (0.15 ns/pF) C_L + 142.5 ns		15	—	150	220	
t_{PHL} = (0.85 ns/pF) C_L + 442.5 ns	t_{PHL}	5.0	—	485	970	
t_{PHL} = (0.45 ns/pF) C_L + 177.5 ns		10	—	200	400	
t_{PHL} = (0.35 ns/pF) C_L + 142.5 ns		15	—	160	320	
$\overline{\text{Lamp Test}}$ Propagation Delay Time	t_{PLH}					ns
t_{PLH} = (0.45 ns/pF) C_L + 290.5 ns		5.0	—	313	625	
t_{PLH} = (0.25 ns/pF) C_L + 112.5 ns		10	—	125	250	
t_{PLH} = (0.20 ns/pF) C_L + 80 ns		15	—	90	180	
t_{PHL} = (1.3 ns/pF) C_L + 248 ns	t_{PHL}	5.0	—	313	625	
t_{PHL} = (0.45 ns/pF) C_L + 102.5 ns		10	—	125	250	
t_{PHL} = (0.35 ns/pF) C_L + 72.5 ns		15	—	90	180	
Setup Time	t_{su}	5.0	100	—	—	ns
		10	40	—	—	
		15	30	—	—	
Hold Time	t_h	5.0	60	—	—	ns
		10	40	—	—	
		15	30	—	—	
Latch Enable Pulse Width	t_{WL}	5.0	520	260	—	ns
		10	220	110	—	
		15	130	65	—	

* The formulas given are for the typical characteristics only.

This device contains protection circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit. A destructive high current mode may occur if V_{in} and V_{out} are not constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Due to the sourcing capability of this circuit, damage can occur to the device if V_{DD} is applied, and the outputs are shorted to V_{SS} and are at a logical 1 (See Maximum Ratings).

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

Input LE low, and Inputs D, $\overline{BI}$ and $\overline{LT}$ high.
f in respect to a system clock.
All outputs connected to respective C_L loads.

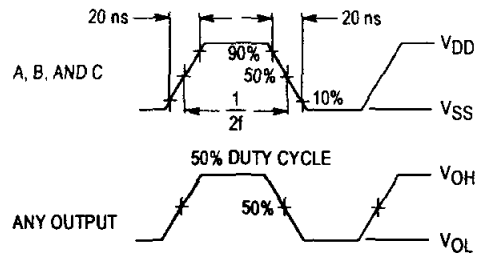
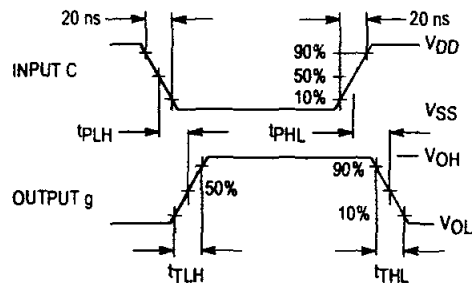
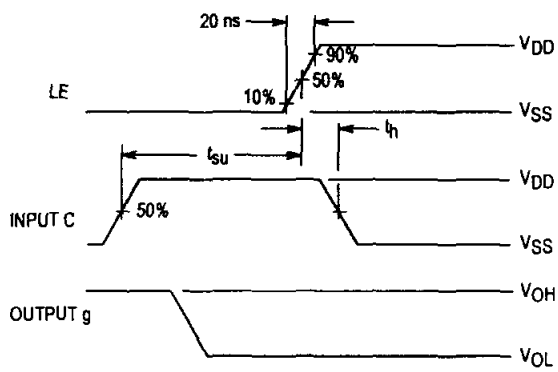


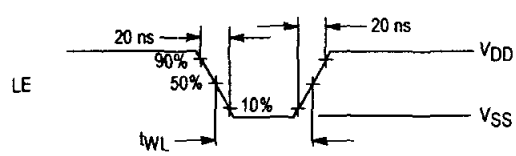
Figure 1. Dynamic Power Dissipation Signal Waveforms



(a) Inputs D and LE low, and Inputs A, B, $\overline{BI}$ and $\overline{LT}$ high.



(b) Input D low, Inputs A, B, $\overline{BI}$ and $\overline{LT}$ high.

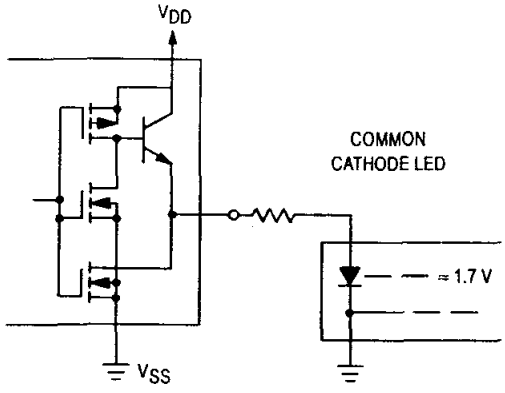


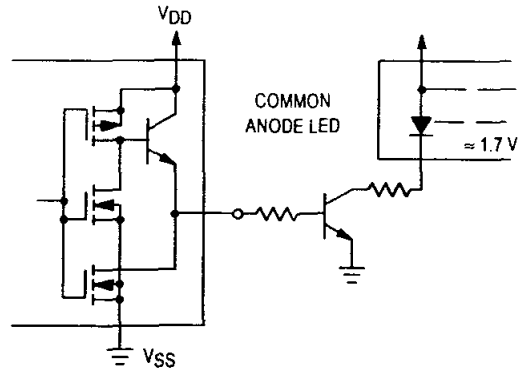
(c) Data DCBA strobed into latches.

Figure 2. Dynamic Signal Waveforms

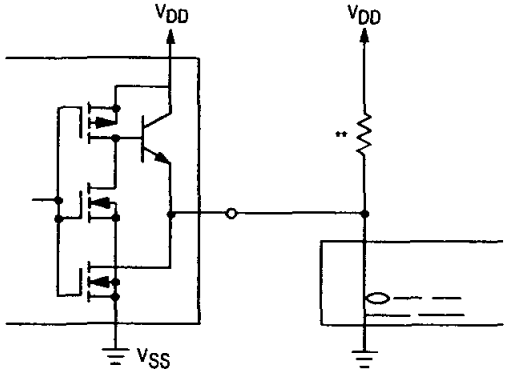
CONNECTIONS TO VARIOUS DISPLAY READOUTS

LIGHT EMITTING DIODE (LED) READOUT

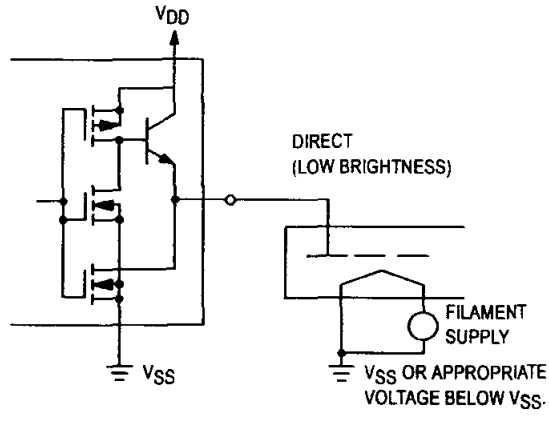




INCANDESCENT READOUT

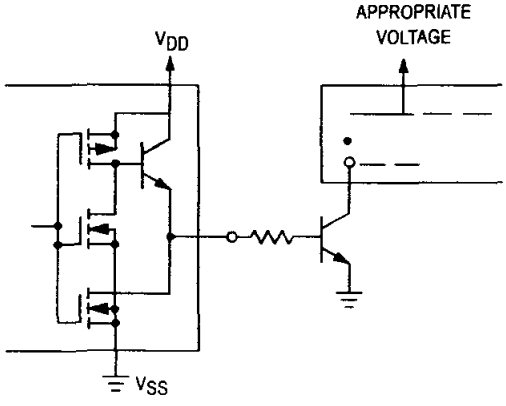


FLUORESCENT READOUT

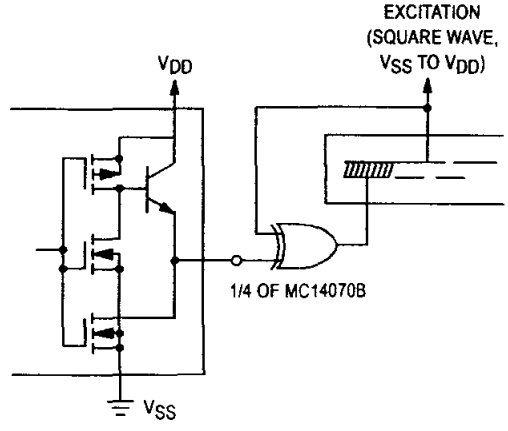


(CAUTION: Maximum working voltage = 18.0 V)

GAS DISCHARGE READOUT



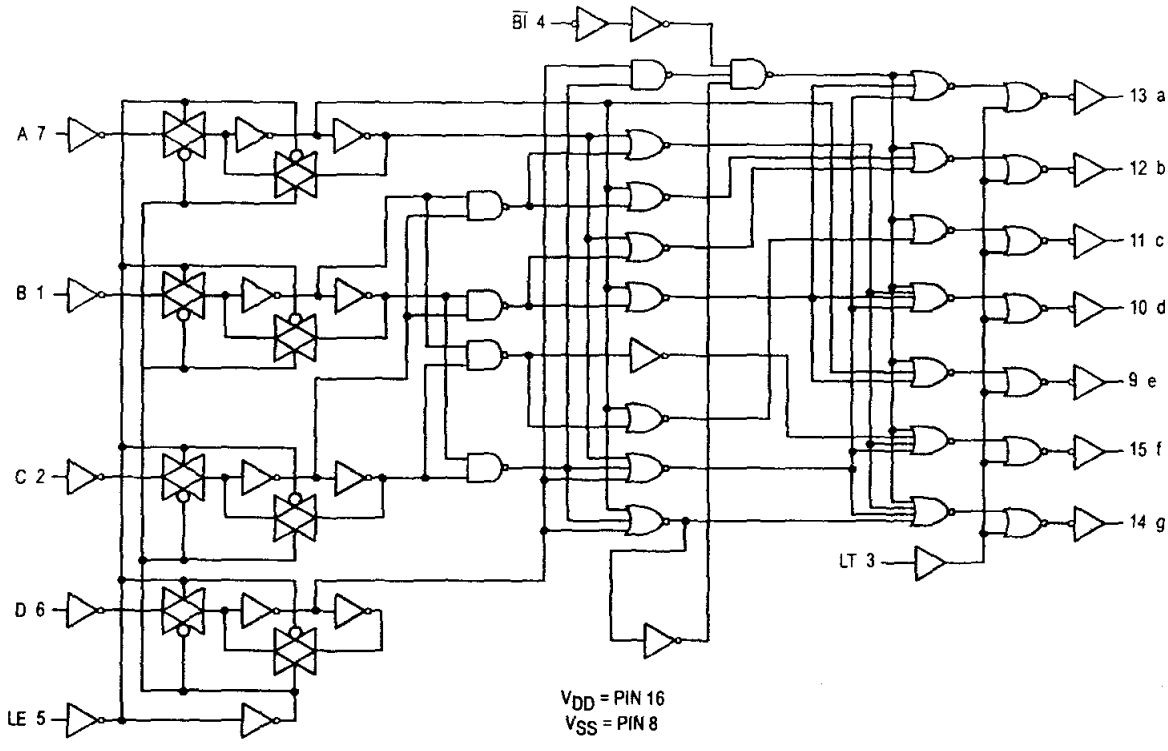
LIQUID CRYSTAL (LCD) READOUT



** A filament pre–warm resistor is recommended to reduce filament thermal shock and increase the effective cold resistance of the filament.

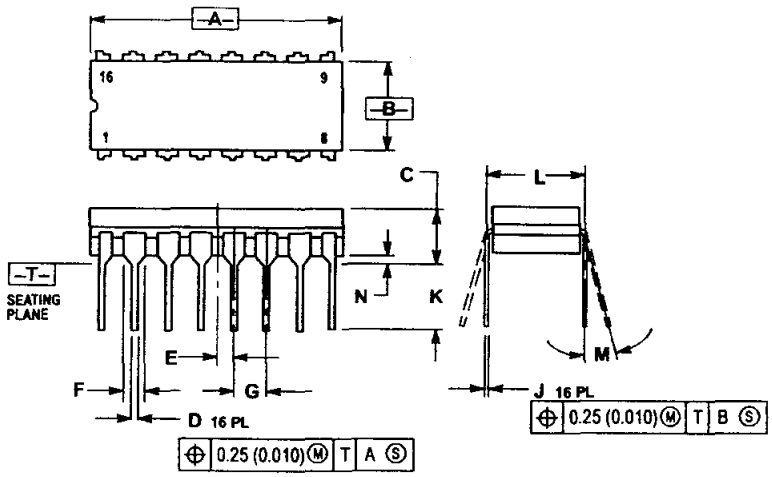
Direct dc drive of LCD's not recommended for life of LCD readouts.

LOGIC DIAGRAM



OUTLINE DIMENSIONS

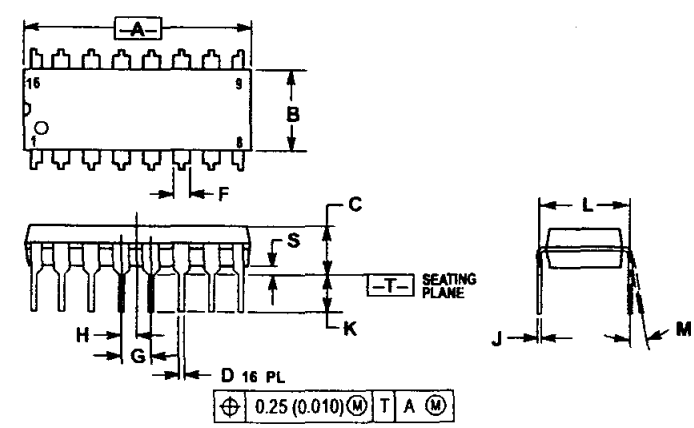
L SUFFIX
CERAMIC DIP PACKAGE
CASE 620–10
ISSUE V



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION F MAY NARROW TO 0.76 (0.030) WHERE THE LEAD ENTERS THE CERAMIC BODY.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.750	0.785	19.05	19.93
B	0.240	0.295	6.10	7.49
C	—	0.200	—	5.08
D	0.015	0.020	0.39	0.50
E	0.050 BSC		1.27 BSC	
F	0.055	0.065	1.40	1.65
G	0.100 BSC		2.54 BSC	
H	0.008	0.015	0.21	0.38
K	0.125	0.170	3.18	4.31
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

P SUFFIX
PLASTIC DIP PACKAGE
CASE 648–08
ISSUE R

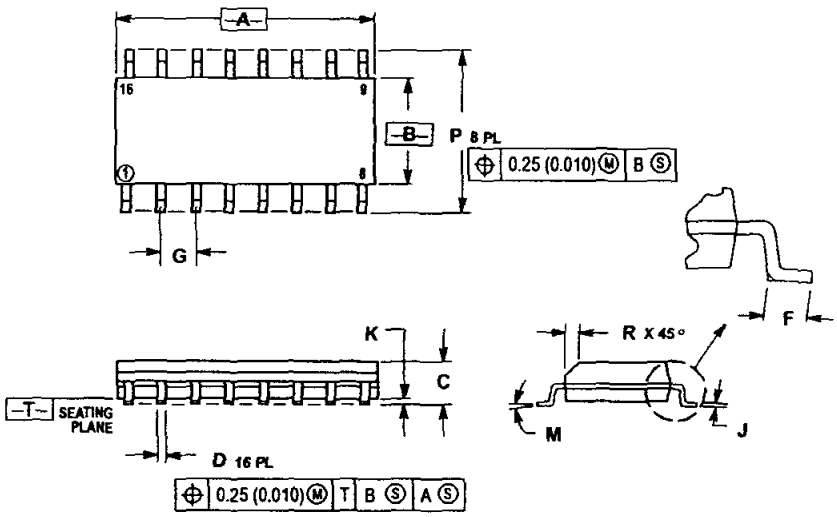


NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0°	10°	0°	10°
S	0.020	0.040	0.51	1.01

OUTLINE DIMENSIONS

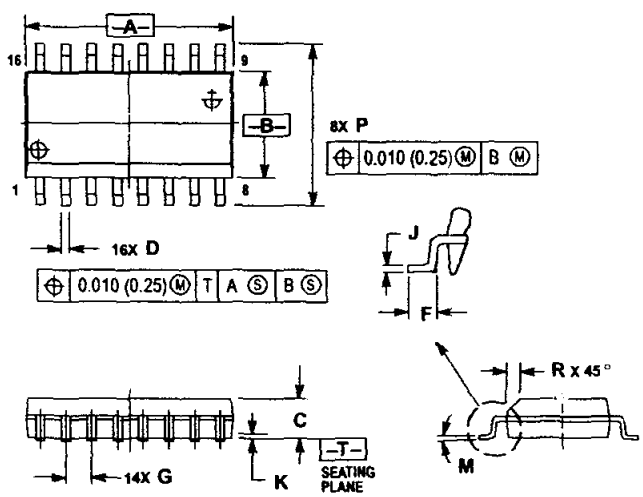
D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751B–05
ISSUE J



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

DW SUFFIX
PLASTIC SOIC PACKAGE
CASE 751G–02
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. *CONTROLLING DIMENSION: MILLIMETER.*
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	10.15	10.45	0.400	0.411
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

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ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park, 51 Ting Kok Road. Tai Po, N.T., Hong Kong. 852–26629298

Features

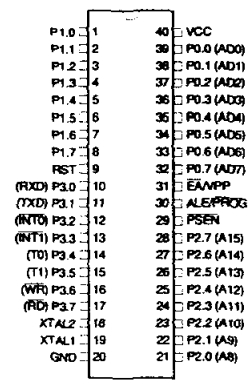
- Compatible with MCS-51™ Products
- 4K Bytes of In-System Reprogrammable Flash Memory
  - Endurance: 1,000 Write/Erase Cycles
- Fully Static Operation: 0 Hz to 24 MHz
- Three-level Program Memory Lock
- 128 x 8-bit Internal RAM
- 32 Programmable I/O Lines
- Two 16-bit Timer/Counters
- Six Interrupt Sources
- Programmable Serial Channel
- Low-power Idle and Power-down Modes

Description

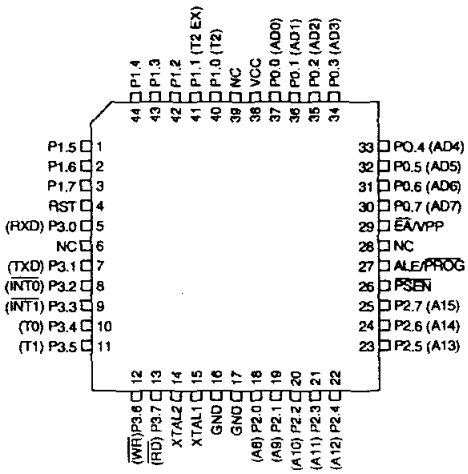
The AT89C51 is a low-power, high-performance CMOS 8-bit microcomputer with 4K bytes of Flash programmable and erasable read only memory (PEROM). The device is manufactured using Atmel's high-density nonvolatile memory technology and is compatible with the industry-standard MCS-51 instruction set and pinout. The on-chip Flash allows the program memory to be reprogrammed in-system or by a conventional nonvolatile memory programmer. By combining a versatile 8-bit CPU with Flash on a monolithic chip, the Atmel AT89C51 is a powerful microcomputer which provides a highly-flexible and cost-effective solution to many embedded control applications.

Pin Configurations

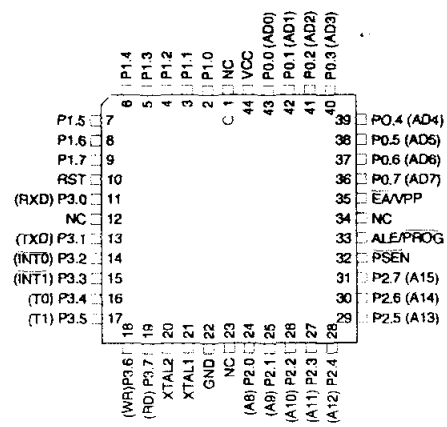
PDIP



PQFP/TQFP



PLCC

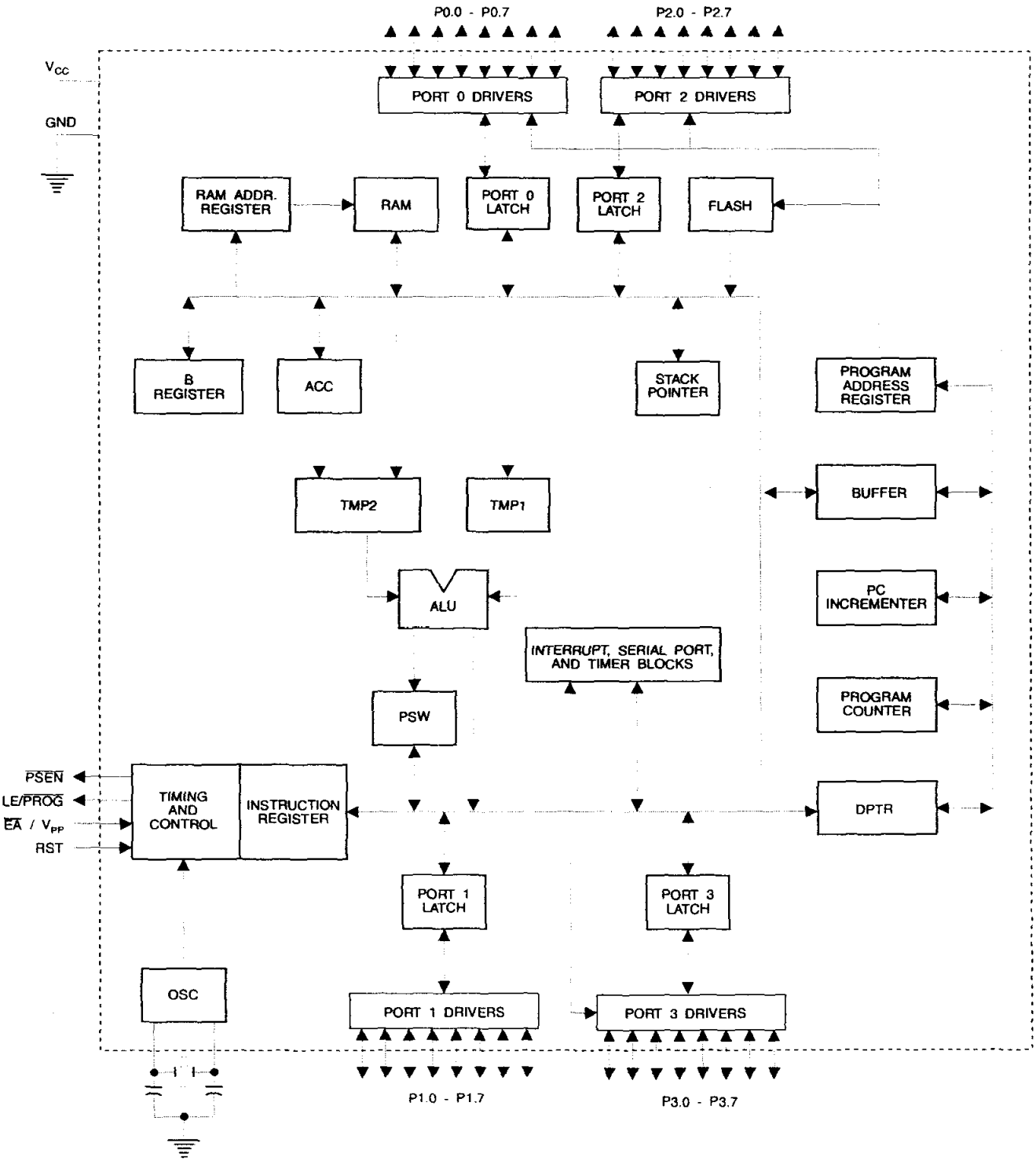


8-bit Microcontroller with 4K Bytes Flash

AT89C51

Rev. 0265G–02/00

Block Diagram



The AT89C51 provides the following standard features: 4K bytes of Flash, 128 bytes of RAM, 32 I/O lines, two 16-bit timer/counters, a five vector two-level interrupt architecture, a full duplex serial port, on-chip oscillator and clock circuitry. In addition, the AT89C51 is designed with static logic for operation down to zero frequency and supports two software selectable power saving modes. The Idle Mode stops the CPU while allowing the RAM, timer/counters, serial port and interrupt system to continue functioning. The Power-down Mode saves the RAM contents but freezes the oscillator disabling all other chip functions until the next hardware reset.

Pin Description

VCC

Supply voltage.

GND

Ground.

Port 0

Port 0 is an 8-bit open-drain bi-directional I/O port. As an output port, each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high-impedance inputs.

Port 0 may also be configured to be the multiplexed low-order address/data bus during accesses to external program and data memory. In this mode P0 has internal pullups.

Port 0 also receives the code bytes during Flash programming, and outputs the code bytes during program verification. External pullups are required during program verification.

Port 1

Port 1 is an 8-bit bi-directional I/O port with internal pullups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current (I_{IL}) because of the internal pullups.

Port 1 also receives the low-order address bytes during Flash programming and verification.

Port 2

Port 2 is an 8-bit bi-directional I/O port with internal pullups. The Port 2 output buffers can sink/source four TTL inputs. When 1s are written to Port 2 pins they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current (I_{IL}) because of the internal pullups.

Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application, it uses strong internal pullups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

Port 3

Port 3 is an 8-bit bi-directional I/O port with internal pullups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current (I_{IL}) because of the pullups.

Port 3 also serves the functions of various special features of the AT89C51 as listed below:

Port Pin	Alternate Functions
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{INT0}$ (external interrupt 0)
P3.3	$\overline{INT1}$ (external interrupt 1)
P3.4	T0 (timer 0 external input)
P3.5	T1 (timer 1 external input)
P3.6	$\overline{WR}$ (external data memory write strobe)
P3.7	$\overline{RD}$ (external data memory read strobe)

Port 3 also receives some control signals for Flash programming and verification.

RST

Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device.

ALE/$\overline{PROG}$

Address Latch Enable output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input ($\overline{PROG}$) during Flash programming.

In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that one ALE

ulse is skipped during each access to external Data lemory.

desired, ALE operation can be disabled by setting bit 0 of FR location 8EH. With the bit set, ALE is active only dur- g a MOVX or MOVC instruction. Otherwise, the pin is eakly pulled high. Setting the ALE-disable bit has no ffect if the microcontroller is in external execution mode.

SEN

rogram Store Enable is the read strobe to external pro- ram memory.

/hen the AT89C51 is executing code from external pro- ram memory, $\overline{PSEN}$ is activated twice each machine ycle, except that two $\overline{PSEN}$ activations are skipped during ach access to external data memory.

A/VPP

xternal Access Enable. $\overline{EA}$ must be strapped to GND in rder to enable the device to fetch code from external pro- ram memory locations starting at 0000H up to FFFFH. ote, however, that if lock bit 1 is programmed, $\overline{EA}$ will be ternally latched on reset.

$\overline{EA}$ should be strapped to V_{CC} for internal program xecutions.

his pin also receives the 12-volt programming enable volt- ge (V_{PP}) during Flash programming, for parts that require 2-volt V_{PP}.

TAL1

put to the inverting oscillator amplifier and input to the ternal clock operating circuit.

TAL2

utput from the inverting oscillator amplifier.

)scillator Characteristics

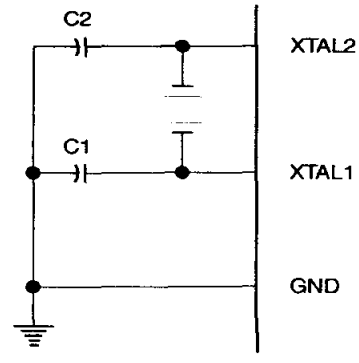
TAL1 and XTAL2 are the input and output, respectively, an inverting amplifier which can be configured for use as 1 on-chip oscillator, as shown in Figure 1. Either a quartz ystal or ceramic resonator may be used. To drive the evice from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven as shown in Figure 2. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

Idle Mode

In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special functions registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

It should be noted that when idle is terminated by a hard ware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.

Figure 1. Oscillator Connections

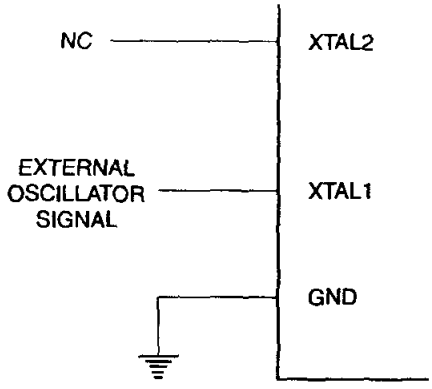


Note: C1, C2 = 30 pF ± 10 pF for Crystals
= 40 pF ± 10 pF for Ceramic Resonators

tatus of External Pins During Idle and Power-down Modes

Mode	Program Memory	ALE	$\overline{PSEN}$	PORT0	PORT1	PORT2	PORT3
dle	Internal	1	1	Data	Data	Data	Data
dle	External	1	1	Float	Data	Address	Data
ower-down	Internal	0	0	Data	Data	Data	Data
ower-down	External	0	0	Float	Data	Data	Data

Figure 2. External Clock Drive Configuration



Power-down Mode

In the power-down mode, the oscillator is stopped, and the instruction that invokes power-down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the power-down mode is terminated. The only exit from power-down is a hardware reset. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before V_{CC} is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

Program Memory Lock Bits

On the chip are three lock bits which can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in the table below.

When lock bit 1 is programmed, the logic level at the $\overline{EA}$ pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value, and holds that value until reset is activated. It is necessary that the latched value of $\overline{EA}$ be in agreement with the current logic level at that pin in order for the device to function properly.

Lock Bit Protection Modes

Program Lock Bits				
	LB1	LB2	LB3	Protection Type
1	U	U	U	No program lock features
2	P	U	U	MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, $\overline{EA}$ is sampled and latched on reset, and further programming of the Flash is disabled
3	P	P	U	Same as mode 2, also verify is disabled
4	P	P	P	Same as mode 3, also external execution is disabled

ogramming the Flash

e AT89C51 is normally shipped with the on-chip Flash mory array in the erased state (that is, contents = FFH) l ready to be programmed. The programming interface cepts either a high-voltage (12-volt) or a low-voltage $_{CC}$) program enable signal. The low-voltage program- ng mode provides a convenient way to program the 89C51 inside the user's system, while the high-voltage gramming mode is compatible with conventional third- ty Flash or EPROM programmers.

e AT89C51 is shipped with either the high-voltage or -voltage programming mode enabled. The respective -side marking and device signature codes are listed in following table.

	V_{PP} = 12V	V_{PP} = 5V
p-Side Mark	AT89C51 xxxx yyww	AT89C51 xxxx-5 yyww
gnature	(030H) = 1EH (031H) = 51H (032H) =F FH	(030H) = 1EH (031H) = 51H (032H) = 05H

e AT89C51 code memory array is programmed byte-by- e in either programming mode. *To program any non- nk byte in the on-chip Flash Memory, the entire memory st be erased using the Chip Erase Mode.*

ogramming Algorithm: Before programming the 89C51, the address, data and control signals should be up according to the Flash programming mode table and ure 3 and Figure 4. To program the AT89C51, take the owing steps.

1. Input the desired memory location on the address lines.
2. Input the appropriate data byte on the data lines.
3. Activate the correct combination of control signals.
4. Raise $\overline{EA}/V_{PP}$ to 12V for the high-voltage programming mode.
5. Pulse ALE/$\overline{PROG}$ once to program a byte in the Flash array or the lock bits. The byte-write cycle is self-timed and typically takes no more than 1.5 ms. Repeat steps 1 through 5, changing the address and data for the entire array or until the end of the object file is reached.

$\overline{Data}$ Polling: The AT89C51 features $\overline{Data}$ Polling to indicate the end of a write cycle. During a write cycle, an attempted read of the last byte written will result in the complement of the written datum on PO.7. Once the write cycle has been completed, true data are valid on all outputs, and the next cycle may begin. $\overline{Data}$ Polling may begin any time after a write cycle has been initiated.

Ready/$\overline{Busy}$: The progress of byte programming can also be monitored by the RDY/$\overline{BSY}$ output signal. P3.4 is pulled low after ALE goes high during programming to indicate BUSY. P3.4 is pulled high again when programming is done to indicate READY.

Program Verify: If lock bits LB1 and LB2 have not been programmed, the programmed code data can be read back via the address and data lines for verification. The lock bits cannot be verified directly. Verification of the lock bits is achieved by observing that their features are enabled.

Chip Erase: The entire Flash array is erased electrically by using the proper combination of control signals and by holding ALE/$\overline{PROG}$ low for 10 ms. The code array is written with all "1"s. The chip erase operation must be executed before the code memory can be re-programmed.

Reading the Signature Bytes: The signature bytes are read by the same procedure as a normal verification of locations 030H, 031H, and 032H, except that P3.6 and P3.7 must be pulled to a logic low. The values returned are as follows.

(030H) = 1EH indicates manufactured by Atmel
(031H) = 51H indicates 89C51
(032H) = FFH indicates 12V programming
(032H) = 05H indicates 5V programming

Programming Interface

Every code byte in the Flash array can be written and the entire array can be erased by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

All major programming vendors offer worldwide support for the Atmel microcontroller series. Please contact your local programming vendor for the appropriate software revision.

Flash Programming Modes

Mode		RST	PSEN	ALE/PROG	EA/V_{PP}	P2.6	P2.7	P3.6	P3.7
Write Code Data		H	L		H/12V	L	H	H	H
Read Code Data		H	L	H	H	L	L	H	H
Write Lock	Bit - 1	H	L		H/12V	H	H	H	H
	Bit - 2	H	L		H/12V	H	H	L	L
	Bit - 3	H	L		H/12V	H	L	H	L
Chip Erase		H	L	(1)	H/12V	H	L	L	L
Read Signature Byte		H	L	H	H	L	L	L	L

Note: 1. Chip Erase requires a 10 ms PROG pulse.

Figure 3. Programming the Flash

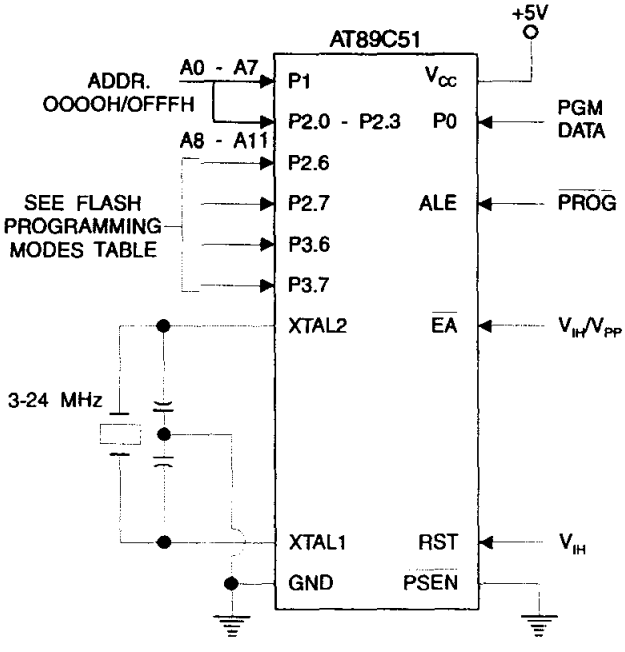
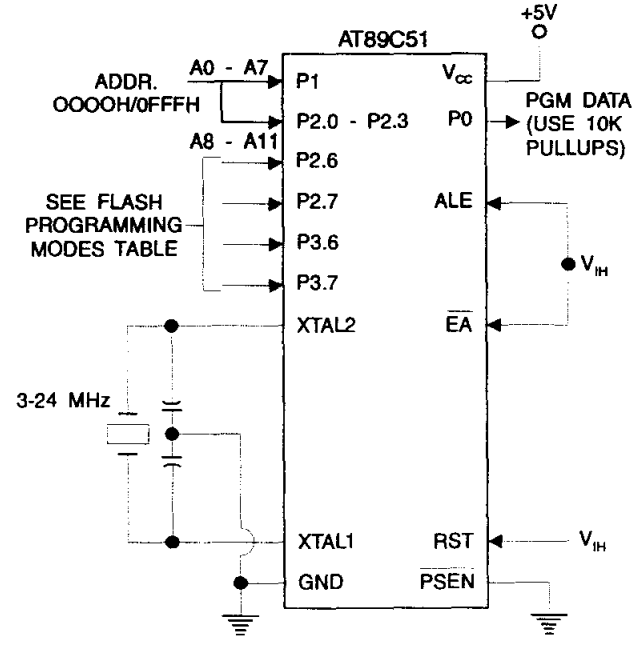
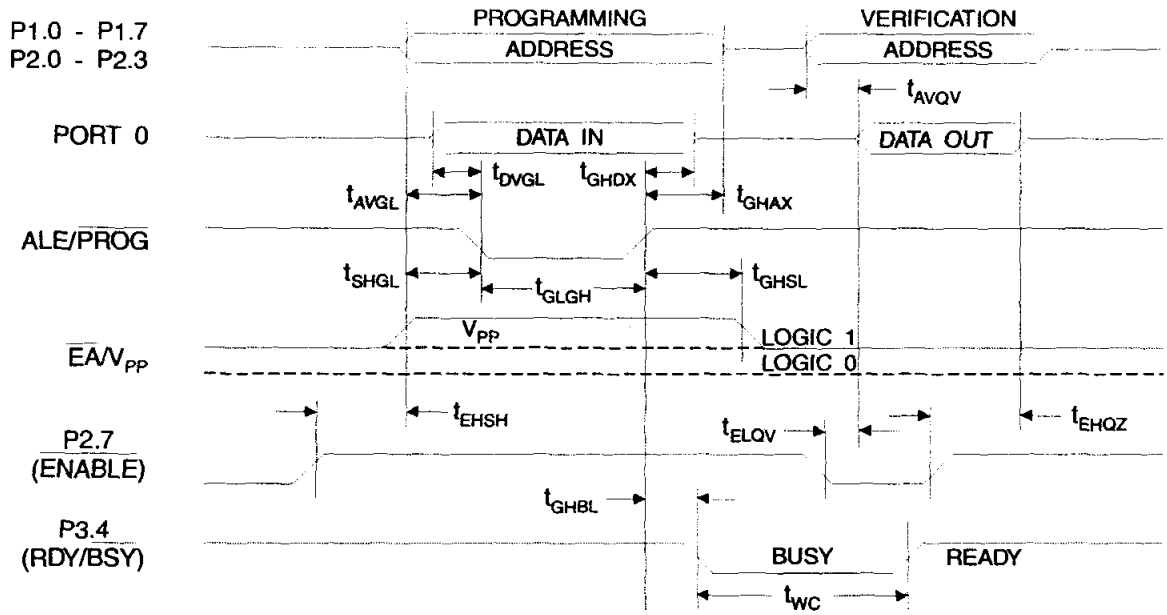


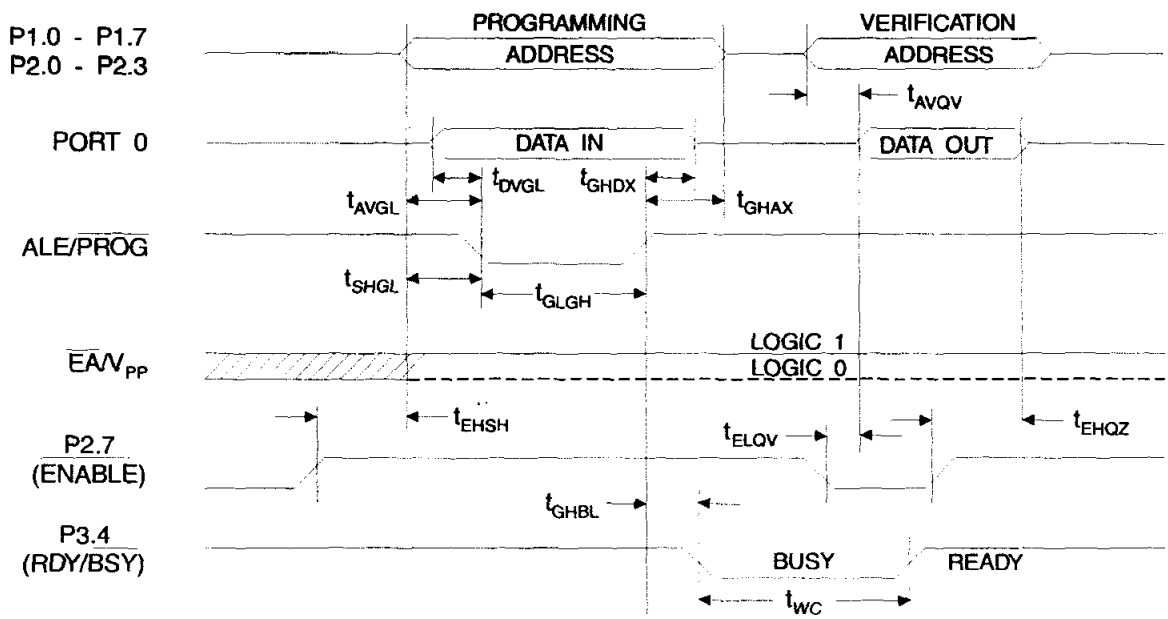
Figure 4. Verifying the Flash



Flash Programming and Verification Waveforms - High-voltage Mode (V_{PP} = 12V)



Flash Programming and Verification Waveforms - Low-voltage Mode (V_{PP} = 5V)



Flash Programming and Verification Characteristics

T_A = 0°C to 70°C, V_{CC} = 5.0 ± 10%

Symbol	Parameter	Min	Max	Units
V_{PP}[1]	Programming Enable Voltage	11.5	12.5	V
I_{PP}[1]	Programming Enable Current		1.0	mA
$1/t_{CLCL}$	Oscillator Frequency	3	24	MHz
t_{AVGL}	Address Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
t_{GHAX}	Address Hold After $\overline{PROG}$	$48t_{CLCL}$		
t_{DVGL}	Data Setup to $\overline{PROG}$ Low	$48t_{CLCL}$		
t_{GHDX}	Data Hold After $\overline{PROG}$	$48t_{CLCL}$		
t_{EHSH}	P2.7 ($\overline{ENABLE}$) High to V_{PP}	$48t_{CLCL}$		
t_{SHGL}	V_{PP} Setup to $\overline{PROG}$ Low	10		µs
t_{GHSL}[1]	V_{PP} Hold After $\overline{PROG}$	10		µs
t_{GLGH}	$\overline{PROG}$ Width	1	110	µs
t_{AVQV}	Address to Data Valid		$48t_{CLCL}$	
t_{ELQV}	$\overline{ENABLE}$ Low to Data Valid		$48t_{CLCL}$	
t_{EHQZ}	Data Float After $\overline{ENABLE}$	0	$48t_{CLCL}$	
t_{GHBL}	$\overline{PROG}$ High to $\overline{BUSY}$ Low		1.0	µs
t_{WC}	Byte Write Cycle Time		2.0	ms

Note: 1. Only used in 12-volt programming mode.

Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0V to +7.0V
Maximum Operating Voltage	6.6V
DC Output Current	15.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

T_A = -40°C to 85°C, V_{CC} = 5.0V ± 20% (unless otherwise noted)

Symbol	Parameter	Condition	Min	Max	Units
V_{IL}	Input Low-voltage	(Except $\overline{EA}$)	-0.5	0.2 V_{CC} - 0.1	V
V_{IL1}	Input Low-voltage ($\overline{EA}$)		-0.5	0.2 V_{CC} - 0.3	V
V_{IH}	Input High-voltage	(Except XTAL1, RST)	0.2 V_{CC} + 0.9	V_{CC} + 0.5	V
V_{IH1}	Input High-voltage	(XTAL1, RST)	0.7 V_{CC}	V_{CC} + 0.5	V
V_{OL}	Output Low-voltage[1] (Ports 1,2,3)	I_{OL} = 1.6 mA		0.45	V
V_{OL1}	Output Low-voltage[1] (Port 0, ALE, $\overline{PSEN}$)	I_{OL} = 3.2 mA		0.45	V
V_{OH}	Output High-voltage (Ports 1,2,3, ALE, $\overline{PSEN}$)	I_{OH} = -60 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -25 µA	0.75 V_{CC}		V
		I_{OH} = -10 µA	0.9 V_{CC}		V
V_{OH1}	Output High-voltage (Port 0 in External Bus Mode)	I_{OH} = -800 µA, V_{CC} = 5V ± 10%	2.4		V
		I_{OH} = -300 µA	0.75 V_{CC}		V
		I_{OH} = -80 µA	0.9 V_{CC}		V
I_{IL}	Logical 0 Input Current (Ports 1,2,3)	V_{IN} = 0.45V		-50	µA
I_{TL}	Logical 1 to 0 Transition Current (Ports 1,2,3)	V_{IN} = 2V, VCC = 5V ± 10%		-650	µA
I_{LI}	Input Leakage Current (Port 0, $\overline{EA}$)	0.45 < V_{IN} < V_{CC}		±10	µA
RRST	Reset Pull-down Resistor		50	300	KΩ
C_{IO}	Pin Capacitance	Test Freq. = 1 MHz, T_A = 25°C		10	pF
I_{CC}	Power Supply Current	Active Mode, 12 MHz		20	mA
		Idle Mode, 12 MHz		5	mA
	Power-down Mode[2]	V_{CC} = 6V		100	µA
		V_{CC} = 3V		40	µA

Notes: 1. Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
Maximum I_{OL} per port pin: 10 mA
Maximum I_{OL} per 8-bit port: Port 0: 26 mA
Ports 1, 2, 3: 15 mA
Maximum total I_{OL} for all output pins: 71 mA
If I_{OL} exceeds the test condition, V_{OL} may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.
2. Minimum V_{CC} for Power-down is 2V.

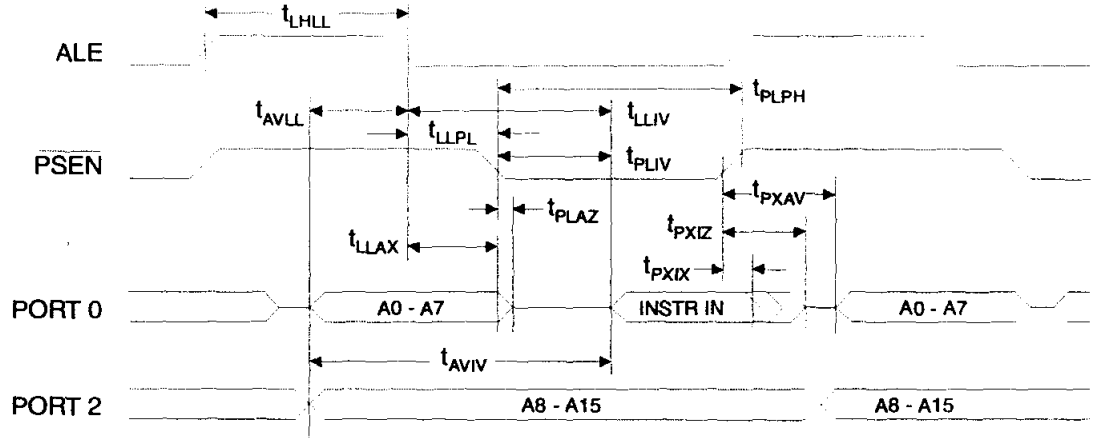
AC Characteristics

Under operating conditions, load capacitance for Port 0, ALE/$\overline{PROG}$, and $\overline{PSEN}$ = 100 pF; load capacitance for all other outputs = 80 pF.

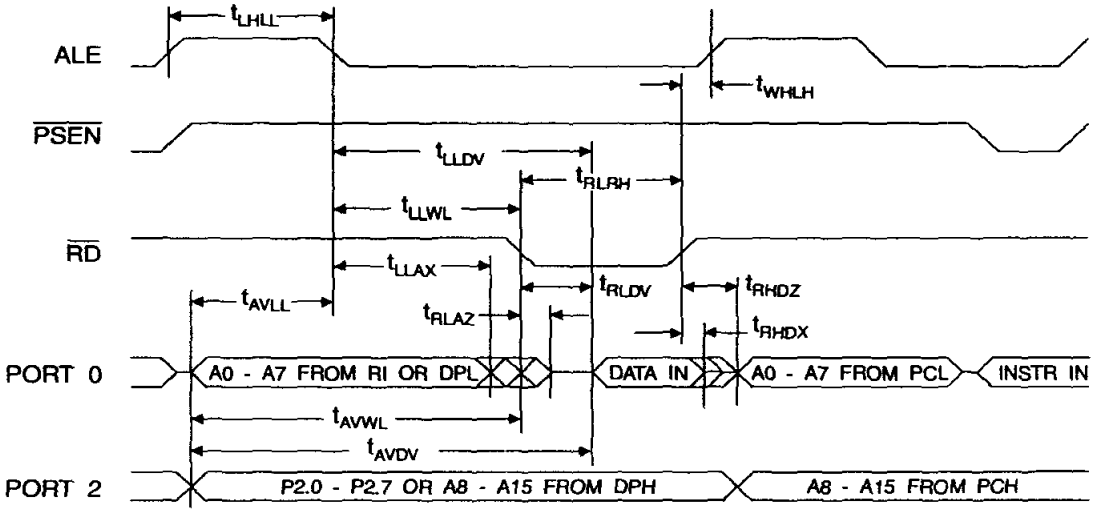
External Program and Data Memory Characteristics

Symbol	Parameter	12 MHz Oscillator		16 to 24 MHz Oscillator		Units
		Min	Max	Min	Max	
$1/t_{CLCL}$	Oscillator Frequency			0	24	MHz
t_{LHLL}	ALE Pulse Width	127		$2t_{CLCL}$-40		ns
t_{AVLL}	Address Valid to ALE Low	43		t_{CLCL}-13		ns
t_{LLAX}	Address Hold After ALE Low	48		t_{CLCL}-20		ns
t_{LLIV}	ALE Low to Valid Instruction In		233		$4t_{CLCL}$-65	ns
t_{LLPL}	ALE Low to $\overline{PSEN}$ Low	43		t_{CLCL}-13		ns
t_{PLPH}	$\overline{PSEN}$ Pulse Width	205		$3t_{CLCL}$-20		ns
t_{PLIV}	$\overline{PSEN}$ Low to Valid Instruction In		145		$3t_{CLCL}$-45	ns
t_{PXIX}	Input Instruction Hold After $\overline{PSEN}$	0		0		ns
t_{PXIZ}	Input Instruction Float After $\overline{PSEN}$		59		t_{CLCL}-10	ns
t_{PXAV}	$\overline{PSEN}$ to Address Valid	75		t_{CLCL}-8		ns
t_{AVIV}	Address to Valid Instruction In		312		$5t_{CLCL}$-55	ns
t_{PLAZ}	$\overline{PSEN}$ Low to Address Float		10		10	ns
t_{RLRH}	$\overline{RD}$ Pulse Width	400		$6t_{CLCL}$-100		ns
t_{WLWH}	$\overline{WR}$ Pulse Width	400		$6t_{CLCL}$-100		ns
t_{RLDV}	$\overline{RD}$ Low to Valid Data In		252		$5t_{CLCL}$-90	ns
t_{RHDX}	Data Hold After $\overline{RD}$	0		0		ns
t_{RHDZ}	Data Float After $\overline{RD}$		97		$2t_{CLCL}$-28	ns
t_{LLDV}	ALE Low to Valid Data In		517		$8t_{CLCL}$-150	ns
t_{AVDV}	Address to Valid Data In		585		$9t_{CLCL}$-165	ns
t_{LLWL}	ALE Low to $\overline{RD}$ or $\overline{WR}$ Low	200	300	$3t_{CLCL}$-50	$3t_{CLCL}$+50	ns
t_{AVWL}	Address to $\overline{RD}$ or $\overline{WR}$ Low	203		$4t_{CLCL}$-75		ns
t_{QVWX}	Data Valid to $\overline{WR}$ Transition	23		t_{CLCL}-20		ns
t_{QVWH}	Data Valid to $\overline{WR}$ High	433		$7t_{CLCL}$-120		ns
t_{WHQX}	Data Hold After $\overline{WR}$	33		t_{CLCL}-20		ns
t_{RLAZ}	$\overline{RD}$ Low to Address Float		0		0	ns
t_{WHLH}	$\overline{RD}$ or $\overline{WR}$ High to ALE High	43	123	t_{CLCL}-20	t_{CLCL}+25	ns

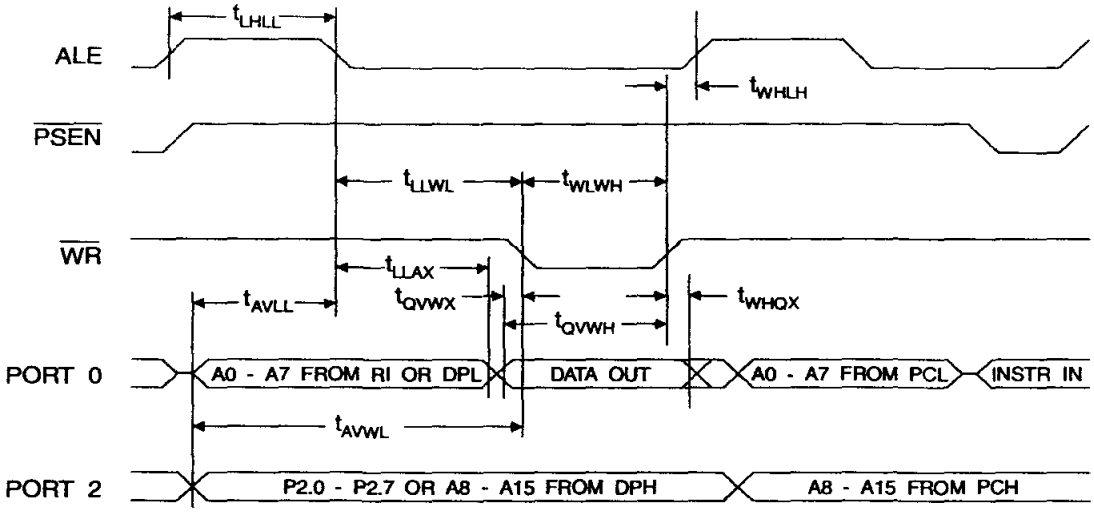
xternal Program Memory Read Cycle



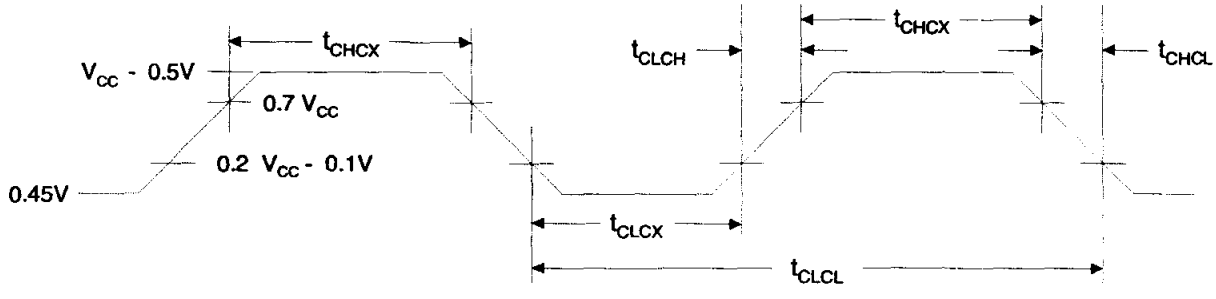
xternal Data Memory Read Cycle



External Data Memory Write Cycle



External Clock Drive Waveforms



External Clock Drive

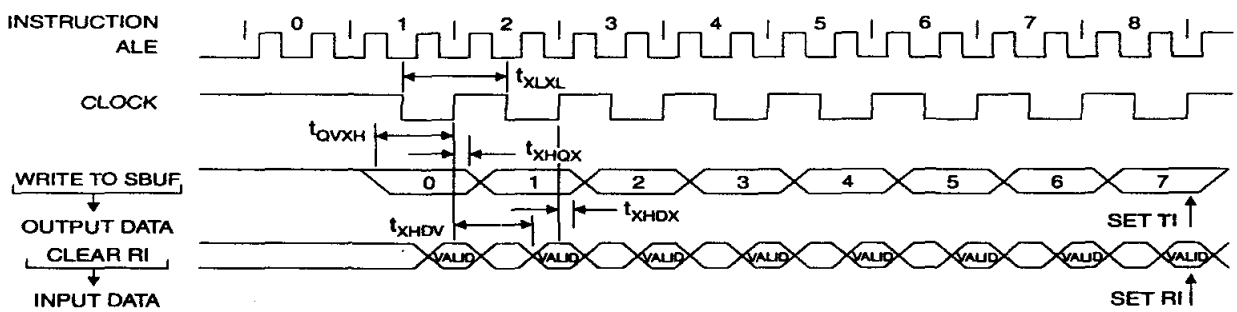
Symbol	Parameter	Min	Max	Units
$1/t_{CLCL}$	Oscillator Frequency	0	24	MHz
t_{CLCL}	Clock Period	41.6		ns
t_{CHCX}	High Time	15		ns
t_{CLCX}	Low Time	15		ns
t_{CLCH}	Rise Time		20	ns
t_{CHCL}	Fall Time		20	ns

Serial Port Timing: Shift Register Mode Test Conditions

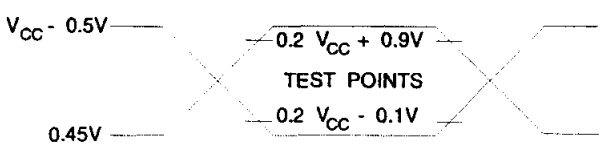
(V_{CC} = 5.0 V ± 20%; Load Capacitance = 80 pF)

Symbol	Parameter	12 MHz Osc		Variable Oscillator		Units
		Min	Max	Min	Max	
t_{XLXL}	Serial Port Clock Cycle Time	1.0		$12t_{CLCL}$		µs
t_{QVXH}	Output Data Setup to Clock Rising Edge	700		$10t_{CLCL}$-133		ns
t_{XHQX}	Output Data Hold After Clock Rising Edge	50		$2t_{CLCL}$-117		ns
t_{XHDX}	Input Data Hold After Clock Rising Edge	0		0		ns
t_{XHDV}	Clock Rising Edge to Input Data Valid		700		$10t_{CLCL}$-133	ns

Shift Register Mode Timing Waveforms

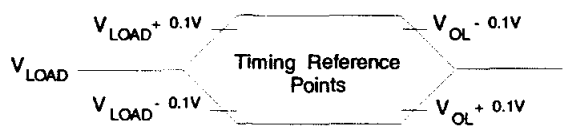


AC Testing Input/Output Waveforms[1]



Note: 1. AC Inputs during testing are driven at V_{CC} - 0.5V for a logic 1 and 0.45V for a logic 0. Timing measurements are made at V_{IH} min. for a logic 1 and V_{IL} max. for a logic 0.

Float Waveforms[1]



Note: 1. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when 100 mV change from the loaded V_{OH}/V_{OL} level occurs.

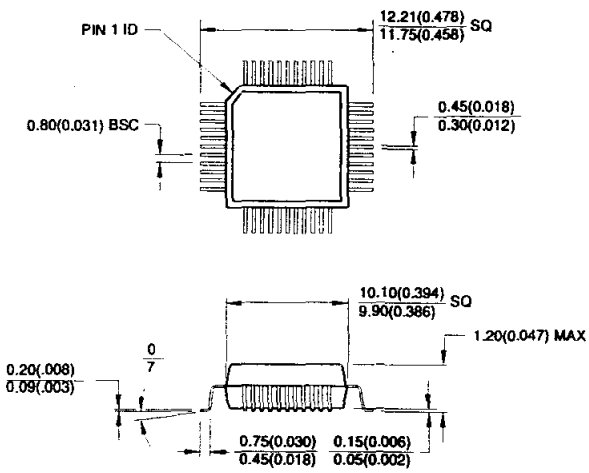
Ordering Information

Speed (MHz)	Power Supply	Ordering Code	Package	Operation Range
12	5V ± 20%	AT89C51-12AC	44A	Commercial
		AT89C51-12JC	44J	(0°C to 70°C)
		AT89C51-12PC	40P6	
		AT89C51-12QC	44Q	
		AT89C51-12AI	44A	Industrial
		AT89C51-12JI	44J	(-40°C to 85°C)
		AT89C51-12PI	40P6	
		AT89C51-12QI	44Q	
16	5V ± 20%	AT89C51-16AC	44A	Commercial
		AT89C51-16JC	44J	(0°C to 70°C)
		AT89C51-16PC	40P6	
		AT89C51-16QC	44Q	
		AT89C51-16AI	44A	Industrial
		AT89C51-16JI	44J	(-40°C to 85°C)
		AT89C51-16PI	40P6	
		AT89C51-16QI	44Q	
20	5V ± 20%	AT89C51-20AC	44A	Commercial
		AT89C51-20JC	44J	(0°C to 70°C)
		AT89C51-20PC	40P6	
		AT89C51-20QC	44Q	
		AT89C51-20AI	44A	Industrial
		AT89C51-20JI	44J	(-40°C to 85°C)
		AT89C51-20PI	40P6	
		AT89C51-20QI	44Q	
24	5V ± 20%	AT89C51-24AC	44A	Commercial
		AT89C51-24JC	44J	(0°C to 70°C)
		AT89C51-24PC	40P6	
		AT89C51-24QC	44Q	
		AT89C51-24AI	44A	Industrial
		AT89C51-24JI	44J	(-40°C to 85°C)
		AT89C51-24PI	40P6	
		AT89C51-24QI	44Q	

Package Type	
44A	44-lead, Thin Plastic Gull Wing Quad Flatpack (TQFP)
44J	44-lead, Plastic J-leaded Chip Carrier (PLCC)
40P6	40-lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
44Q	44-lead, Plastic Gull Wing Quad Flatpack (PQFP)

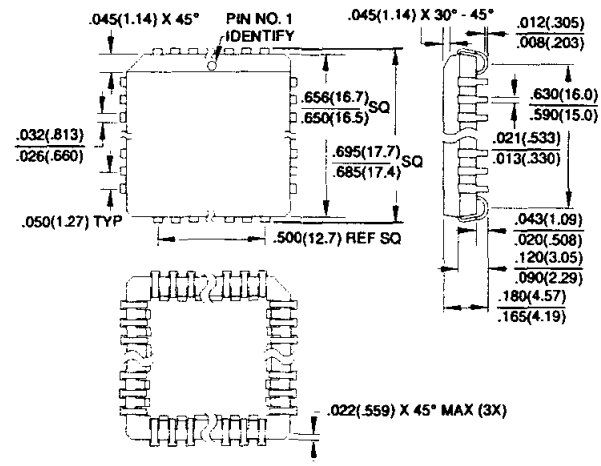
Packaging Information

44A, 44-lead, Thin (1.0 mm) Plastic Gull Wing Quad Flatpack (TQFP)
Dimensions in Millimeters and (Inches)*
JEDEC STANDARD MS-026 ACB

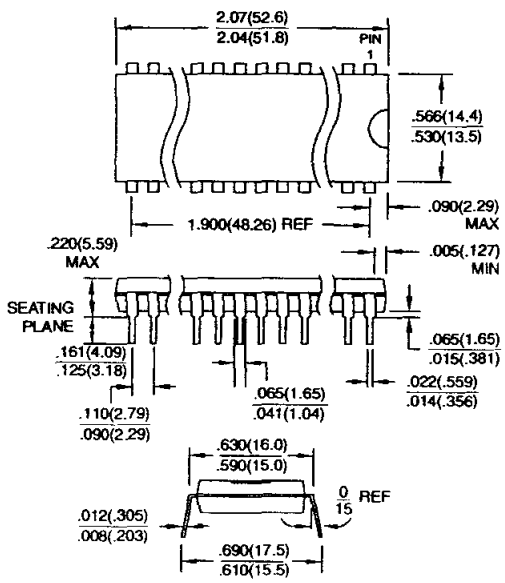


Controlling dimension: millimeters

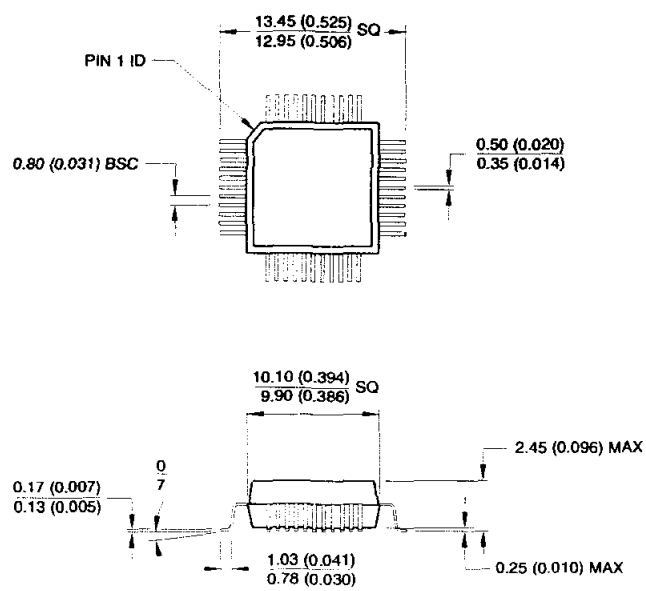
44J, 44-lead, Plastic J-leaded Chip Carrier (PLCC)
Dimensions in Inches and (Millimeters)
JEDEC STANDARD MS-018 AC



40P6, 40-lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
Dimensions in Inches and (Millimeters)



44Q, 44-lead, Plastic Quad Flat Package (PQFP)
Dimensions in Millimeters and (Inches)*
JEDEC STANDARD MS-022 AB



Controlling dimension: millimeters

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