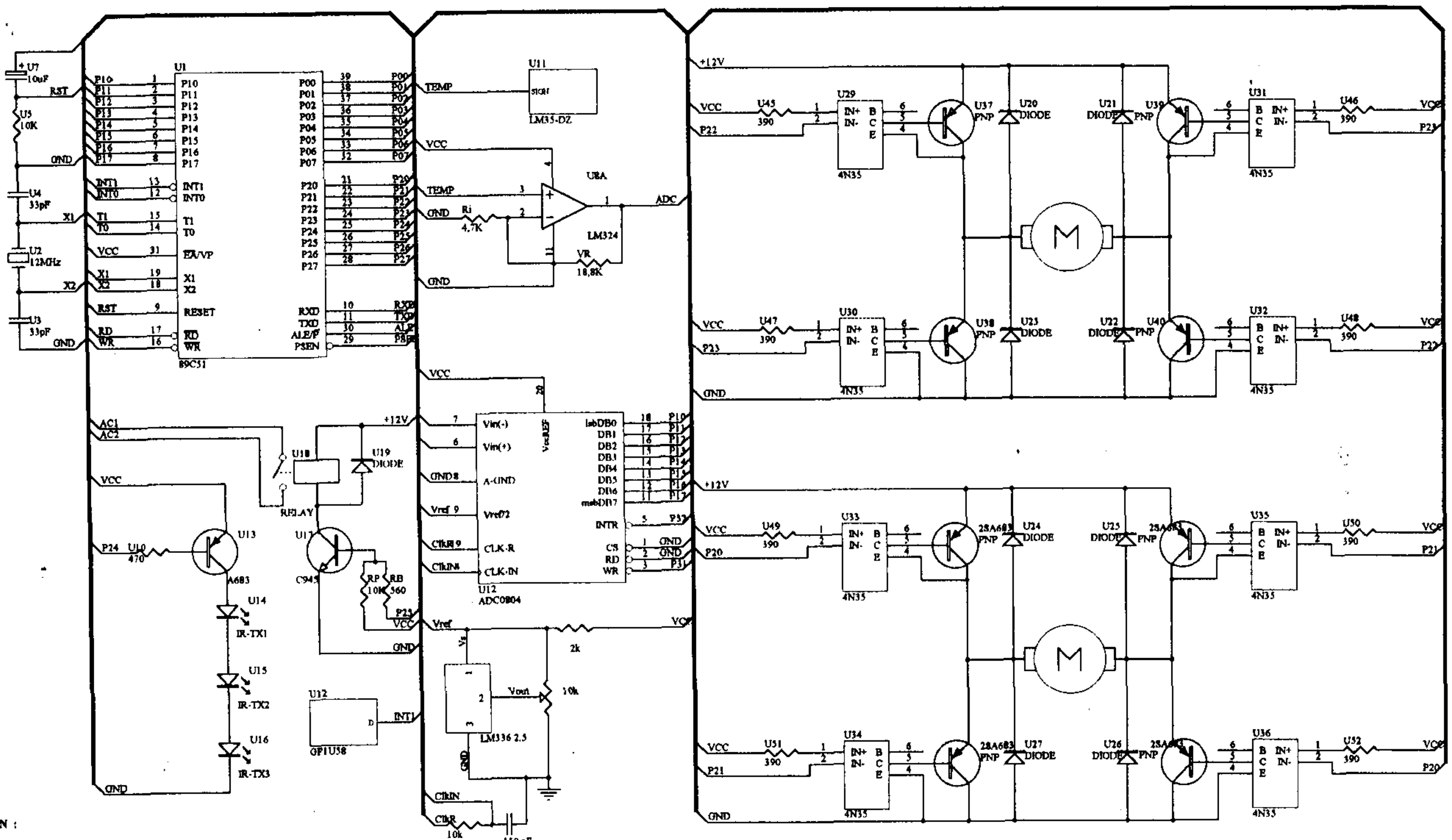
# LAMPIRAN A




**KETERANGAN :**

Rangkaian di atas terdiri atas beberapa bagian yaitu :

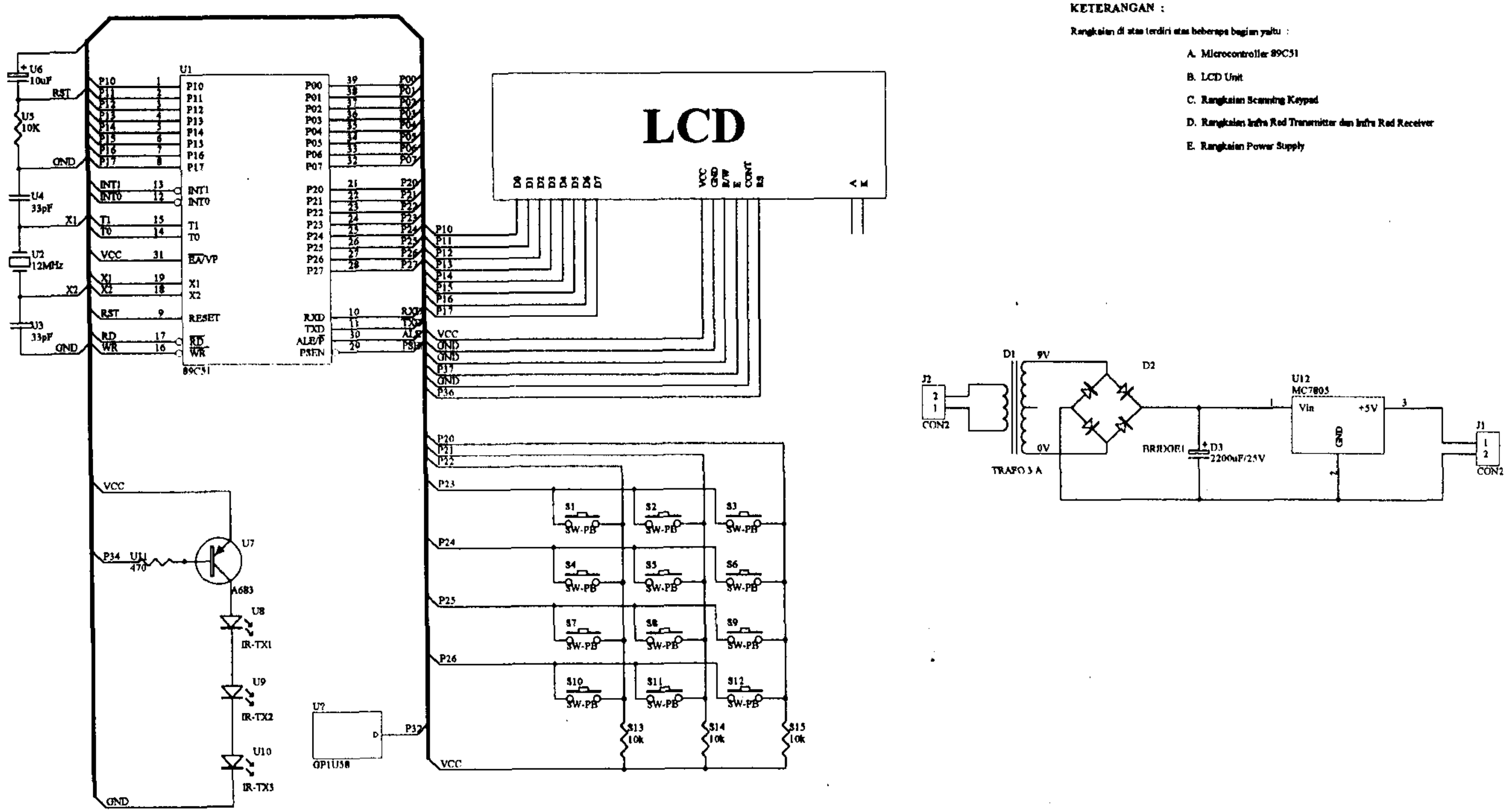
A. Microcontroller 89C51

B. Sensor Suhu LM35 beserta Rangkaian Pengkondisi Signal (RPS) s/d ADC 0804

C. Rangkaian Infra Red Transmitter dan Infra Red Receiver

D. Rangkaian H-Bridge Driver Motor untuk Low Valve dan High Valve

| Title | | | |
|---|---|---|---|
| **Rangkaian Unit Tangki** | | | |
| Size: B | Number: HR/01/08/2001 | | Revision: OK |
| Date: 2-Oct-2001 | | Sheet of 1 | |
| File: D:\Pao\dataset\TA_Hartono.sch | | Drawn By: - | |




**KETERANGAN :**

Rangkaian di atas terdiri atas beberapa bagian yaitu :

A. Microcontroller 89C51

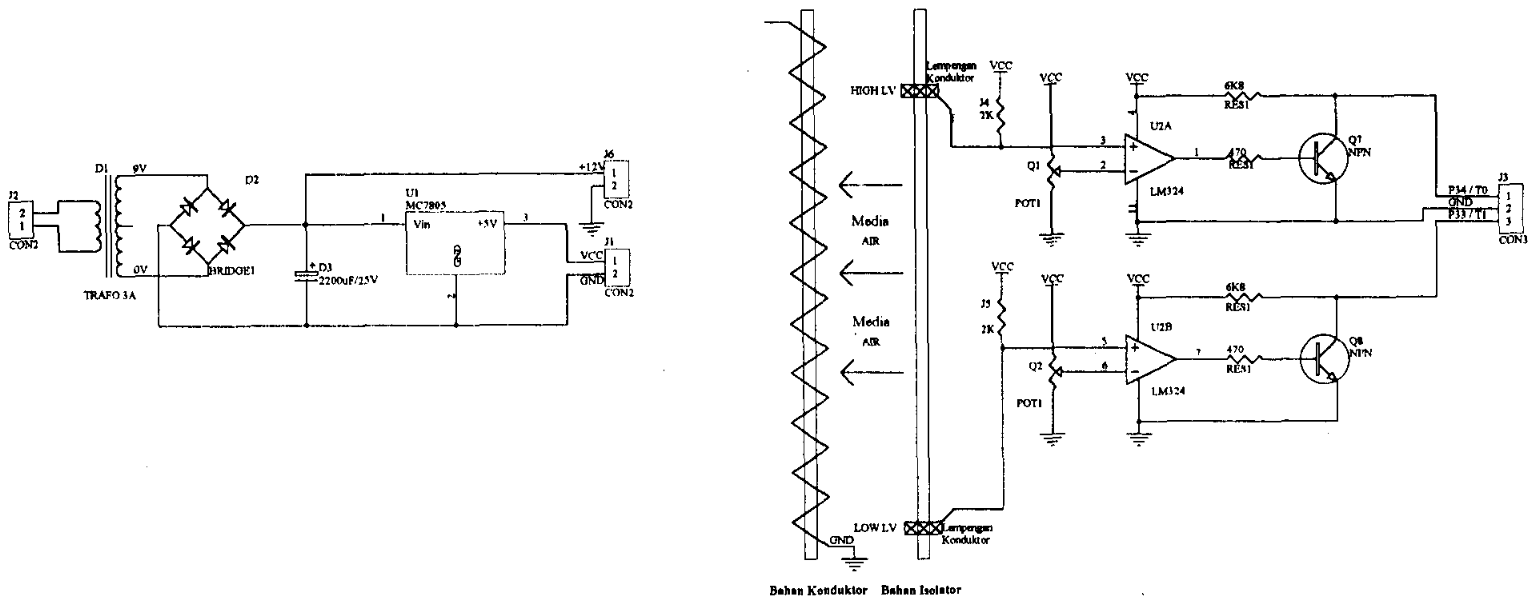
B. LCD Unit

C. Rangkaian Scanning Keypad

D. Rangkaian Infra Red Transmitter dan Infra Red Receiver

E. Rangkaian Power Supply

| | | | |
|---|---|---|---|
| Title | Rangkaian Unit Pemantau & Pengendali | | |
| Size B | Number HR/03/08/2001 | | Revision OK |
| Date: | 2-Oct-2001 | Sheet of 3 | |
| File: | D:\Pao\dataset\TA_Hartono3.sch | Drawn By: - | |




**KETERANGAN :**

Rangkaian di atas terdiri atas beberapa bagian yaitu :

A. Rangkaian Power Supply

B. Rangkaian Sensor Level ( Limit Sensor)

| Title | Rangkaian Limit Switch | | |
|---|---|---|---|
| Size: B | Number: HR/02/08/2001 | | Revision: OK |
| Date: | 8-Oct-2001 | Sheet | of 2 |
| File: | D:\Pao\dataseet\TA_Hartono2.sch | Drawn By: | - |

## Features

- **_Compatible with MCS-51™ Products_**
- **4K Bytes of In-System Reprogrammable Flash Memory**
  - **Endurance: 1,000 Write/Erase Cycles**
- **Fully Static Operation: 0 Hz to 24 MHz**
- **Three-Level Program Memory Lock**
- **128 x 8-Bit Internal RAM**
- **32 Programmable I/O Lines**
- **Two 16-Bit Timer/Counters**
- **Six Interrupt Sources**
- **Programmable Serial Channel**
- **Low Power Idle and Power Down Modes**

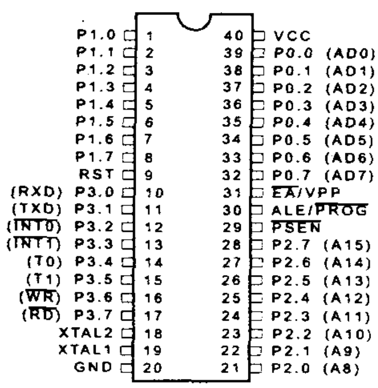
## Description

The AT89C51 is a low-power, high-performance CMOS 8-bit microcomputer with 4K bytes of Flash Programmable and Erasable Read Only Memory (PEROM). The device is manufactured using Atmel's high density nonvolatile memory technology and is compatible with the industry standard MCS-51™ instruction set and pinout. The on-chip Flash allows the program memory to be reprogrammed in-system or by a conventional nonvolatile memory programmer. By combining a versatile 8-bit CPU with Flash on a monolithic chip, the Atmel AT89C51 is a powerful microcomputer which provides a highly flexible and cost effective solution to many embedded control applications.

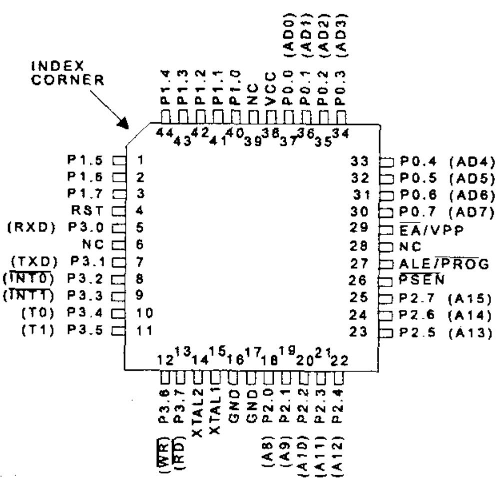
*(continued)*

## Pin Configurations

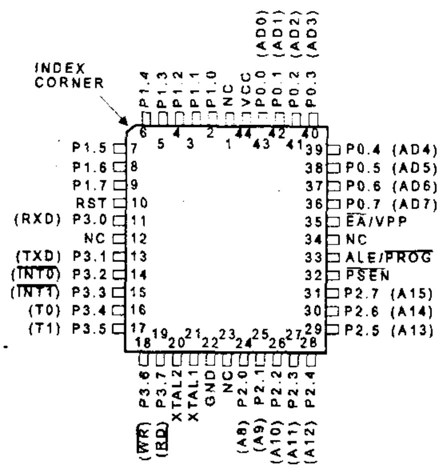
PDIP




PQFP/TQFP




PLCC

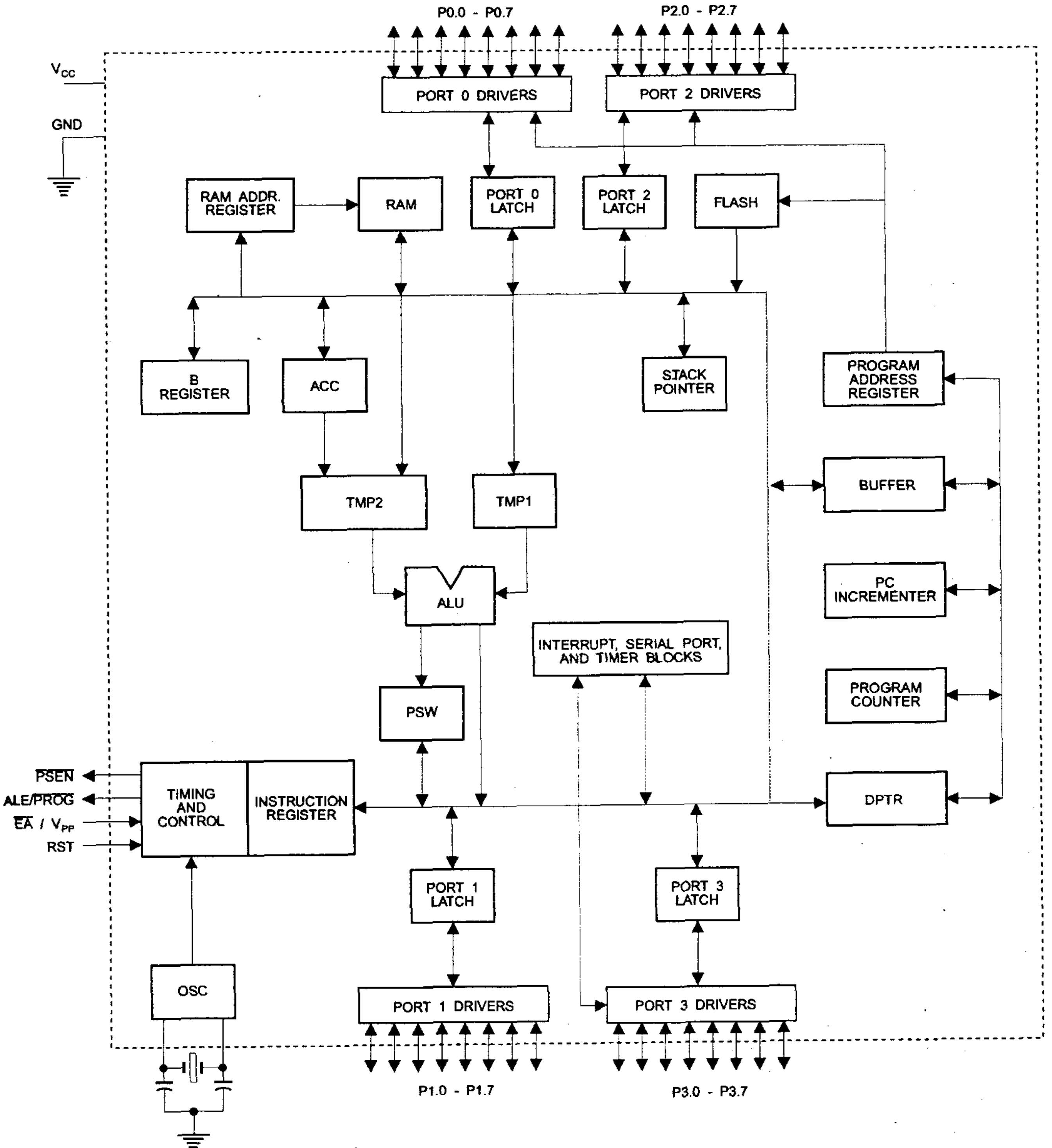



# 8-Bit Microcontroller with 4K Bytes Flash

# AT89C51

0265F-A-12/97

## Block Diagram



The AT89C51 provides the following standard features: 4K bytes of Flash, 128 bytes of RAM, 32 I/O lines, two 16-bit timer/counters, a five vector two-level interrupt architecture, a full duplex serial port, on-chip oscillator and clock circuitry. In addition, the AT89C51 is designed with static logic for operation down to zero frequency and supports two software selectable power saving modes. The Idle Mode stops the CPU while allowing the RAM, timer/counters, serial port and interrupt system to continue functioning. The Power Down Mode saves the RAM contents but freezes the oscillator disabling all other chip functions until the next hardware reset.

## Pin Description

**$V_{CC}$**

Supply voltage.

**GND**

Ground.

**Port 0**

Port 0 is an 8-bit open drain bidirectional I/O port. As an output port each pin can sink eight TTL inputs. When 1s are written to port 0 pins, the pins can be used as high-impedance inputs.

Port 0 may also be configured to be the multiplexed low-order address/data bus during accesses to external program and data memory. In this mode P0 has internal pullups.

Port 0 also receives the code bytes during Flash programming, and outputs the code bytes during program verification. External pullups are required during program verification.

**Port 1**

Port 1 is an 8-bit bidirectional I/O port with internal pullups. The Port 1 output buffers can sink/source four TTL inputs. When 1s are written to Port 1 pins they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 1 pins that are externally being pulled low will source current ($I_{IL}$) because of the internal pullups.

Port 1 also receives the low-order address bytes during Flash programming and verification.

**Port 2**

Port 2 is an 8-bit bidirectional I/O port with internal pullups. The Port 2 output buffers can sink/source four TTL inputs. When 1s are written to Port 2 pins they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 2 pins that are externally being pulled low will source current ($I_{IL}$) because of the internal pullups.

Port 2 emits the high-order address byte during fetches from external program memory and during accesses to external data memory that use 16-bit addresses (MOVX @ DPTR). In this application it uses strong internal pullups when emitting 1s. During accesses to external data memory that use 8-bit addresses (MOVX @ RI), Port 2 emits the contents of the P2 Special Function Register.

Port 2 also receives the high-order address bits and some control signals during Flash programming and verification.

**Port 3**

Port 3 is an 8-bit bidirectional I/O port with internal pullups. The Port 3 output buffers can sink/source four TTL inputs. When 1s are written to Port 3 pins they are pulled high by the internal pullups and can be used as inputs. As inputs, Port 3 pins that are externally being pulled low will source current ($I_{IL}$) because of the pullups.

Port 3 also serves the functions of various special features of the AT89C51 as listed below:

| Port Pin | Alternate Functions |
|---|---|
| P3.0 | RXD (serial input port) |
| P3.1 | TXD (serial output port) |
| P3.2 | $\overline{\text{INT0}}$ (external interrupt 0) |
| P3.3 | $\overline{\text{INT1}}$ (external interrupt 1) |
| P3.4 | T0 (timer 0 external input) |
| P3.5 | T1 (timer 1 external input) |
| P3.6 | $\overline{\text{WR}}$ (external data memory write strobe) |
| P3.7 | $\overline{\text{RD}}$ (external data memory read strobe) |

Port 3 also receives some control signals for Flash programming and verification.

**RST**

Reset input. A high on this pin for two machine cycles while the oscillator is running resets the device.

**ALE/$\overline{\text{PROG}}$**

Address Latch Enable output pulse for latching the low byte of the address during accesses to external memory. This pin is also the program pulse input ($\overline{\text{PROG}}$) during Flash programming.

In normal operation ALE is emitted at a constant rate of 1/6 the oscillator frequency, and may be used for external timing or clocking purposes. Note, however, that one ALE pulse is skipped during each access to external Data Memory.

If desired, ALE operation can be disabled by setting bit 0 of SFR location 8EH. With the bit set, ALE is active only during a MOVX or MOVC instruction. Otherwise, the pin is weakly pulled high. Setting the ALE-disable bit has no effect if the microcontroller is in external execution mode.

**$\overline{\text{PSEN}}$**

Program Store Enable is the read strobe to external program memory.

When the AT89C51 is executing code from external program memory, $\overline{PSEN}$ is activated twice each machine cycle, except that two $\overline{PSEN}$ activations are skipped during each access to external data memory.

**$\overline{EA}/V_{PP}$**

External Access Enable. $\overline{EA}$ must be strapped to GND in order to enable the device to fetch code from external program memory locations starting at 0000H up to FFFFH. Note, however, that if lock bit 1 is programmed, $\overline{EA}$ will be internally latched on reset.

$\overline{EA}$ should be strapped to $V_{CC}$ for internal program executions.

This pin also receives the 12-volt programming enable voltage ($V_{PP}$) during Flash programming, for parts that require 12-volt $V_{PP}$.

**XTAL1**

Input to the inverting oscillator amplifier and input to the internal clock operating circuit.

**XTAL2**

Output from the inverting oscillator amplifier.

## Oscillator Characteristics

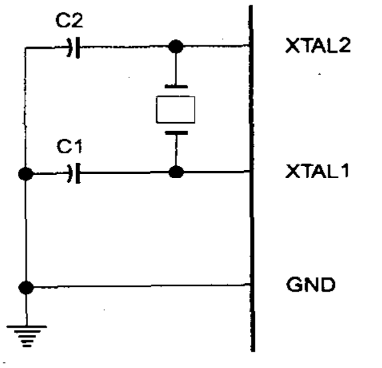
XTAL1 and XTAL2 are the input and output, respectively, of an inverting amplifier which can be configured for use as an on-chip oscillator, as shown in Figure 1. Either a quartz crystal or ceramic resonator may be used. To drive the device from an external clock source, XTAL2 should be left unconnected while XTAL1 is driven as shown in Figure 2. There are no requirements on the duty cycle of the external clock signal, since the input to the internal clocking circuitry is through a divide-by-two flip-flop, but minimum and maximum voltage high and low time specifications must be observed.

## Idle Mode

In idle mode, the CPU puts itself to sleep while all the on-chip peripherals remain active. The mode is invoked by software. The content of the on-chip RAM and all the special functions registers remain unchanged during this mode. The idle mode can be terminated by any enabled interrupt or by a hardware reset.

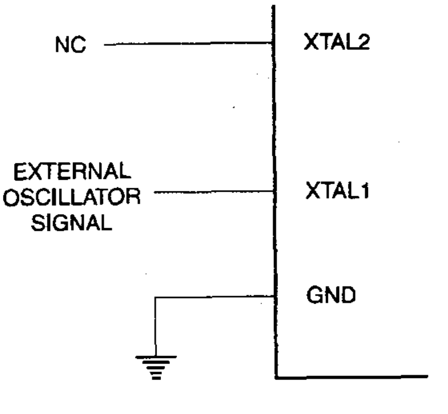
It should be noted that when idle is terminated by a hard ware reset, the device normally resumes program execution, from where it left off, up to two machine cycles before the internal reset algorithm takes control. On-chip hardware inhibits access to internal RAM in this event, but access to the port pins is not inhibited. To eliminate the possibility of an unexpected write to a port pin when Idle is terminated by reset, the instruction following the one that invokes Idle should not be one that writes to a port pin or to external memory.

**Figure 1.** Oscillator Connections




Note: C1, C2 = 30 pF ± 10 pF for Crystals
= 40 pF ± 10 pF for Ceramic Resonators

**Figure 2.** External Clock Drive Configuration




## Status of External Pins During Idle and Power Down Modes

| Mode | Program Memory | ALE | $\overline{PSEN}$ | PORT0 | PORT1 | PORT2 | PORT3 |
|---|---|---|---|---|---|---|---|
| Idle | Internal | 1 | 1 | Data | Data | Data | Data |
| Idle | External | 1 | 1 | Float | Data | Address | Data |
| Power Down | Internal | 0 | 0 | Data | Data | Data | Data |
| Power Down | External | 0 | 0 | Float | Data | Data | Data |

## Power Down Mode

In the power down mode the oscillator is stopped, and the instruction that invokes power down is the last instruction executed. The on-chip RAM and Special Function Registers retain their values until the power down mode is terminated. The only exit from power down is a hardware reset. Reset redefines the SFRs but does not change the on-chip RAM. The reset should not be activated before $V_{CC}$ is restored to its normal operating level and must be held active long enough to allow the oscillator to restart and stabilize.

## Program Memory Lock Bits

On the chip are three lock bits which can be left unprogrammed (U) or can be programmed (P) to obtain the additional features listed in the table below:

When lock bit 1 is programmed, the logic level at the $\overline{EA}$ pin is sampled and latched during reset. If the device is powered up without a reset, the latch initializes to a random value, and holds that value until reset is activated. It is necessary that the latched value of $\overline{EA}$ be in agreement with the current logic level at that pin in order for the device to function properly.

## Lock Bit Protection Modes

| Program Lock Bits | | | | Protection Type |
|---|---|---|---|---|
| | LB1 | LB2 | LB3 | |
| 1 | U | U | U | No program lock features. |
| 2 | P | U | U | MOVC instructions executed from external program memory are disabled from fetching code bytes from internal memory, $\overline{EA}$ is sampled and latched on reset, and further programming of the Flash is disabled. |
| 3 | P | P | U | Same as mode 2, also verify is disabled. |
| 4 | P | P | P | Same as mode 3, also external execution is disabled. |

## Programming the Flash

The AT89C51 is normally shipped with the on-chip Flash memory array in the erased state (that is, contents = FFH) and ready to be programmed. The programming interface accepts either a high-voltage (12-volt) or a low-voltage ($V_{CC}$) program enable signal. The low voltage programming mode provides a convenient way to program the AT89C51 inside the user's system, while the high-voltage programming mode is compatible with conventional third party Flash or EPROM programmers.

The AT89C51 is shipped with either the high-voltage or low-voltage programming mode enabled. The respective top-side marking and device signature codes are listed in the following table.

| | $V_{PP}$ = 12V | $V_{PP}$ = 5V |
|---|---|---|
| Top-Side Mark | AT89C51<br>xxxx<br>yyww | AT89C51<br>xxxx-5<br>yyww |
| Signature | (030H)=1EH<br>(031H)=51H<br>(032H)=FFH | (030H)=1EH<br>(031H)=51H<br>(032H)=05H |

The AT89C51 code memory array is programmed byte-by-byte in either programming mode. *To program any non-blank byte in the on-chip Flash Memory, the entire memory must be erased using the Chip Erase Mode.*

**Programming Algorithm:** Before programming the AT89C51, the address, data and control signals should be set up according to the Flash programming mode table and Figures 3 and 4. To program the AT89C51, take the following steps.

1. Input the desired memory location on the address lines.
2. Input the appropriate data byte on the data lines.
3. Activate the correct combination of control signals.
4. Raise $\overline{EA}/V_{PP}$ to 12V for the high-voltage programming mode.
5. Pulse ALE/$\overline{PROG}$ once to program a byte in the Flash array or the lock bits. The byte-write cycle is self-timed and typically takes no more than 1.5 ms. Repeat steps 1 through 5, changing the address and data for the entire array or until the end of the object file is reached.

**$\overline{\text{Data}}$ Polling:** The AT89C51 features $\overline{\text{Data}}$ Polling to indicate the end of a write cycle. During a write cycle, an attempted read of the last byte written will result in the complement of the written datum on PO.7. Once the write cycle has been completed, true data are valid on all outputs, and the next cycle may begin. $\overline{\text{Data}}$ Polling may begin any time after a write cycle has been initiated.

**Ready/$\overline{\text{Busy}}$:** The progress of byte programming can also be monitored by the RDY/$\overline{BSY}$ output signal. P3.4 is pulled low after ALE goes high during programming to indicate BUSY. P3.4 is pulled high again when programming is done to indicate READY.

**Program Verify:** If lock bits LB1 and LB2 have not been programmed, the programmed code data can be read back via the address and data lines for verification. The lock bits cannot be verified directly. Verification of the lock bits is achieved by observing that their features are enabled.

**Chip Erase:** The entire Flash array is erased electrically by using the proper combination of control signals and by holding ALE/$\overline{PROG}$ low for 10 ms. The code array is written with all "1"s. The chip erase operation must be executed before the code memory can be re-programmed.

**Reading the Signature Bytes:** The signature bytes are read by the same procedure as a normal verification of locations 030H,

031H, and 032H, except that P3.6 and P3.7 must be pulled to a logic low. The values returned are as follows.

(030H) = 1EH indicates manufactured by Atmel
(031H) = 51H indicates 89C51
(032H) = FFH indicates 12V programming
(032H) = 05H indicates 5V programming

## Programming Interface

Every code byte in the Flash array can be written and the entire array can be erased by using the appropriate combination of control signals. The write operation cycle is self-timed and once initiated, will automatically time itself to completion.

All major programming vendors offer worldwide support for the Atmel microcontroller series. Please contact your local programming vendor for the appropriate software revision.

## Flash Programming Modes

| Mode | | RST | $\overline{PSEN}$ | ALE/$\overline{PROG}$ | $\overline{EA}/V_{PP}$ | P2.6 | P2.7 | P3.6 | P3.7 |
|---|---|---|---|---|---|---|---|---|---|
| Write Code Data | | H | L | | H/12V | L | H | H | H |
| Read Code Data | | H | L | H | H | L | L | H | H |
| Write Lock | Bit - 1 | H | L | | H/12V | H | H | H | H |
| | Bit - 2 | H | L | | H/12V | H | H | L | L |
| | Bit - 3 | H | L | | H/12V | H | L | H | L |
| Chip Erase | | H | L | (1) | H/12V | H | L | L | L |
| Read Signature Byte | | H | L | H | H | L | L | L | L |

Note: 1. Chip Erase requires a 10-ms PROG pulse.

**Figure 3.** Programming the Flash

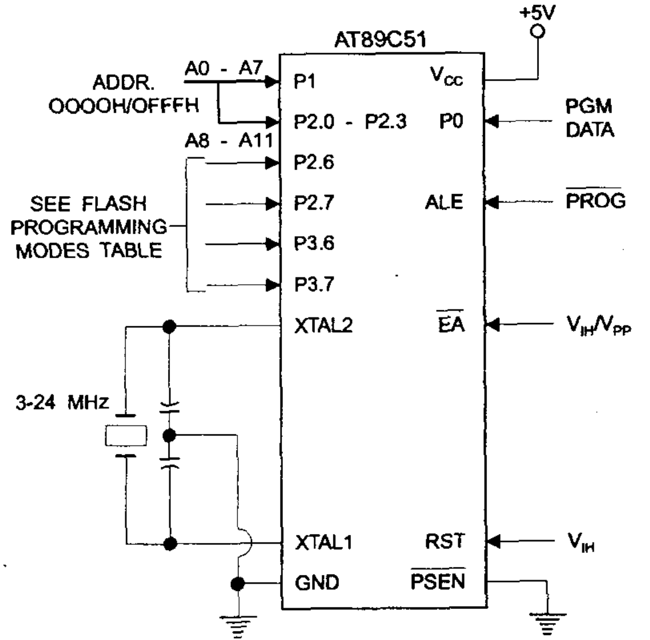
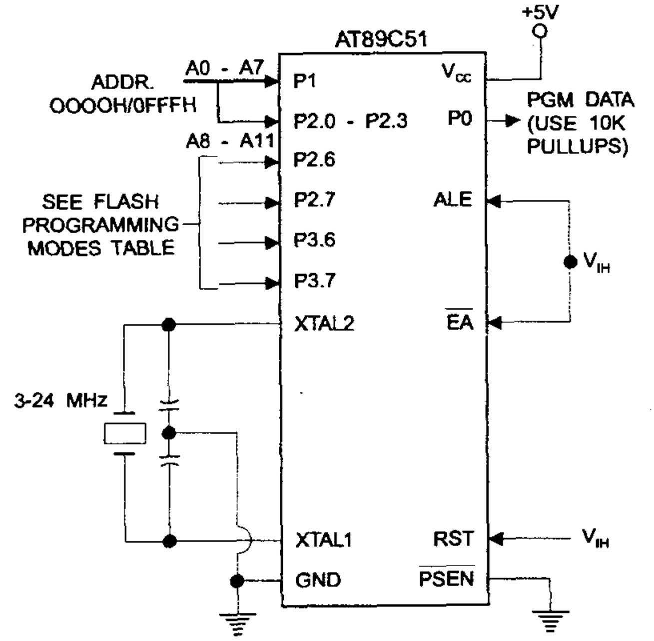



**Figure 4.** Verifying the Flash



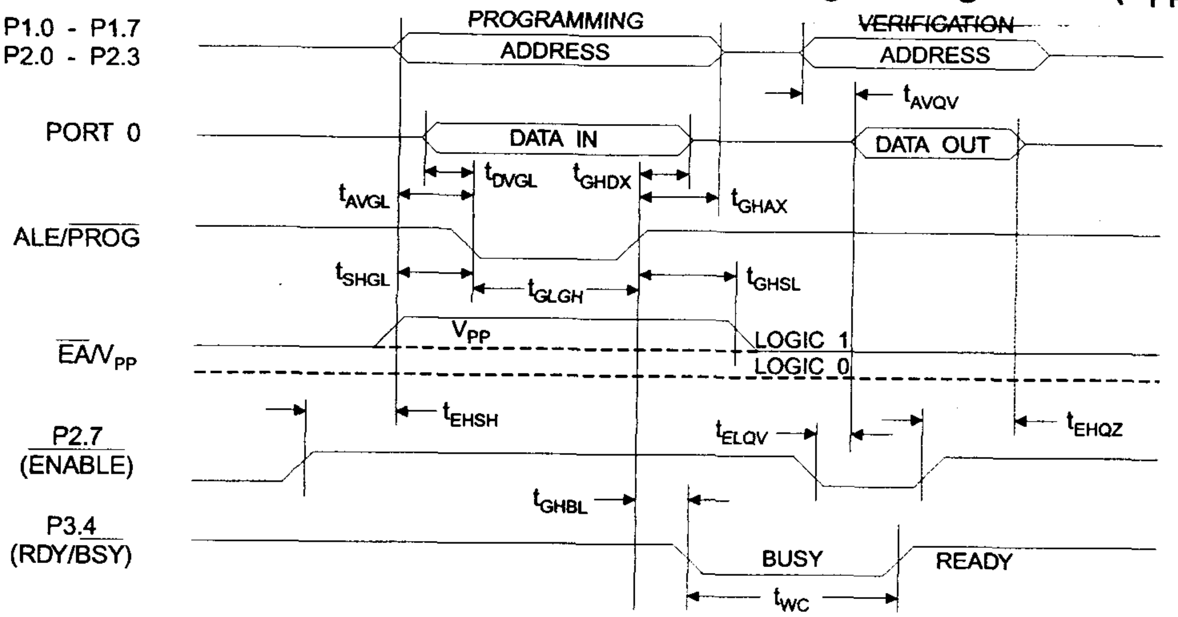

## Flash Programming and Verification Characteristics

$T_A$ = 0°C to 70°C, $V_{CC}$ = 5.0 ± 10%

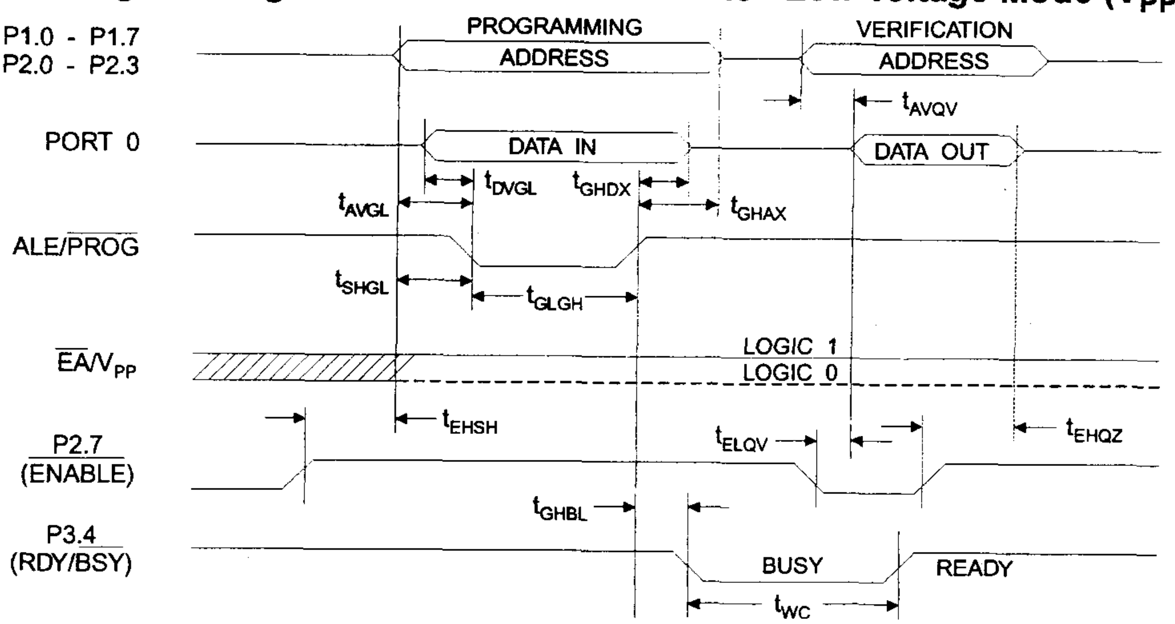
| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $V_{PP}$(1) | Programming Enable Voltage | 11.5 | 12.5 | V |
| $I_{PP}$(1) | Programming Enable Current | | 1.0 | mA |
| $1/t_{CLCL}$ | Oscillator Frequency | 3 | 24 | MHz |
| $t_{AVGL}$ | Address Setup to $\overline{\text{PROG}}$ Low | $48t_{CLCL}$ | | |
| $t_{GHAX}$ | Address Hold After $\overline{\text{PROG}}$ | $48t_{CLCL}$ | | |
| $t_{DVGL}$ | Data Setup to $\overline{\text{PROG}}$ Low | $48t_{CLCL}$ | | |
| $t_{GHDX}$ | Data Hold After $\overline{\text{PROG}}$ | $48t_{CLCL}$ | | |
| $t_{EHSH}$ | P2.7 ($\overline{\text{ENABLE}}$) High to $V_{PP}$ | $48t_{CLCL}$ | | |
| $t_{SHGL}$ | $V_{PP}$ Setup to $\overline{\text{PROG}}$ Low | 10 | | µs |
| $t_{GHSL}$(1) | $V_{PP}$ Hold After $\overline{\text{PROG}}$ | 10 | | µs |
| $t_{GLGH}$ | $\overline{\text{PROG}}$ Width | 1 | 110 | µs |
| $t_{AVQV}$ | Address to Data Valid | | $48t_{CLCL}$ | |
| $t_{ELQV}$ | $\overline{\text{ENABLE}}$ Low to Data Valid | | $48t_{CLCL}$ | |
| $t_{EHQZ}$ | Data Float After $\overline{\text{ENABLE}}$ | 0 | $48t_{CLCL}$ | |
| $t_{GHBL}$ | $\overline{\text{PROG}}$ High to $\overline{\text{BUSY}}$ Low | | 1.0 | µs |
| $t_{WC}$ | Byte Write Cycle Time | | 2.0 | ms |

Note: 1. Only used in 12-volt programming mode.

## Flash Programming and Verification Waveforms - High Voltage Mode ($V_{PP}$ = 12V)




## Flash Programming and Verification Waveforms - Low Voltage Mode ($V_{PP}$ = 5V)



## Absolute Maximum Ratings*

| | |
|---|---|
| Operating Temperature | -55°C to +125°C |
| Storage Temperature | -65°C to +150°C |
| Voltage on Any Pin with Respect to Ground | -1.0V to +7.0V |
| Maximum Operating Voltage | 6.6V |
| DC Output Current | 15.0 mA |

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## DC Characteristics

$T_A$ = -40°C to 85°C, $V_{CC}$ = 5.0V ± 20% (unless otherwise noted)

| Symbol | Parameter | Condition | Min | Max | Units |
|---|---|---|---|---|---|
| $V_{IL}$ | Input Low Voltage | (Except $\overline{EA}$) | -0.5 | 0.2 $V_{CC}$ - 0.1 | V |
| $V_{IL1}$ | Input Low Voltage ($\overline{EA}$) | | -0.5 | 0.2 $V_{CC}$ - 0.3 | V |
| $V_{IH}$ | Input High Voltage | (Except XTAL1, RST) | 0.2 $V_{CC}$ + 0.9 | $V_{CC}$ + 0.5 | V |
| $V_{IH1}$ | Input High Voltage | (XTAL1, RST) | 0.7 $V_{CC}$ | $V_{CC}$ + 0.5 | V |
| $V_{OL}$ | Output Low Voltage(1) (Ports 1,2,3) | $I_{OL}$ = 1.6 mA | | 0.45 | V |
| $V_{OL1}$ | Output Low Voltage(1) (Port 0, ALE, $\overline{PSEN}$) | $I_{OL}$ = 3.2 mA | | 0.45 | V |
| $V_{OH}$ | Output High Voltage (Ports 1,2,3, ALE, $\overline{PSEN}$) | $I_{OH}$ = -60 µA, $V_{CC}$ = 5V ± 10% | 2.4 | | V |
| | | $I_{OH}$ = -25 µA | 0.75 $V_{CC}$ | | V |
| | | $I_{OH}$ = -10 µA | 0.9 $V_{CC}$ | | V |
| $V_{OH1}$ | Output High Voltage (Port 0 in External Bus Mode) | $I_{OH}$ = -800 µA, $V_{CC}$ = 5V ± 10% | 2.4 | | V |
| | | $I_{OH}$ = -300 µA | 0.75 $V_{CC}$ | | V |
| | | $I_{OH}$ = -80 µA | 0.9 $V_{CC}$ | | V |
| $I_{IL}$ | Logical 0 Input Current (Ports 1,2,3) | $V_{IN}$ = 0.45V | | -50 | µA |
| $I_{TL}$ | Logical 1 to 0 Transition Current (Ports 1,2,3) | $V_{IN}$ = 2V, VCC = 5V ± 10% | | -650 | µA |
| $I_{LI}$ | Input Leakage Current (Port 0, $\overline{EA}$) | 0.45 < $V_{IN}$ < $V_{CC}$ | | ±10 | µA |
| RRST | Reset Pulldown Resistor | | 50 | 300 | KΩ |
| $C_{IO}$ | Pin Capacitance | Test Freq. = 1 MHz, $T_A$ = 25°C | | 10 | pF |
| $I_{CC}$ | Power Supply Current | Active Mode, 12 MHz | | 20 | mA |
| | | Idle Mode, 12 MHz | | 5 | mA |
| | Power Down Mode(2) | $V_{CC}$ = 6V | | 100 | µA |
| | | $V_{CC}$ = 3V | | 40 | µA |

Notes: 1. Under steady state (non-transient) conditions, $I_{OL}$ must be externally limited as follows:
Maximum $I_{OL}$ per port pin: 10 mA
Maximum $I_{OL}$ per 8-bit port: Port 0: 26 mA
Ports 1, 2, 3: 15 mA
Maximum total $I_{OL}$ for all output pins: 71 mA
If $I_{OL}$ exceeds the test condition, $V_{OL}$ may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

2. Minimum $V_{CC}$ for Power Down is 2V.

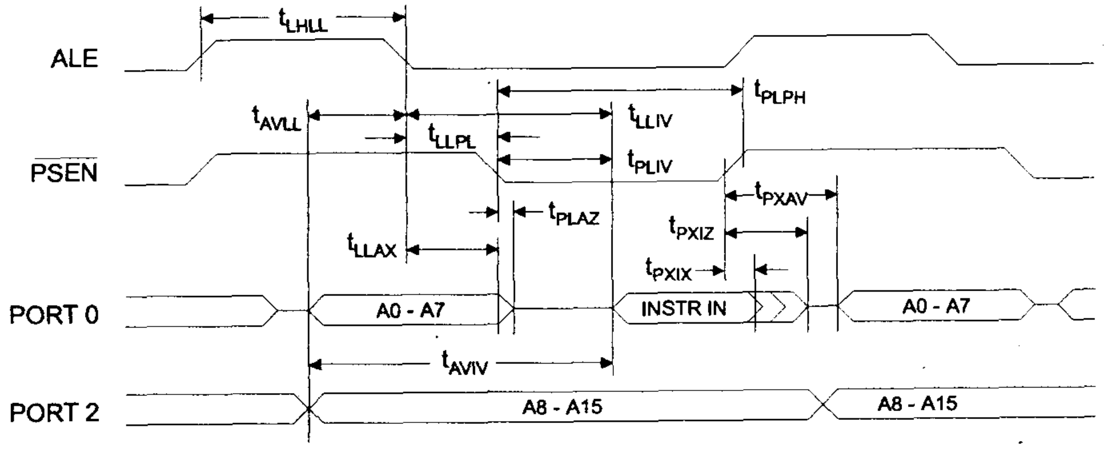
## AC Characteristics

(Under Operating Conditions; Load Capacitance for Port 0, ALE/$\overline{PROG}$, and $\overline{PSEN}$ = 100 pF; Load Capacitance for all other outputs = 80 pF)

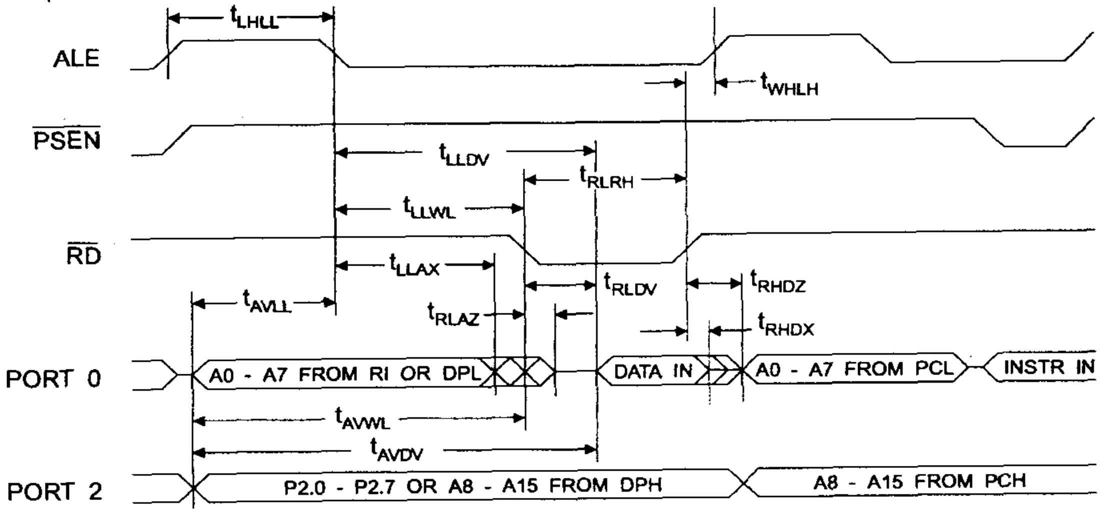
## External Program and Data Memory Characteristics

| Symbol | Parameter | 12 MHz Oscillator | | 16 to 24 MHz Oscillator | | Units |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| $1/t_{CLCL}$ | Oscillator Frequency | | | 0 | 24 | MHz |
| $t_{LHLL}$ | ALE Pulse Width | 127 | | $2t_{CLCL}$-40 | | ns |
| $t_{AVLL}$ | Address Valid to ALE Low | 43 | | $t_{CLCL}$-13 | | ns |
| $t_{LLAX}$ | Address Hold After ALE Low | 48 | | $t_{CLCL}$-20 | | ns |
| $t_{LLIV}$ | ALE Low to Valid Instruction In | | 233 | | $4t_{CLCL}$-65 | ns |
| $t_{LLPL}$ | ALE Low to $\overline{PSEN}$ Low | 43 | | $t_{CLCL}$-13 | | ns |
| $t_{PLPH}$ | $\overline{PSEN}$ Pulse Width | 205 | | $3t_{CLCL}$-20 | | ns |
| $t_{PLIV}$ | $\overline{PSEN}$ Low to Valid Instruction In | | 145 | | $3t_{CLCL}$-45 | ns |
| $t_{PXIX}$ | Input Instruction Hold After $\overline{PSEN}$ | 0 | | 0 | | ns |
| $t_{PXIZ}$ | Input Instruction Float After $\overline{PSEN}$ | | 59 | | $t_{CLCL}$-10 | ns |
| $t_{PXAV}$ | $\overline{PSEN}$ to Address Valid | 75 | | $t_{CLCL}$-8 | | ns |
| $t_{AVIV}$ | Address to Valid Instruction In | | 312 | | $5t_{CLCL}$-55 | ns |
| $t_{PLAZ}$ | $\overline{PSEN}$ Low to Address Float | | 10 | | 10 | ns |
| $t_{RLRH}$ | $\overline{RD}$ Pulse Width | 400 | | $6t_{CLCL}$-100 | | ns |
| $t_{WLWH}$ | $\overline{WR}$ Pulse Width | 400 | | $6t_{CLCL}$-100 | | ns |
| $t_{RLDV}$ | $\overline{RD}$ Low to Valid Data In | | 252 | | $5t_{CLCL}$-90 | ns |
| $t_{RHDX}$ | Data Hold After $\overline{RD}$ | 0 | | 0 | | ns |
| $t_{RHDZ}$ | Data Float After $\overline{RD}$ | | 97 | | $2t_{CLCL}$-28 | ns |
| $t_{LLDV}$ | ALE Low to Valid Data In | | 517 | | $8t_{CLCL}$-150 | ns |
| $t_{AVDV}$ | Address to Valid Data In | | 585 | | $9t_{CLCL}$-165 | ns |
| $t_{LLWL}$ | ALE Low to $\overline{RD}$ or $\overline{WR}$ Low | 200 | 300 | $3t_{CLCL}$-50 | $3t_{CLCL}$+50 | ns |
| $t_{AVWL}$ | Address to $\overline{RD}$ or $\overline{WR}$ Low | 203 | | $4t_{CLCL}$-75 | | ns |
| $t_{QVWX}$ | Data Valid to $\overline{WR}$ Transition | 23 | | $t_{CLCL}$-20 | | ns |
| $t_{QVWH}$ | Data Valid to $\overline{WR}$ High | 433 | | $7t_{CLCL}$-120 | | ns |
| $t_{WHQX}$ | Data Hold After $\overline{WR}$ | 33 | | $t_{CLCL}$-20 | | ns |
| $t_{RLAZ}$ | $\overline{RD}$ Low to Address Float | | 0 | | 0 | ns |
| $t_{WHLH}$ | $\overline{RD}$ or $\overline{WR}$ High to ALE High | 43 | 123 | $t_{CLCL}$-20 | $t_{CLCL}$+25 | ns |

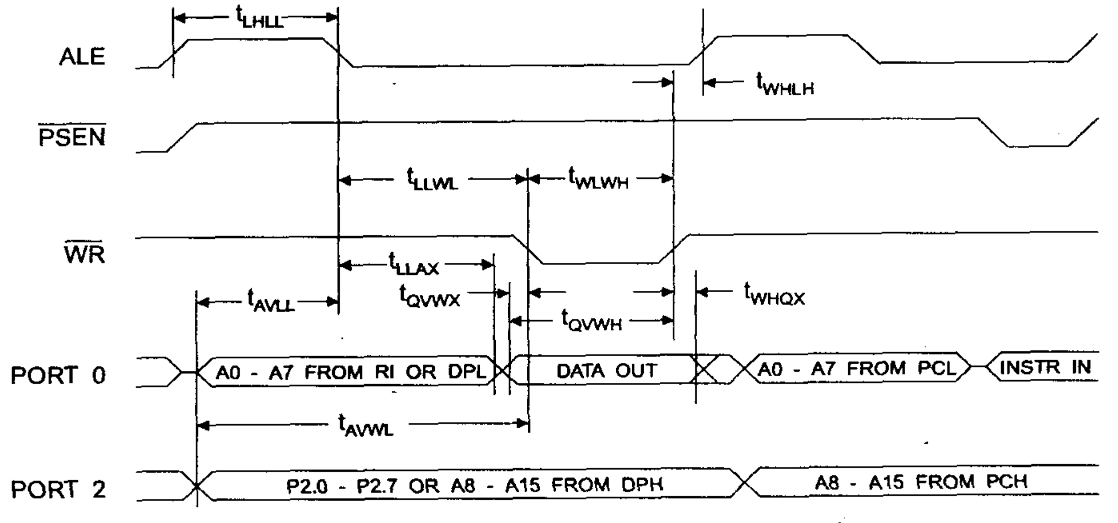
## External Program Memory Read Cycle



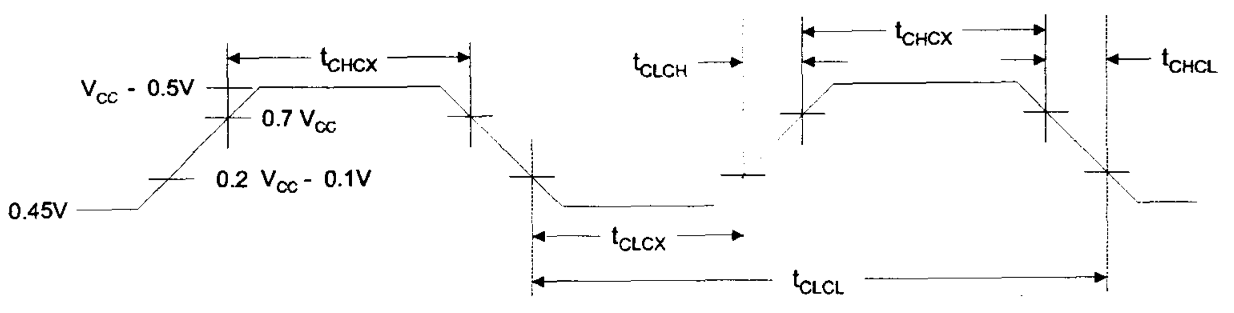

## External Data Memory Read Cycle



## External Data Memory Write Cycle




## External Clock Drive Waveforms




## External Clock Drive

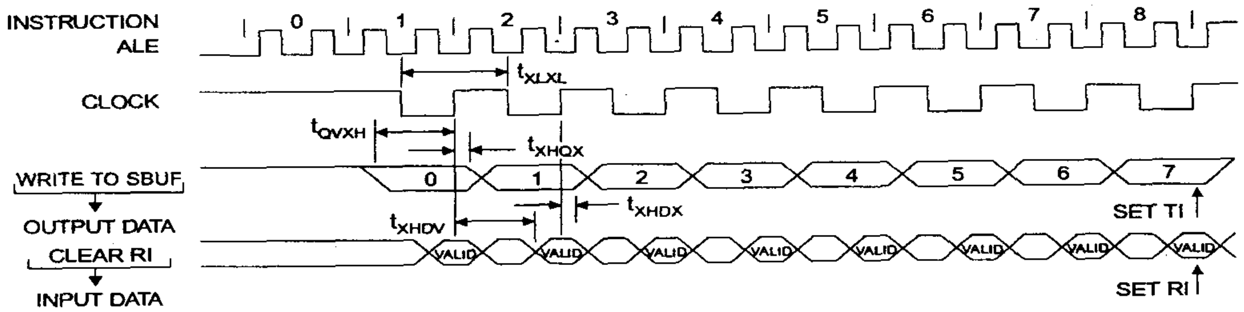
| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $1/t_{CLCL}$ | Oscillator Frequency | 0 | 24 | MHz |
| $t_{CLCL}$ | Clock Period | 41.6 | | ns |
| $t_{CHCX}$ | High Time | 15 | | ns |
| $t_{CLCX}$ | Low Time | 15 | | ns |
| $t_{CLCH}$ | Rise Time | | 20 | ns |
| $t_{CHCL}$ | Fall Time | | 20 | ns |

## Serial Port Timing: Shift Register Mode Test Conditions

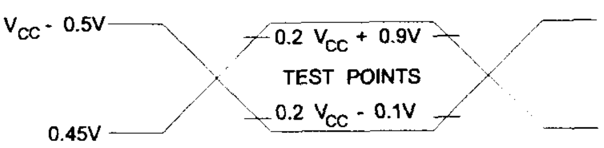
($V_{CC}$ = 5.0 V ± 20%; Load Capacitance = 80 pF)

| Symbol | Parameter | 12 MHz Osc | | Variable Oscillator | | Units |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| $t_{XLXL}$ | Serial Port Clock Cycle Time | 1.0 | | $12t_{CLCL}$ | | µs |
| $t_{QVXH}$ | Output Data Setup to Clock Rising Edge | 700 | | $10t_{CLCL}$-133 | | ns |
| $t_{XHQX}$ | Output Data Hold After Clock Rising Edge | 50 | | $2t_{CLCL}$-117 | | ns |
| $t_{XHDX}$ | Input Data Hold After Clock Rising Edge | 0 | | 0 | | ns |
| $t_{XHDV}$ | Clock Rising Edge to Input Data Valid | | 700 | | $10t_{CLCL}$-133 | ns |

## Shift Register Mode Timing Waveforms

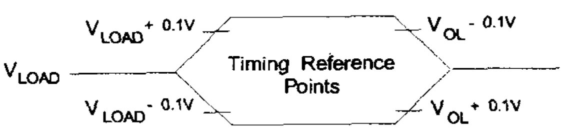



## AC Testing Input/Output Waveforms[1]




Note: 1. AC Inputs during testing are driven at $V_{CC}$ - 0.5V for a logic 1 and 0.45V for a logic 0. Timing measurements are made at $V_{IH}$ min. for a logic 1 and $V_{IL}$ max. for a logic 0.

## Float Waveforms[1]




Note: 1. For timing purposes, a port pin is no longer floating when a 100 mV change from load voltage occurs. A port pin begins to float when 100 mV change from the loaded $V_{OH}/V_{OL}$ level occurs.

## Ordering Information

| Speed (MHz) | Power Supply | Ordering Code | Package | Operation Range |
|---|---|---|---|---|
| 12 | 5V ± 20% | AT89C51-12AC | 44A | Commercial |
| | | AT89C51-12JC | 44J | (0°C to 70°C) |
| | | AT89C51-12PC | 40P6 | |
| | | AT89C51-12QC | 44Q | |
| | | AT89C51-12AI | 44A | Industrial |
| | | AT89C51-12JI | 44J | (-40°C to 85°C) |
| | | AT89C51-12PI | 40P6 | |
| | | AT89C51-12QI | 44Q | |
| | | AT89C51-12AA | 44A | Automotive |
| | | AT89C51-12JA | 44J | (-40°C to 105°C) |
| | | AT89C51-12PA | 40P6 | |
| | | AT89C51-12QA | 44Q | |
| 16 | 5V ± 20% | AT89C51-16AC | 44A | Commercial |
| | | AT89C51-16JC | 44J | (0°C to 70°C) |
| | | AT89C51-16PC | 40P6 | |
| | | AT89C51-16QC | 44Q | |
| | | AT89C51-16AI | 44A | Industrial |
| | | AT89C51-16JI | 44J | (-40°C to 85°C) |
| | | AT89C51-16PI | 40P6 | |
| | | AT89C51-16QI | 44Q | |
| | | AT89C51-16AA | 44A | Automotive |
| | | AT89C51-16JA | 44J | (-40°C to 105°C) |
| | | AT89C51-16PA | 40P6 | |
| | | AT89C51-16QA | 44Q | |
| 20 | 5V ± 20% | AT89C51-20AC | 44A | Commercial |
| | | AT89C51-20JC | 44J | (0°C to 70°C) |
| | | AT89C51-20PC | 40P6 | |
| | | AT89C51-20QC | 44Q | |
| | | AT89C51-20AI | 44A | Industrial |
| | | AT89C51-20JI | 44J | (-40°C to 85°C) |
| | | AT89C51-20PI | 40P6 | |
| | | AT89C51-20QI | 44Q | |

## Ordering Information

| Speed (MHz) | Power Supply | Ordering Code | Package | Operation Range |
|---|---|---|---|---|
| 24 | 5V ± 20% | AT89C51-24AC | 44A | Commercial |
| | | AT89C51-24JC | 44J | (0°C to 70°C) |
| | | AT89C51-24PC | 44P6 | |
| | | AT89C51-24QC | 44Q | |
| | | AT89C51-24AI | 44A | Industrial |
| | | AT89C51-24JI | 44J | (-40°C to 85°C) |
| | | AT89C51-24PI | 44P6 | |
| | | AT89C51-24QI | 44Q | |

| Package Type | |
|---|---|
| **44A** | 44 Lead, Thin Plastic Gull Wing Quad Flatpack (TQFP) |
| **44J** | 44 Lead, Plastic J-Leaded Chip Carrier (PLCC) |
| **40P6** | 40 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP) |
| **44Q** | 44 Lead, Plastic Gull Wing Quad Flatpack (PQFP) |

National Semiconductor

December 1994

# LM124/LM224/LM324/LM2902 Low Power Quad Operational Amplifiers

## General Description

The LM124 series consists of four independent, high gain, internally frequency compensated operational amplifiers which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

Application areas include transducer amplifiers, DC gain blocks and all the conventional op amp circuits which now can be more easily implemented in single power supply systems. For example, the LM124 series can be directly operated off of the standard +5V power supply voltage which is used in digital systems and will easily provide the required interface electronics without requiring the additional ±15V power supplies.

## Unique Characteristics

- In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage
- The unity gain cross frequency is temperature compensated
- The input bias current is also temperature compensated

## Advantages

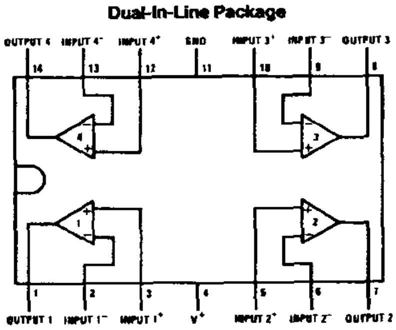
- Eliminates need for dual supplies
- Four internally compensated op amps in a single package
- Allows directly sensing near GND and $V_{OUT}$ also goes to GND
- Compatible with all forms of logic
- Power drain suitable for battery operation

## Features

- Internally frequency compensated for unity gain
- Large DC voltage gain 100 dB
- Wide bandwidth (unity gain) 1 MHz (temperature compensated)
- Wide power supply range:
  - Single supply 3V to 32V
  - or dual supplies ±1.5V to ±16V
- Very low supply current drain (700 μA)—essentially independent of supply voltage
- Low input biasing current 45 nA (temperature compensated)
- Low input offset voltage 2 mV and offset current 5 nA
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Large output voltage swing 0V to V+ − 1.5V

## Connection Diagram

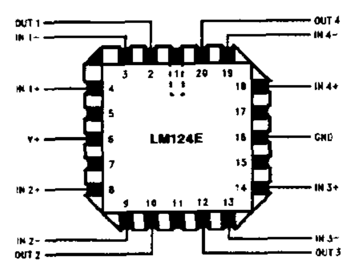
**Dual-In-Line Package**




TL/H/9299-1

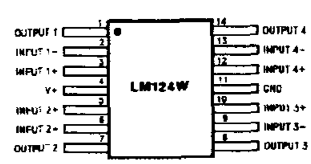
**Top View**

**Order Number LM124J, LM124AJ, LM124J/883**, LM124AJ/883*, LM224J, LM224AJ, LM324J, LM324M, LM324AM, LM2902M, LM324N, LM324AN or LM2902N**
**See NS Package Number J14A, M14A or N14A**




TL/H/9299-32

**Order Number LM124AE/883 or LM124E/883**
**See NS Package Number E20A**




TL/H/9299-33

**Order Number LM124AW/883 or LM124W/883**
**See NS Package Number W14B**

*LM124A available per JM38510/11006
**LM124 available per JM38510/11005



RRD-B30M115/Printed in U. S. A.

## Absolute Maximum Ratings

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications. (Note 9)**

| | LM124/LM224/LM324 LM124A/LM224A/LM324A | LM2902 |
|---|---|---|
| Supply Voltage, $V^+$ | 32V | 26V |
| Differential Input Voltage | 32V | 26V |
| Input Voltage | −0.3V to +32V | −0.3V to +26V |
| Input Current ($V_{IN} < -0.3V$) (Note 3) | 50 mA | 50 mA |
| Power Dissipation (Note 1) | | |
| Molded DIP | 1130 mW | 1130 mW |
| Cavity DIP | 1260 mW | 1260 mW |
| Small Outline Package | 800 mW | 800 mW |
| Output Short-Circuit to GND (One Amplifier) (Note 2) $V^+ \leq 15V$ and $T_A = 25°C$ | Continuous | Continuous |
| Operating Temperature Range | | −40°C to +85°C |
| LM324/LM324A | 0°C to +70°C | |
| LM224/LM224A | −25°C to +85°C | |
| LM124/LM124A | −55°C to +125°C | |

| | LM124/LM224/LM324 LM124A/LM224A/LM324A | LM2902 |
|---|---|---|
| Storage Temperature Range | −65°C to +150°C | −65°C to +150°C |
| Lead Temperature (Soldering, 10 seconds) | 260°C | 260°C |
| Soldering Information | | |
| Dual-In-Line Package | | |
| Soldering (10 seconds) | 260°C | 260°C |
| Small Outline Package | | |
| Vapor Phase (60 seconds) | 215°C | 215°C |
| Infrared (15 seconds) | 220°C | 220°C |

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

| | | |
|---|---|---|
| ESD Tolerance (Note 10) | 250V | 250V |

## Electrical Characteristics $V^+ = +5.0V$, (Note 4), unless otherwise stated

| Parameter | Conditions | LM124A | | | LM224A | | | LM324A | | | LM124/LM224 | | | LM324 | | | LM2902 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Input Offset Voltage | (Note 5) $T_A = 25°C$ | | 1 | 2 | | 1 | 3 | | 2 | 3 | | 2 | 5 | | 2 | 7 | | 2 | 7 | mV |
| Input Bias Current (Note 6) | $I_{IN(+)}$ or $I_{IN(-)}$, $V_{CM} = 0V$, $T_A = 25°C$ | | 20 | 50 | | 40 | 80 | | 45 | 100 | | 45 | 150 | | 45 | 250 | | 45 | 250 | nA |
| Input Offset Current | $I_{IN(+)} - I_{IN(-)}$, $V_{CM} = 0V$, $T_A = 25°C$ | | 2 | 10 | | 2 | 15 | | 5 | 30 | | 3 | 30 | | 5 | 50 | | 5 | 50 | nA |
| Input Common-Mode Voltage Range (Note 7) | $V^+ = 30V$, (LM2902, $V^+ = 26V$), $T_A = 25°C$ | 0 | | $V^+-1.5$ | 0 | | $V^+-1.5$ | 0 | | $V^+-1.5$ | 0 | | $V^+-1.5$ | 0 | | $V^+-1.5$ | 0 | | $V^+-1.5$ | V |
| Supply Current | Over Full Temperature Range $R_L = \infty$ On All Op Amps | | | | | | | | | | | | | | | | | | | mA |
| | $V^+ = 30V$ (LM2902 $V^+ = 26V$) | | 1.5 | 3 | | 1.5 | 3 | | 1.5 | 3 | | 1.5 | 3 | | 1.5 | 3 | | 1.5 | 3 | |
| | $V^+ = 5V$ | | 0.7 | 1.2 | | 0.7 | 1.2 | | 0.7 | 1.2 | | 0.7 | 1.2 | | 0.7 | 1.2 | | 0.7 | 1.2 | |
| Large Signal Voltage Gain | $V^+ = 15V$, $R_L \geq 2\ k\Omega$, ($V_O = 1V$ to $11V$), $T_A = 25°C$ | 50 | 100 | | 50 | 100 | | 25 | 100 | | 50 | 100 | | 25 | 100 | | 25 | 100 | | V/mV |
| Common-Mode Rejection Ratio | DC, $V_{CM} = 0V$ to $V^+ - 1.5V$, $T_A = 25°C$ | 70 | 85 | | 70 | 85 | | 65 | 85 | | 70 | 85 | | 65 | 85 | | 50 | 70 | | dB |
| Power Supply Rejection Ratio | $V^+ = 5V$ to $30V$ (LM2902, $V^+ = 5V$ to $26V$), $T_A = 25°C$ | 65 | 100 | | 65 | 100 | | 65 | 100 | | 65 | 100 | | 65 | 100 | | 50 | 100 | | dB |

## Electrical Characteristics $V^+ = +5.0V$ (Note 4) unless otherwise stated (Continued)

| Parameter | | Conditions | | LM124A | | | LM224A | | | LM324A | | | LM124/LM224 | | | LM324 | | | LM2902 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Amplifier-to-Amplifier Coupling (Note 8) | | $f = 1$ kHz to 20 kHz, $T_A = 25°C$ (Input Referred) | | | −120 | | | −120 | | | −120 | | | −120 | | | −120 | | | −120 | | dB |
| Output Current | Source | $V_{IN}^+ = 1V$, $V_{IN}^- = 0V$, $V^+ = 15V$, $V_O = 2V$, $T_A = 25°C$ | | 20 | 40 | | 20 | 40 | | 20 | 40 | | 20 | 40 | | 20 | 40 | | 20 | 40 | | mA |
| | Sink | $V_{IN}^- = 1V$, $V_{IN}^+ = 0V$, $V^+ = 15V$, $V_O = 2V$, $T_A = 25°C$ | | 10 | 20 | | 10 | 20 | | 10 | 20 | | 10 | 20 | | 10 | 20 | | 10 | 20 | | mA |
| | | $V_{IN}^- = 1V$, $V_{IN}^+ = 0V$, $V^+ = 15V$, $V_O = 200$ mV, $T_A = 25°C$ | | 12 | 50 | | 12 | 50 | | 12 | 50 | | 12 | 50 | | 12 | 50 | | 12 | 50 | | $\mu$A |
| Short Circuit to Ground | | (Note 2) $V^+ = 15V$, $T_A = 25°C$ | | | 40 | 60 | | 40 | 60 | | 40 | 60 | | 40 | 60 | | 40 | 60 | | 40 | 60 | mA |
| Input Offset Voltage | | (Note 5) | | | | 4 | | | 4 | | | 5 | | | 7 | | | 9 | | | 10 | mV |
| Input Offset Voltage Drift | | $R_S = 0\Omega$ | | | 7 | 20 | | 7 | 20 | | 7 | 30 | | 7 | | | 7 | | | 7 | | $\mu$V/°C |
| Input Offset Current | | $I_{IN(+)} - I_{IN(-)}$, $V_{CM} = 0V$ | | | | 30 | | | 30 | | | 75 | | | 100 | | | 150 | | 45 | 200 | nA |
| Input Offset Current Drift | | $R_S = 0\Omega$ | | | 10 | 200 | | 10 | 200 | | 10 | 300 | | 10 | | | 10 | | | 10 | | pA/°C |
| Input Bias Current | | $I_{IN(+)}$ or $I_{IN(-)}$ | | | 40 | 100 | | 40 | 100 | | 40 | 200 | | 40 | 300 | | 40 | 500 | | 40 | 500 | nA |
| Input Common-Mode Voltage Range (Note 7) | | $V^+ = +30V$ (LM2902, $V^+ = 26V$) | | 0 | | $V^+ - 2$ | 0 | | $V^+ - 2$ | 0 | | $V^+ - 2$ | 0 | | $V^+ - 2$ | 0 | | $V^+ - 2$ | 0 | | $V^+ - 2$ | V |
| Large Signal Voltage Gain | | $V^+ = +15V$ ($V_O$ Swing $= 1V$ to $11V$) $R_L \geq 2$ k$\Omega$ | | 25 | | | 25 | | | 15 | | | 25 | | | 15 | | | 15 | | | V/mV |
| Output Voltage Swing | $V_{OH}$ | $V^+ = 30V$ (LM2902, $V^+ = 26V$) | $R_L = 2$ k$\Omega$ | 26 | | | 26 | | | 26 | | | 26 | | | 26 | | | 22 | | | V |
| | | | $R_L = 10$ k$\Omega$ | 27 | 28 | | 27 | 28 | | 27 | 28 | | 27 | 28 | | 27 | 28 | | 23 | 24 | | V |
| | $V_{OL}$ | $V^+ = 5V$, $R_L = 10$ k$\Omega$ | | | 5 | 20 | | 5 | 20 | | 5 | 20 | | 5 | 20 | | 5 | 20 | | 5 | 100 | mV |

## Electrical Characteristics $V^+ = +5.0V$ (Note 4) unless otherwise stated (Continued)

| Parameter | | Conditions | | LM124A | | | LM224A | | | LM324A | | | LM124/LM224 | | | LM324 | | | LM2902 | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| Output Current | Source | $V_O = 2V$ | $V_{IN}^+ = +1V$, $V_{IN}^- = 0V$, $V^+ = 15V$ | 10 | 20 | | 10 | 20 | | 10 | 20 | | 10 | 20 | | 10 | 20 | | 10 | 20 | | mA |
| | Sink | | $V_{IN}^- = +1V$, $V_{IN}^+ = 0V$, $V^+ = 15V$ | 10 | 15 | | 5 | 8 | | 5 | 8 | | 5 | 8 | | 5 | 8 | | 5 | 8 | | |

**Note 1:** For operating at high temperatures, the LM324/LM324A/LM2902 must be derated based on a +125°C maximum junction temperature and a thermal resistance of 88°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM224/LM224A and LM124/LM124A can be derated based on a +150°C maximum junction temperature. The dissipation is the total of all four amplifiers—use external resistors, where possible, to allow the amplifier to saturate of to reduce the power which is dissipated in the integrated circuit.

**Note 2:** Short circuits from the output to $V^+$ can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately 40 mA independent of the magnitude of $V^+$. At values of supply voltage in excess of +15V, continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.

**Note 3:** This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the op amps to go to the $V^+$ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than −0.3V (at 25°C).

**Note 4:** These specifications are limited to $-55°C \le T_A \le +125°C$ for the LM124/LM124A. With the LM224/LM224A, all temperature specifications are limited to $-25°C \le T_A \le +85°C$, the LM324/LM324A temperature specifications are limited to $0°C \le T_A \le +70°C$, and the LM2902 specifications are limited to $-40°C \le T_A \le +85°C$.

**Note 5:** $V_O \approx 1.4V$, $R_S = 0\Omega$ with $V^+$ from 5V to 30V; and over the full input common-mode range (0V to $V^+ - 1.5V$) for LM2902, $V^+$ from 5V to 26V.

**Note 6:** The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.

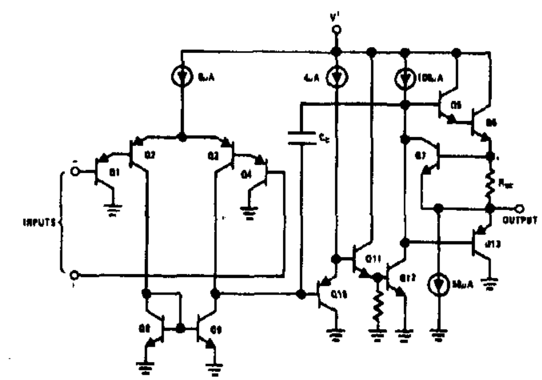
**Note 7:** The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0.3V (at 25°C). The upper end of the common-mode voltage range is $V^+ - 1.5V$ (at 25°C), but either or both inputs can go to +32V without damage (+26V for LM2902), independent of the magnitude of $V^+$.

**Note 8:** Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitance increases at higher frequencies.

**Note 9:** Refer to RETS124AX for LM124A military specifications and refer to RETS124X for LM124 military specifications.

**Note 10:** Human body model, 1.5 kΩ in series with 100 pF.

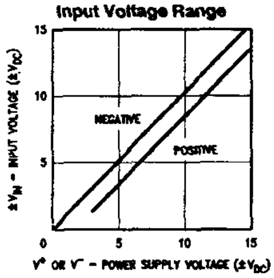
## Schematic Diagram (Each Amplifier)



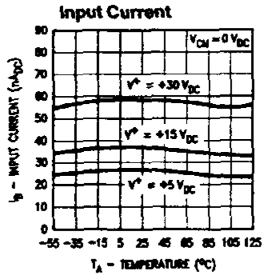

TL/H/9299–2

## Typical Performance Characteristics

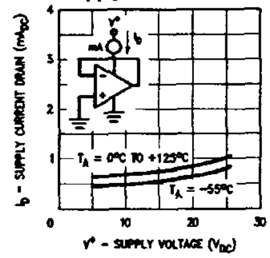
### Input Voltage Range



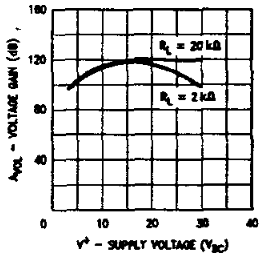

### Input Current



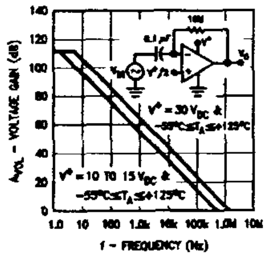

### Supply Current



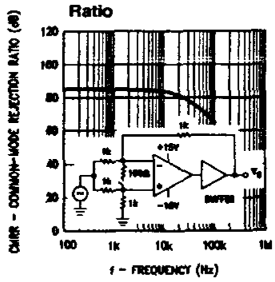

### Voltage Gain



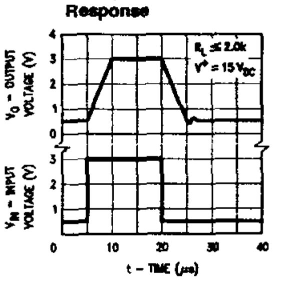

### Open Loop Frequency Response



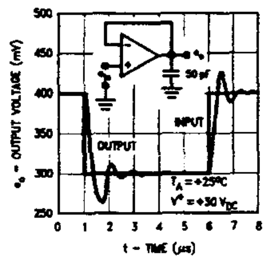

### Common Mode Rejection Ratio



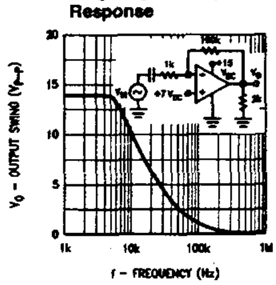

### Voltage Follower Pulse Response



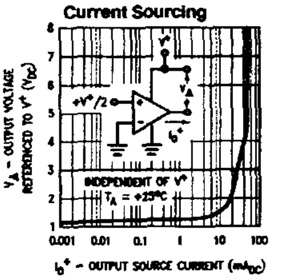

### Voltage Follower Pulse Response (Small Signal)



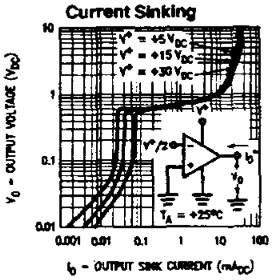

### Large Signal Frequency Response



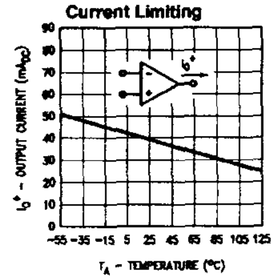

### Output Characteristics Current Sourcing




### Output Characteristics Current Sinking

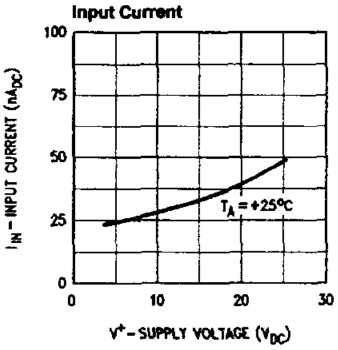


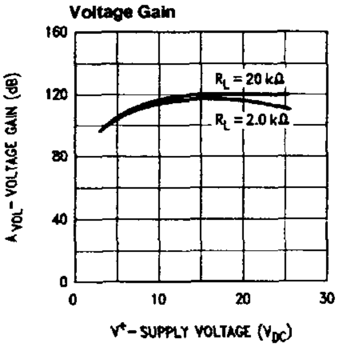

### Current Limiting




TL/H/9299–3

## Typical Performance Characteristics (LM2902 only)




TL/H/9299–4

## Application Hints

The LM124 series are op amps which operate with only a single power supply voltage, have true-differential inputs, and remain in the linear mode with an input common-mode voltage of 0 $V_{DC}$. These amplifiers operate over a wide range of power supply voltage with little change in performance characteristics. At 25°C amplifier operation is possible down to a minimum supply voltage of 2.3 $V_{DC}$.

The pinouts of the package have been designed to simplify PC board layouts. Inverting inputs are adjacent to outputs for all of the amplifiers and the outputs have also been placed at the corners of the package (pins 1, 7, 8, and 14).

Precautions should be taken to insure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a test socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Large differential input voltages can be easily accommodated and, as input differential voltage protection diodes are not needed, no large input currents result from large differential input voltages. The differential input voltage may be larger than V+ without damaging the device. Protection should be provided to prevent the input voltages from going negative more than −0.3 $V_{DC}$ (at 25°C). An input clamp diode with a resistor to the IC input terminal can be used.

To reduce the power supply drain, the amplifiers have a class A output stage for small signal levels which converts to class B in a large signal mode. This allows the amplifiers to both source and sink large output currents. Therefore both NPN and PNP external current boost transistors can be used to extend the power capability of the basic amplifiers. The output voltage needs to raise approximately 1 diode drop above ground to bias the on-chip vertical PNP transistor for output current sinking applications.

For ac applications, where the load is capacitively coupled to the output of the amplifier, a resistor should be used, from the output of the amplifier to ground to increase the class A bias current and prevent crossover distortion.

Where the load is directly coupled, as in dc applications, there is no crossover distortion.

Capacitive loads which are applied directly to the output of the amplifier reduce the loop stability margin. Values of 50 pF can be accommodated using the worst-case non-inverting unity gain connection. Large closed loop gains or resistive isolation should be used if larger load capacitance must be driven by the amplifier.

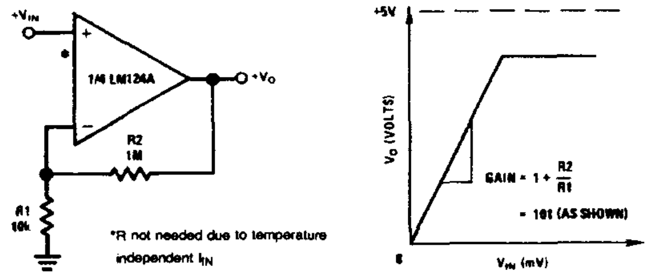
The bias network of the LM124 establishes a drain current which is independent of the magnitude of the power supply voltage over the range of from 3 $V_{DC}$ to 30 $V_{DC}$.

Output short circuits either to ground or to the positive power supply should be of short time duration. Units can be destroyed, not as a result of the short circuit current causing metal fusing, but rather due to the large increase in IC chip dissipation which will cause eventual failure due to excessive junction temperatures. Putting direct short-circuits on more than one amplifier at a time will increase the total IC power dissipation to destructive levels, if not properly protected with external dissipation limiting resistors in series with the output leads of the amplifiers. The larger value of output source current which is available at 25°C provides a larger output current capability at elevated temperatures (see typical performance characteristics) than a standard IC op amp.

The circuits presented in the section on typical applications emphasize operation on only a single power supply voltage. If complementary power supplies are available, all of the standard op amp circuits can be used. In general, introducing a pseudo-ground (a bias voltage reference of $V^+/2$) will allow operation above and below this value in single power supply systems. Many application circuits are shown which take advantage of the wide input common-mode voltage range which includes ground. In most cases, input biasing is not required and input voltages which range to ground can easily be accommodated.

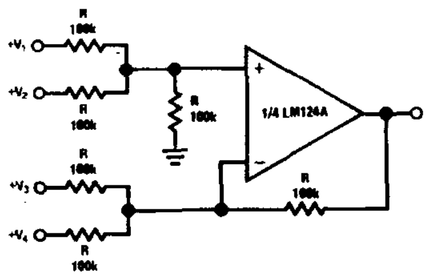
## Typical Single-Supply Applications ($V^{+} = 5.0\ V_{DC}$)

### Non-Inverting DC Gain (0V Input = 0V Output)




TL/H/9299–5

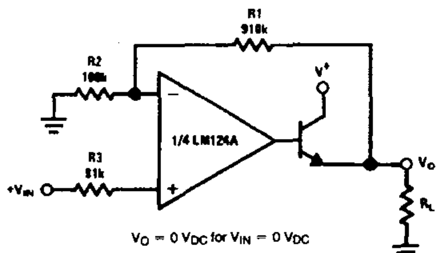
### DC Summing Amplifier ($V_{IN}$'s $\geq 0\ V_{DC}$ and $V_O \geq V_{DC}$)




TL/H/9299–6

Where: $V_O = V_1 + V_2 - V_3 - V_4$
$(V_1 + V_2) \geq (V_3 + V_4)$ to keep $V_O > 0\ V_{DC}$

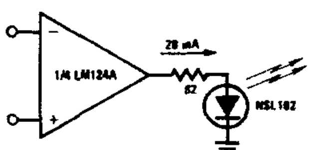
### Power Amplifier




$V_O = 0\ V_{DC}$ for $V_{IN} = 0\ V_{DC}$
$A_V = 10$

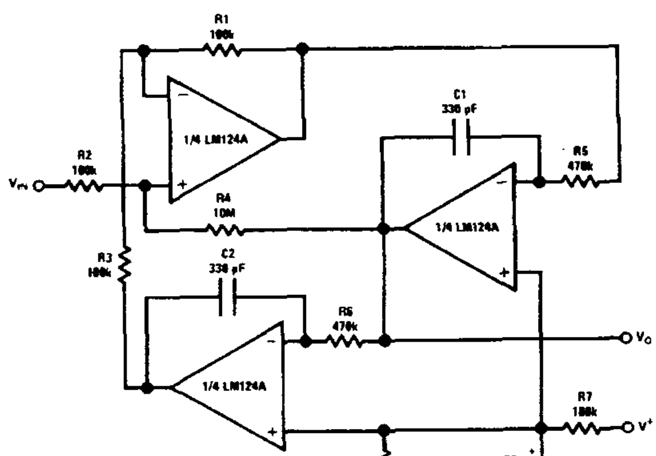
TL/H/9299–7

### LED Driver




TL/H/9299–8

### "BI-QUAD" RC Active Bandpass Filter

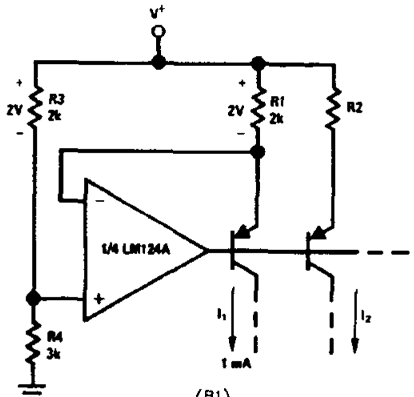



$f_o = 1\ kHz$
$Q = 50$
$A_V = 100\ (40\ dB)$

TL/H/9299–9

## Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$) (Continued)

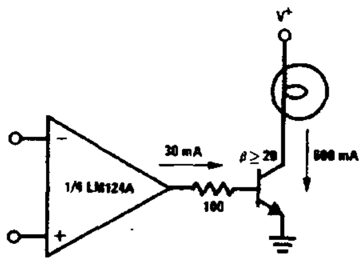
**Fixed Current Sources**




$I_2 = \left(\frac{R1}{R2}\right) I_1$

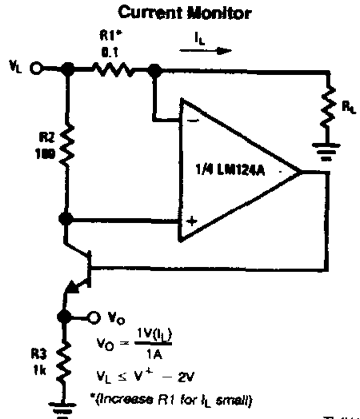
TL/H/9299-10

**Lamp Driver**




TL/H/9299-11

**Current Monitor**



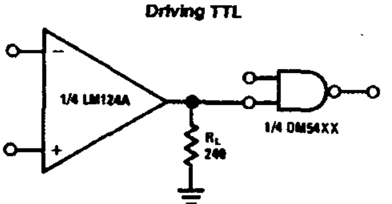

$V_O = \frac{1V(I_L)}{1A}$

$V_L \le V^+ - 2V$

*(Increase R1 for $I_L$ small)

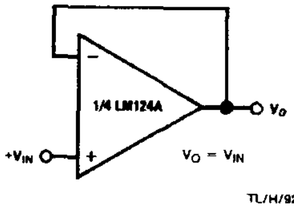
TL/H/9299-12

**Driving TTL**



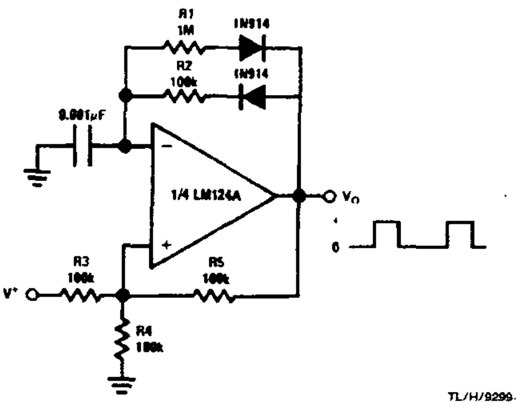

TL/H/9299-13

**Voltage Follower**




TL/H/9299-14

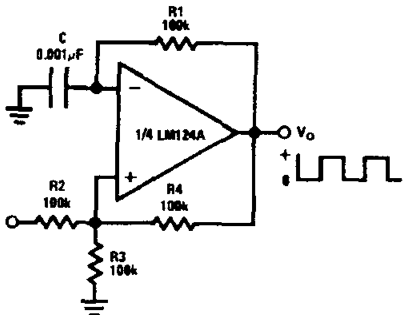
**Pulse Generator**




TL/H/9299-15

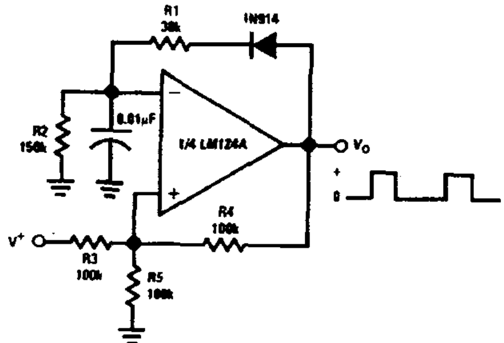
## Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$) (Continued)

### Squarewave Oscillator



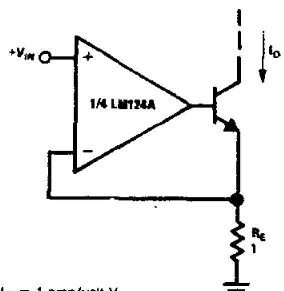

TL/H/9299-16

### Pulse Generator




TL/H/9299-17

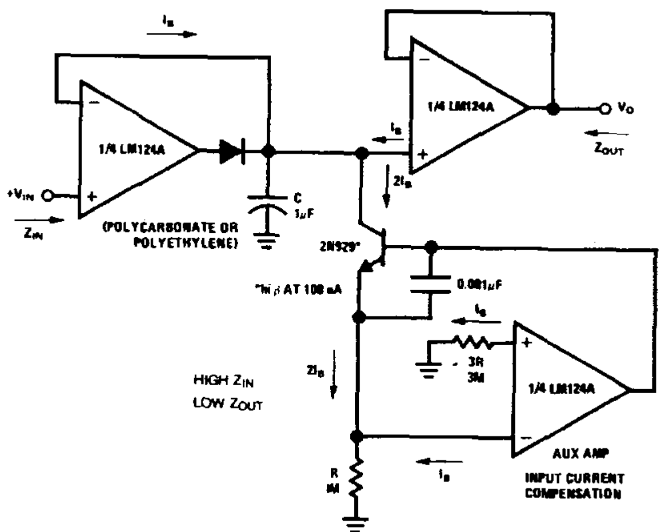
### High Compliance Current Sink




$I_O$ = 1 amp/volt $V_{IN}$
(Increase $R_E$ for $I_O$ small)

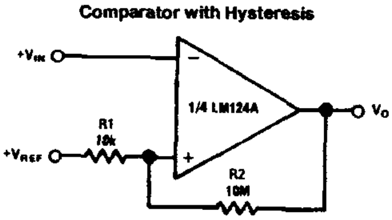
TL/H/9299-18

### Low Drift Peak Detector



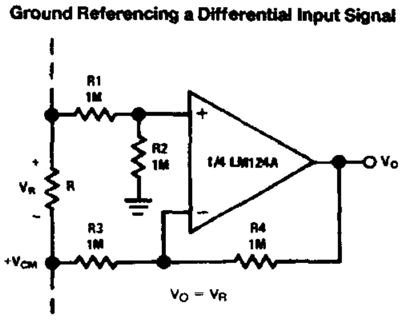

TL/H/9299-19

### Comparator with Hysteresis




TL/H/9299-20

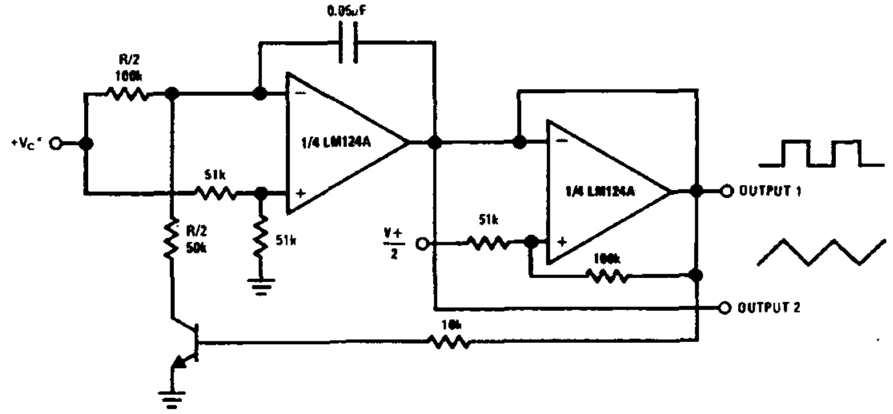
### Ground Referencing a Differential Input Signal




TL/H/9299-21

## Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$) (Continued)

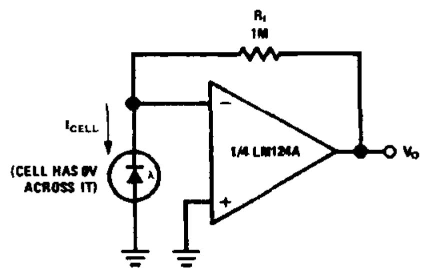
### Voltage Controlled Oscillator Circuit




TL/H/9299–22

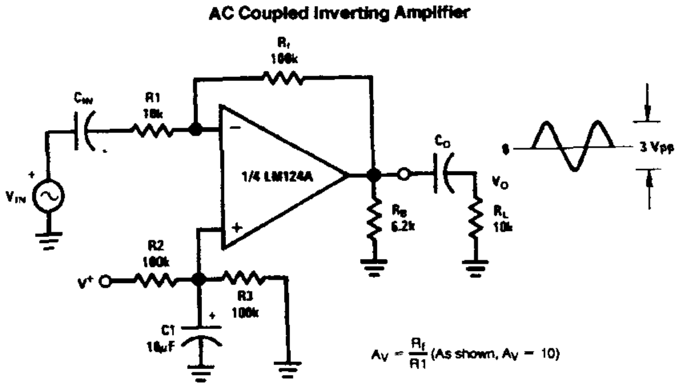
*Wide control voltage range: $0\ V_{DC} \leq V_C \leq 2\ (V^+ - 1.5\ V_{DC})$

### Photo Voltaic-Cell Amplifier




TL/H/9299–23

### AC Coupled Inverting Amplifier

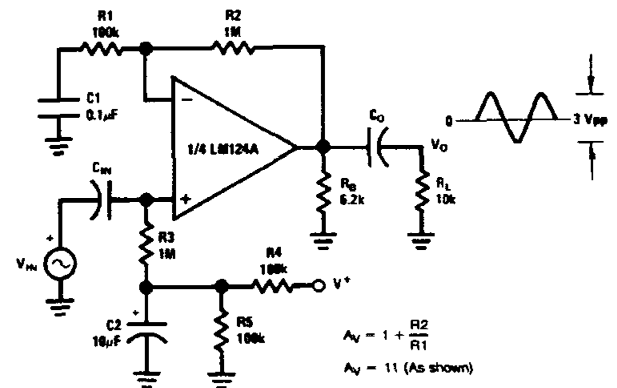



$A_V = \frac{R_f}{R1}$ (As shown, $A_V = 10$)

TL/H/9299–24

## Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$) (Continued)

**AC Coupled Non-Inverting Amplifier**

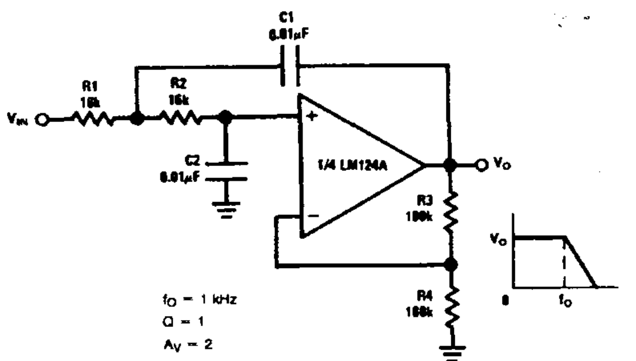



$A_V = 1 + \frac{R2}{R1}$

$A_V = 11$ (As shown)

TL/H/9299–25

**DC Coupled Low-Pass RC Active Filter**



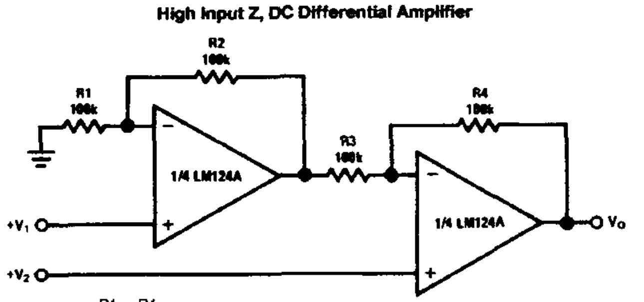

$f_O = 1$ kHz

$Q = 1$

$A_V = 2$

TL/H/9299–26

**High Input Z, DC Differential Amplifier**




TL/H/9299–27

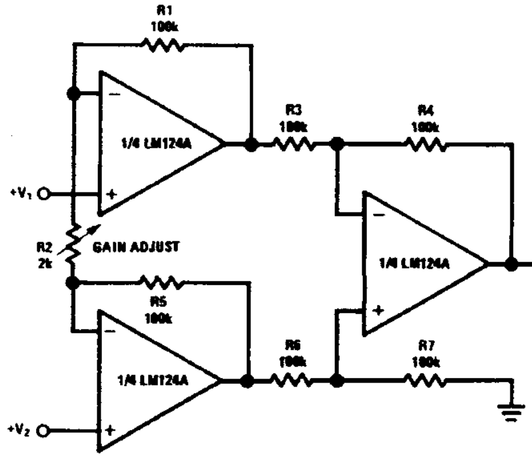
For $\frac{R1}{R2} = \frac{R4}{R3}$ (CMRR depends on this resistor ratio match)

$V_O = 1 + \frac{R4}{R3}(V_2 - V_1)$

As shown: $V_O = 2(V_2 - V_1)$

## Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$) (Continued)

**High Input Z Adjustable-Gain DC Instrumentation Amplifier**



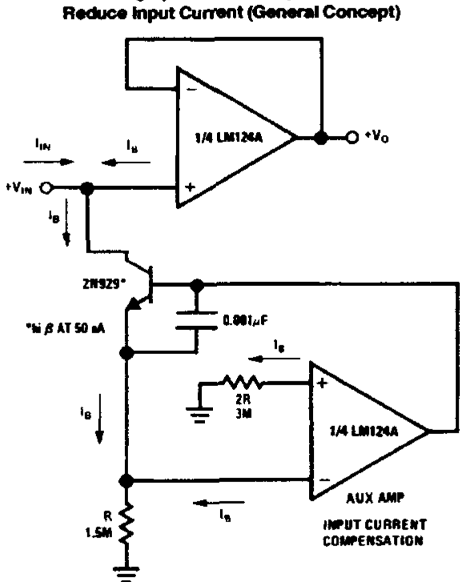

TL/H/9299–28

If R1 = R5 & R3 = R4 = R6 = R7 (CMRR depends on match)

$$V_O = 1 + \frac{2R1}{R2}(V_2 - V_1)$$

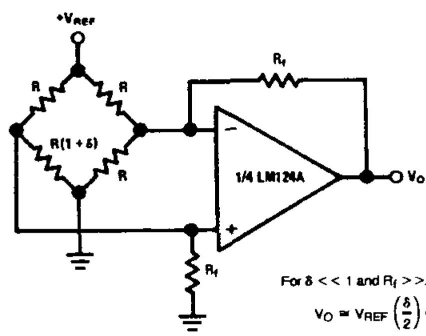
As shown $V_O = 101\ (V_2 - V_1)$

**Using Symmetrical Amplifiers to Reduce Input Current (General Concept)**




TL/H/9299–29

**Bridge Current Amplifier**



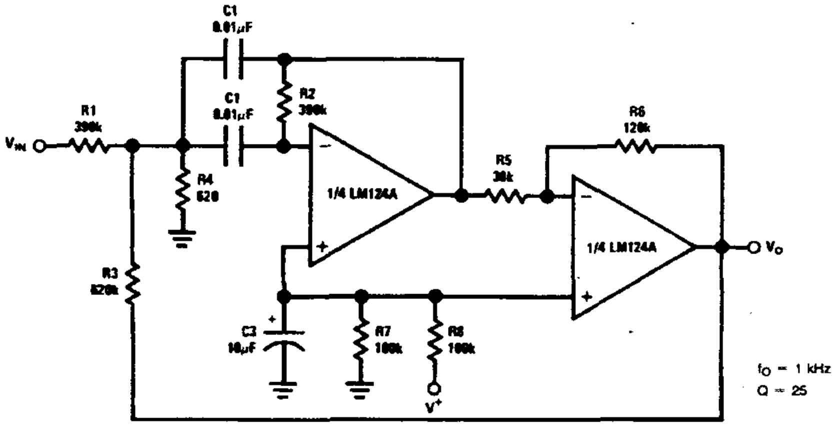

For $\delta << 1$ and $R_f >> R$

$$V_O \cong V_{REF}\left(\frac{\delta}{2}\right)\frac{R_f}{R}$$

TL/H/9299–30

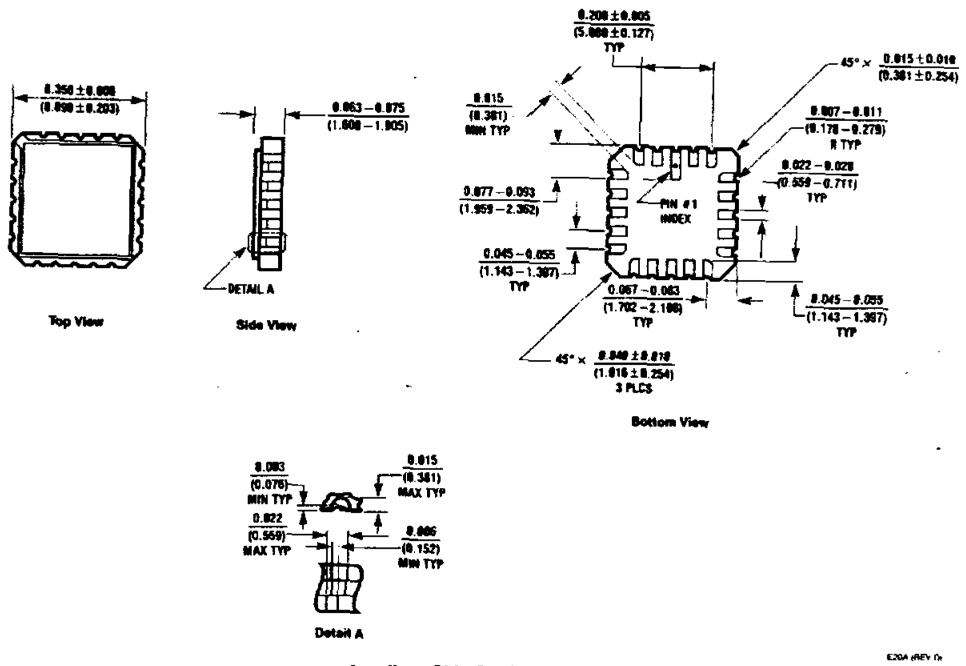
## Typical Single-Supply Applications ($V^+ = 5.0\ V_{DC}$) (Continued)

**Bandpass Active Filter**

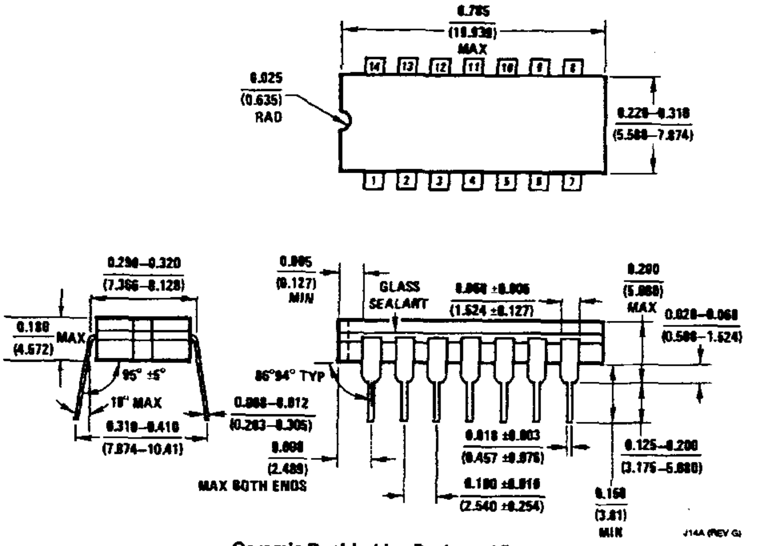



TL/H/9299–31

## Physical Dimensions inches (millimeters)

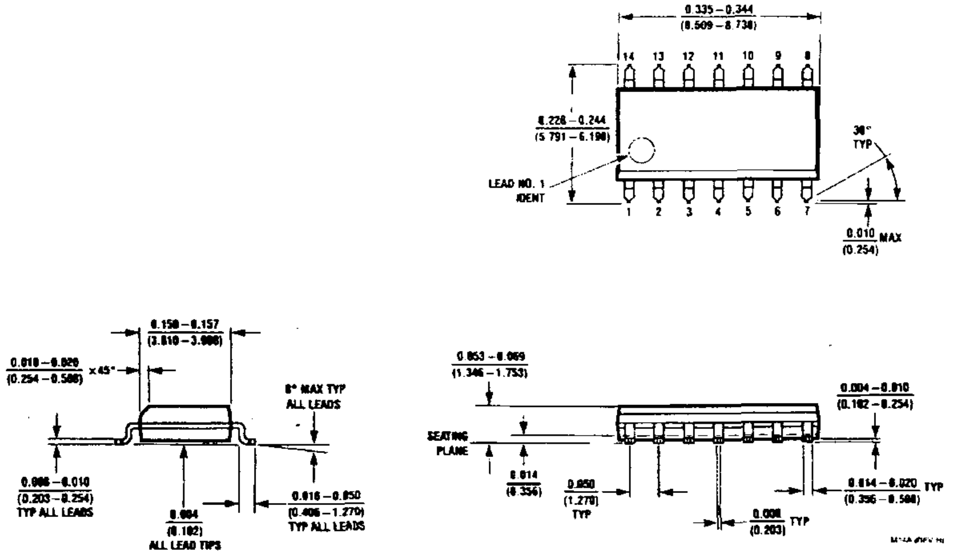


Leadless Chip Carrier Package
Order Number LM124AE/883 or LM124E/883
NS Package Number E20A

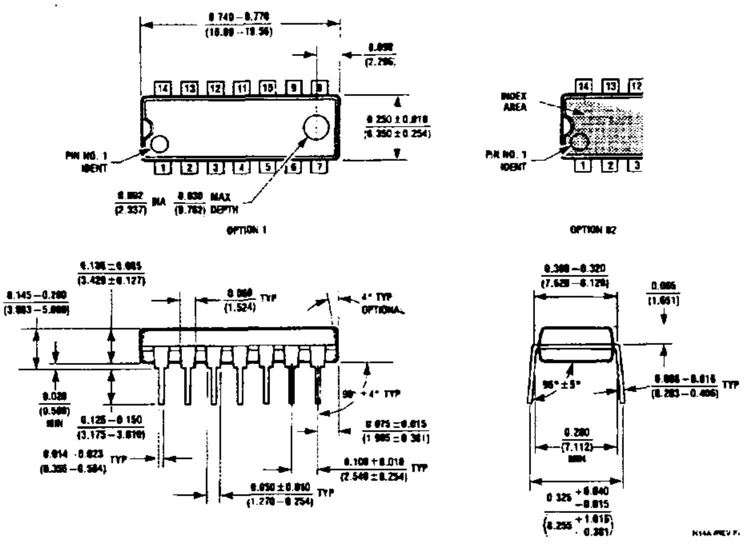


Ceramic Dual-In-Line Package (J)
Order Number LM124J, LM124AJ, LM124AJ/883, LM124J/883, LM224J, LM224AJ or LM324J
NS Package Number J14A

## Physical Dimensions inches (millimeters) (Continued)

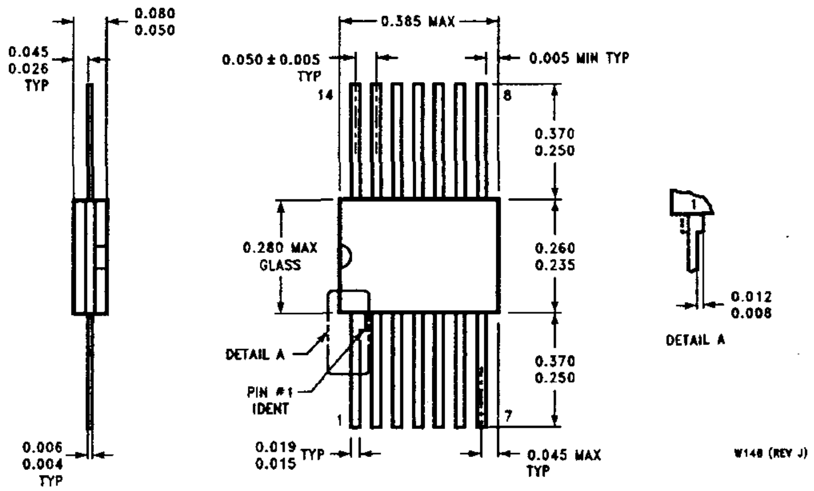


**S.O. Package (M)**
**Order Number LM324M, LM324AM or LM2902M**
**NS Package Number M14A**



**Molded Dual-In-Line Package (N)**
**Order Number LM324N, LM324AN or LM2902N**
**NS Package Number N14A**

## Physical Dimensions inches (millimeters) (Continued)




**Ceramic Flatpak Package**
**Order Number LM124AW/883 or LM124W/883**
**NS Package Number W14B**

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2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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National Semiconductor

# LM35/LM35A/LM35C/LM35CA/LM35D Precision Centigrade Temperature Sensors

## General Description

The LM35 series are precision integrated-circuit temperature sensors, whose output voltage is linearly proportional to the Celsius (Centigrade) temperature. The LM35 thus has an advantage over linear temperature sensors calibrated in ° Kelvin, as the user is not required to subtract a large constant voltage from its output to obtain convenient Centigrade scaling. The LM35 does not require any external calibration or trimming to provide typical accuracies of ±¼°C at room temperature and ±¾°C over a full −55 to +150°C temperature range. Low cost is assured by trimming and calibration at the wafer level. The LM35's low output impedance, linear output, and precise inherent calibration make interfacing to readout or control circuitry especially easy. It can be used with single power supplies, or with plus and minus supplies. As it draws only 60 μA from its supply, it has very low self-heating, less than 0.1°C in still air. The LM35 is rated to operate over a −55° to +150°C temperature range, while the LM35C is rated for a −40° to +110°C range (−10° with improved accuracy). The LM35 series is available packaged in hermetic TO-46 transistor packages, while the LM35C, LM35CA, and LM35D are also available in the plastic TO-92 transistor package. The LM35D is also available in an 8-lead surface mount small outline package and a plastic TO-202 package.

## Features

- Calibrated directly in ° Celsius (Centigrade)
- Linear + 10.0 mV/°C scale factor
- 0.5°C accuracy guaranteeable (at +25°C)
- Rated for full −55° to +150°C range
- Suitable for remote applications
- Low cost due to wafer-level trimming
- Operates from 4 to 30 volts
- Less than 60 μA current drain
- Low self-heating, 0.08°C in still air
- Nonlinearity only ±¼°C typical
- Low impedance output, 0.1 Ω for 1 mA load

## Connection Diagrams

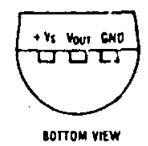
TO-46
**Metal Can Package***


TL/H/5516-1

*Case is connected to negative pin (GND)

Order Number LM35H, LM35AH, LM35CH, LM35CAH or LM35DH
See NS Package Number H03H

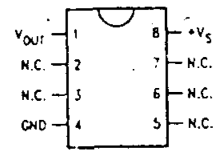
TO-92
**Plastic Package**




TL/H/5516-2

Order Number LM35CZ, LM35CAZ or LM35DZ
See NS Package Number Z03A

SO-8
Small Outline Molded Package

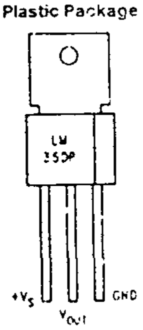



TL/H/5516-21

Top View
N.C. = No Connection

Order Number LM35DM
See NS Package Number M08A

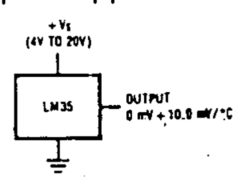
TO-202
Plastic Package




TL/H/5516-24

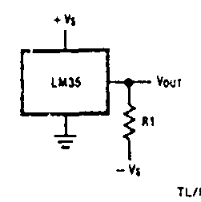
Order Number LM35DP
See NS Package Number P03A

## Typical Applications




TL/H/5516-3

**FIGURE 1. Basic Centigrade Temperature Sensor (+2°C to +150°C)**




TL/H/5516-4

Choose $R_1 = -V_S/50\ \mu A$

$V_{OUT} = +1{,}500$ mV at +150°C
= +250 mV at +25°C
= −550 mV at −55°C

**FIGURE 2. Full-Range Centigrade Temperature Sensor**

## Absolute Maximum Ratings (Note 10)

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.**

| | |
|---|---|
| Supply Voltage | +35V to −0.2V |
| Output Voltage | +6V to −1.0V |
| Output Current | 10 mA |
| Storage Temp., TO-46 Package, | −60°C to +180°C |
| TO-92 Package, | −60°C to +150°C |
| SO-8 Package, | −65°C to +150°C |
| TO-202 Package, | −65°C to +150°C |
| Lead Temp.: | |
| TO-46 Package, (Soldering, 10 seconds) | 300°C |
| TO-92 Package, (Soldering, 10 seconds) | 260°C |
| TO-202 Package, (Soldering, 10 seconds) | +230°C |
| SO Package (Note 12): | |
| Vapor Phase (60 seconds) | 215°C |
| Infrared (15 seconds) | 220°C |
| ESD Susceptibility (Note 11) | 2500V |
| Specified Operating Temperature Range: $T_{MIN}$ to $T_{MAX}$ (Note 2) | |
| LM35, LM35A | −55°C to +150°C |
| LM35C, LM35CA | −40°C to +110°C |
| LM35D | 0°C to +100°C |

## Electrical Characteristics (Note 1) (Note 6)

| Parameter | Conditions | LM35A | | | LM35CA | | | Units (Max.) |
|---|---|---|---|---|---|---|---|---|
| | | Typical | Tested Limit (Note 4) | Design Limit (Note 5) | Typical | Tested Limit (Note 4) | Design Limit (Note 5) | |
| Accuracy (Note 7) | $T_A = +25°C$ | ±0.2 | ±0.5 | | ±0.2 | ±0.5 | | °C |
| | $T_A = -10°C$ | ±0.3 | | | ±0.3 | | ±1.0 | °C |
| | $T_A = T_{MAX}$ | ±0.4 | ±1.0 | | ±0.4 | ±1.0 | | °C |
| | $T_A = T_{MIN}$ | ±0.4 | ±1.0 | | ±0.4 | | ±1.5 | °C |
| Nonlinearity (Note 8) | $T_{MIN} \le T_A \le T_{MAX}$ | **±0.18** | | **±0.35** | **±0.15** | | **±0.3** | °C |
| Sensor Gain (Average Slope) | $T_{MIN} \le T_A \le T_{MAX}$ | **+10.0** | **+9.9, +10.1** | | **+10.0** | | **+9.9, +10.1** | mV/°C |
| Load Regulation (Note 3) $0 \le I_L \le 1$ mA | $T_A = +25°C$ | ±0.4 | ±1.0 | | ±0.4 | ±1.0 | | mV/mA |
| | $T_{MIN} \le T_A \le T_{MAX}$ | **±0.5** | | **±3.0** | **±0.5** | | **±3.0** | mV/mA |
| Line Regulation (Note 3) | $T_A = +25°C$ | ±0.01 | ±0.05 | | ±0.01 | ±0.05 | | mV/V |
| | $4V \le V_S \le 30V$ | **±0.02** | | **±0.1** | **±0.02** | | **±0.1** | mV/V |
| Quiescent Current (Note 9) | $V_S = +5V$, +25°C | 56 | 67 | | 56 | 67 | | µA |
| | $V_S = +5V$ | **105** | | **131** | **91** | | **114** | µA |
| | $V_S = +30V$, +25°C | 56.2 | 68 | | 56.2 | 68 | | µA |
| | $V_S = +30V$ | **105.5** | | **133** | **91.5** | | **116** | µA |
| Change of Quiescent Current (Note 3) | $4V \le V_S \le 30V$, +25°C | 0.2 | 1.0 | | 0.2 | 1.0 | | µA |
| | $4V \le V_S \le 30V$ | **0.5** | | **2.0** | **0.5** | | **2.0** | µA |
| Temperature Coefficient of Quiescent Current | | **+0.39** | | **+0.5** | **+0.39** | | **+0.5** | µA/°C |
| Minimum Temperature for Rated Accuracy | In circuit of *Figure 1*, $I_L = 0$ | +1.5 | | +2.0 | +1.5 | | +2.0 | °C |
| Long Term Stability | $T_J = T_{MAX}$, for 1000 hours | ±0.08 | | | ±0.08 | | | °C |

**Note 1:** Unless otherwise noted, these specifications apply: $-55°C \le T_J \le +150°C$ for the LM35 and LM35A; $-40° \le T_J \le +110°C$ for the LM35C and LM35CA; and $0° \le T_J \le +100°C$ for the LM35D. $V_S = +5Vdc$ and $I_{LOAD} = 50\ \mu A$, in the circuit of *Figure 2*. These specifications also apply from +2°C to $T_{MAX}$ in the circuit of *Figure 1*. Specifications in boldface apply over the full rated temperature range.

**Note 2:** Thermal resistance of the TO-46 package is 400°C/W, junction to ambient, and 24°C/W junction to case. Thermal resistance of the TO-92 package is 180°C/W junction to ambient. Thermal resistance of the small outline molded package is 220°C/W junction to ambient. Thermal resistance of the TO-202 package is 85°C/W junction to ambient. For additional thermal resistance information see table in the Applications section.

## Electrical Characteristics (Note 1) (Note 6) (Continued)

| Parameter | Conditions | LM35 Typical | LM35 Tested Limit (Note 4) | LM35 Design Limit (Note 5) | LM35C, LM35D Typical | LM35C, LM35D Tested Limit (Note 4) | LM35C, LM35D Design Limit (Note 5) | Units (Max.) |
|---|---|---|---|---|---|---|---|---|
| Accuracy, LM35, LM35C (Note 7) | $T_A = +25°C$ | ±0.4 | ±1.0 | | ±0.4 | ±1.0 | | °C |
| | $T_A = -10°C$ | ±0.5 | | | ±0.5 | | ±1.5 | °C |
| | $T_A = T_{MAX}$ | ±0.8 | ±1.5 | | ±0.8 | | ±1.5 | °C |
| | $T_A = T_{MIN}$ | ±0.8 | | ±1.5 | ±0.8 | | ±2.0 | °C |
| Accuracy, LM35D (Note 7) | $T_A = +25°C$ | | | | ±0.6 | ±1.5 | | °C |
| | $T_A = T_{MAX}$ | | | | ±0.9 | | ±2.0 | °C |
| | $T_A = T_{MIN}$ | | | | ±0.9 | | ±2.0 | °C |
| Nonlinearity (Note 8) | $T_{MIN} \le T_A \le T_{MAX}$ | **±0.3** | | **±0.5** | **±0.2** | | **±0.5** | °C |
| Sensor Gain (Average Slope) | $T_{MIN} \le T_A \le T_{MAX}$ | **+10.0** | **+9.8, +10.2** | | **+10.0** | | **+9.8, +10.2** | mV/°C |
| Load Regulation (Note 3) $0 \le I_L \le 1$ mA | $T_A = +25°C$ | ±0.4 | ±2.0 | | ±0.4 | ±2.0 | | mV/mA |
| | $T_{MIN} \le T_A \le T_{MAX}$ | **±0.5** | | **±5.0** | **±0.5** | | **±5.0** | mV/mA |
| Line Regulation (Note 3) | $T_A = +25°C$ | ±0.01 | ±0.1 | | ±0.01 | ±0.1 | | mV/V |
| | $4V \le V_S \le 30V$ | **±0.02** | | **±0.2** | **±0.02** | | **±0.2** | mV/V |
| Quiescent Current (Note 9) | $V_S = +5V$, +25°C | 56 | 80 | | 56 | 80 | | μA |
| | $V_S = +5V$ | **105** | | **158** | **91** | | **138** | μA |
| | $V_S = +30V$, +25°C | 56.2 | 82 | | 56.2 | 82 | | μA |
| | $V_S = +30V$ | **105.5** | | **161** | **91.5** | | **141** | μA |
| Change of Quiescent Current (Note 3) | $4V \le V_S \le 30V$, +25°C | 0.2 | 2.0 | | 0.2 | 2.0 | | μA |
| | $4V \le V_S \le 30V$ | **0.5** | | **3.0** | **0.5** | | **3.0** | μA |
| Temperature Coefficient of Quiescent Current | | **+0.39** | | **+0.7** | **+0.39** | | **+0.7** | μA/°C |
| Minimum Temperature for Rated Accuracy | In circuit of *Figure 1*, $I_L = 0$ | +1.5 | | +2.0 | +1.5 | | +2.0 | °C |
| Long Term Stability | $T_J = T_{MAX}$, for 1000 hours | ±0.08 | | | ±0.08 | | | °C |

**Note 3:** Regulation is measured at constant junction temperature, using pulse testing with a low duty cycle. Changes in output due to heating effects can be computed by multiplying the internal dissipation by the thermal resistance.

**Note 4:** Tested Limits are guaranteed and 100% tested in production.

**Note 5:** Design Limits are guaranteed (but not 100% production tested) over the indicated temperature and supply voltage ranges. These limits are not used to calculate outgoing quality levels.

**Note 6:** Specifications in boldface apply over the full rated temperature range.

**Note 7:** Accuracy is defined as the error between the output voltage and 10mv/°C times the device's case temperature, at specified conditions of voltage, current, and temperature (expressed in °C).

**Note 8:** Nonlinearity is defined as the deviation of the output-voltage-versus-temperature curve from the best-fit straight line, over the device's rated temperature range.

**Note 9:** *Quiescent current is defined in the circuit of Figure 1.*

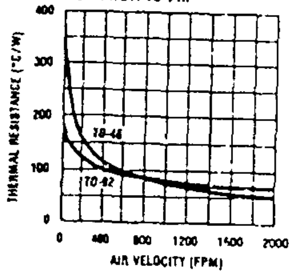
**Note 10:** Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its rated operating conditions. See Note 1.

**Note 11:** Human body model, 100 pF discharged through a 1.5 kΩ resistor.

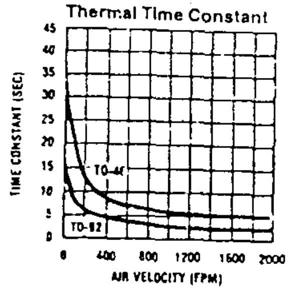
**Note 12:** See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" or the section titled "Surface Mount" found in a current National Semiconductor Linear Data Book for other methods of soldering surface mount devices.

# Typical Performance Characteristics

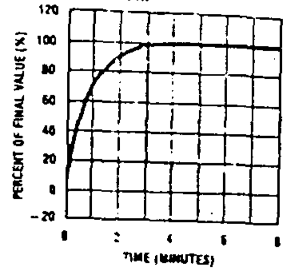
**Thermal Resistance Junction to Air**



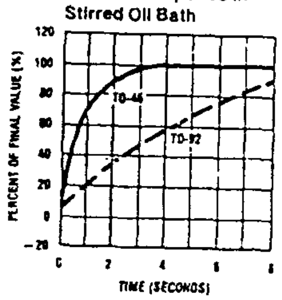

**Thermal Time Constant**



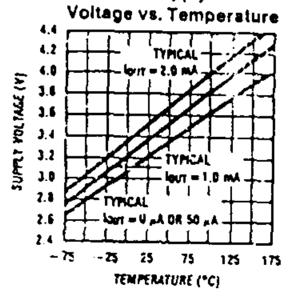

**Thermal Response in Still Air**



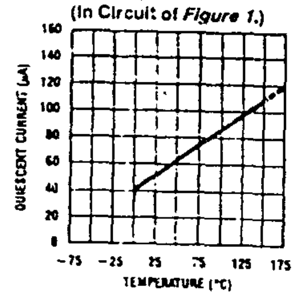

**Thermal Response in Stirred Oil Bath**




**Minimum Supply Voltage vs. Temperature**




**Quiescent Current vs. Temperature (In Circuit of *Figure 1.*)**

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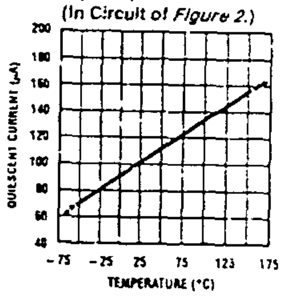
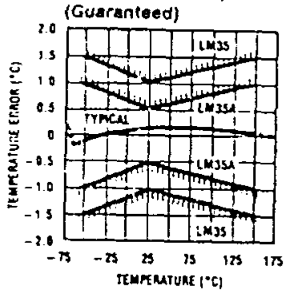
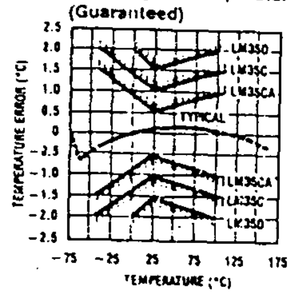
**Quiescent Current vs. Temperature (In Circuit of *Figure 2.*)**




**Accuracy vs. Temperature (Guaranteed)**




**Accuracy vs. Temperature (Guaranteed)**

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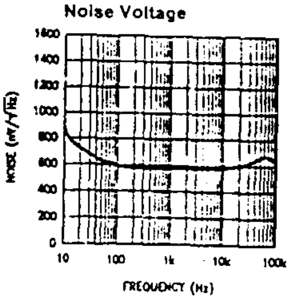
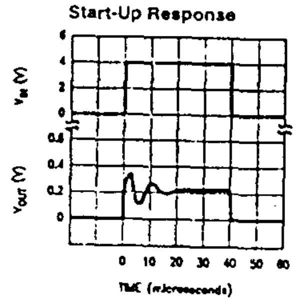
**Noise Voltage**




**Start-Up Response**

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## Applications

The LM35 can be applied easily in the same way as other integrated-circuit temperature sensors. It can be glued or cemented to a surface and its temperature will be within about 0.01°C of the surface temperature.

This presumes that the ambient air temperature is almost the same as the surface temperature; if the air temperature were much higher or lower than the surface temperature, the actual temperature of the LM35 die would be at an intermediate temperature between the surface temperature and the air temperature. This is expecially true for the TO-92 plastic package, where the copper leads are the principal thermal path to carry heat into the device, so its temperature might be closer to the air temperature than to the surface temperature.

To minimize this problem, be sure that the wiring to the LM35, as it leaves the device, is held at the same temperature as the surface of interest. The easiest way to do this is to cover up these wires with a bead of epoxy which will insure that the leads and wires are all at the same temperature as the surface, and that the LM35 die's temperature will not be affected by the air temperature.

The TO-46 metal package can also be soldered to a metal surface or pipe without damage. Of course, in that case the V− terminal of the circuit will be grounded to that metal. Alternatively, the LM35 can be mounted inside a sealed-end metal tube, and can then be dipped into a bath or screwed into a threaded hole in a tank. As with any IC, the LM35 and accompanying wiring and circuits must be kept insulated and dry, to avoid leakage and corrosion. This is especially true if the circuit may operate at cold temperatures where condensation can occur. Printed-circuit coatings and varnishes such as Humiseal and epoxy paints or dips are often used to insure that moisture cannot corrode the LM35 or its connections.

These devices are sometimes soldered to a small light-weight heat fin, to decrease the thermal time constant and speed up the response in slowly-moving air. On the other hand, a small thermal mass may be added to the sensor, to give the steadiest reading despite small deviations in the air temperature.

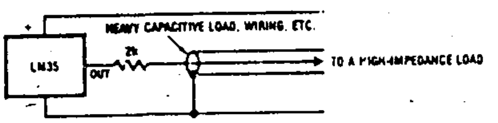
**Temperature Rise of LM35 Due To Self-heating (Thermal Resistance)**

| | TO-46, no heat sink | TO-46, small heat fin* | TO-92, no heat sink | TO-92, small heat fin** | SO-8 no heat sink | SO-8 small heat fin** | TO-202 no heat sink | TO-202*** small heat fin |
|---|---|---|---|---|---|---|---|---|
| Still air | 400°C/W | 100°C/W | 180°C/W | 140°C/W | 220°C/W | 110°C/W | 85°C/W | 60°C/W |
| Moving air | 100°C/W | 40°C/W | 90°C/W | 70°C/W | 105°C/W | 90°C/W | 25°C/W | 40°C/W |
| Still oil | 100°C/W | 40°C/W | 90°C/W | 70°C/W | | | | |
| Stirred oil | 50°C/W | 30°C/W | 45°C/W | 40°C/W | | | | |
| (Clamped to metal, Infinite heat sink) | (24°C/W) | | | | (55°C/W) | | (23°C/W) | |

* Wakefield type 201, or 1" disc of 0.020" sheet brass, soldered to case, or similar

** TO-92 and SO-8 packages glued and leads soldered to 1" square of 1/16" printed circuit board with 2 oz. foil or similar.

## Typical Applications (Continued)




TL/H/5516-19

FIGURE 3. LM35 with Decoupling from Capacitive Load

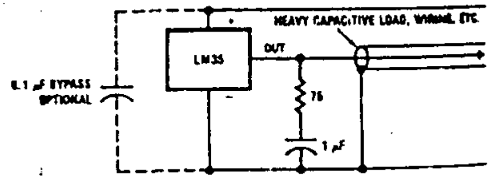



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FIGURE 4. LM35 with R-C Damper

### CAPACITIVE LOADS

Like most micropower circuits, the LM35 has a limited ability to drive heavy capacitive loads. The LM35 by itself is able to drive 50 pf without special precautions. If heavier loads are anticipated, it is easy to isolate or decouple the load with a resistor; see *Figure 3*. Or you can improve the tolerance of capacitance with a series R-C damper from output to ground; see *Figure 4*.

When the LM35 is applied with a 200Ω load resistor as shown in *Figure 5, 6,* or *8,* it is relatively immune to wiring capacitance because the capacitance forms a bypass from ground to input, not on the output. However, as with any linear circuit connected to wires in a hostile environment, its performance can be affected adversely by intense electromagnetic sources such as relays, radio transmitters, motors with arcing brushes, SCR transients, etc, as its wiring can act as a receiving antenna and its internal junctions can act as rectifiers. For best results in such cases, a bypass capacitor from $V_{IN}$ to ground and a series R-C damper such as 75Ω in series with 0.2 or 1 µF from output to ground are often useful. These are shown in *Figures 13, 14,* and *16*.

## Typical Applications (Continued)

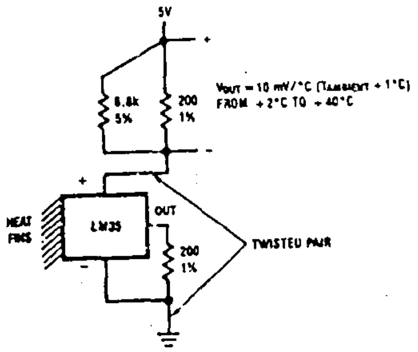


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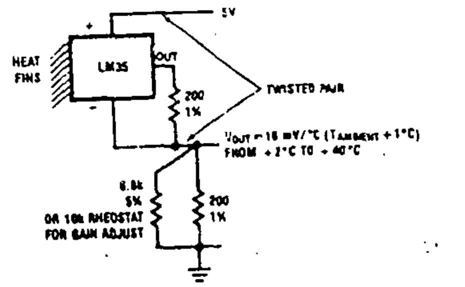
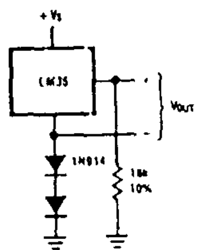
FIGURE 5. Two-Wire Remote Temperature Sensor (Grounded Sensor)



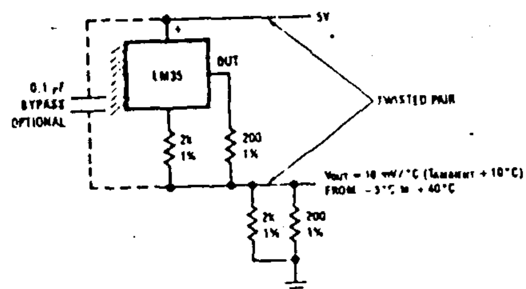

TL/H/5516-6

FIGURE 6. Two-Wire Remote Temperature Sensor (Output Referred to Ground)



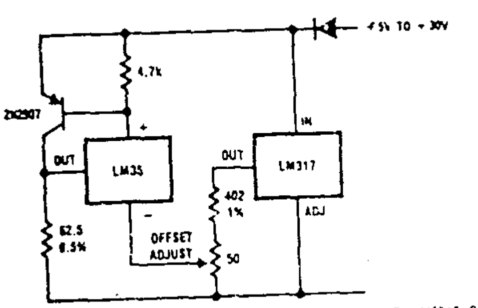

TL/H/5516-7

FIGURE 7. Temperature Sensor, Single Supply, −55° to +150°C



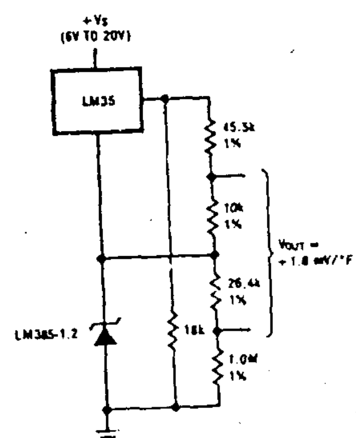

TL/H/5516-8

FIGURE 8. Two-Wire Remote Temperature Sensor (Output Referred to Ground)




TL/H/5516-9

FIGURE 9. 4-To-20 mA Current Source (0°C to +100°C)




TL/H/5516-10

FIGURE 10. Fahrenheit Thermometer

5

## Typical Applications (Continued)

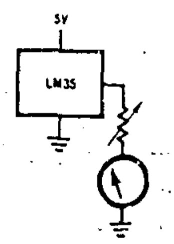



FIGURE 11. Centigrade Thermometer (Analog Meter)

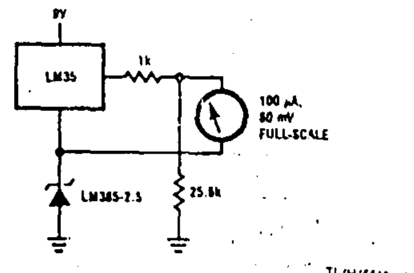



FIGURE 12. Expanded Scale Thermometer
*(50° to 80° Fahrenheit, for Example Shown)*

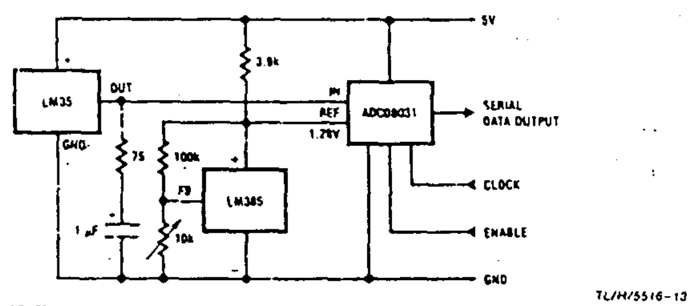



FIGURE 13. Temperature To Digital Converter (Serial Output) (+128°C Full Scale)

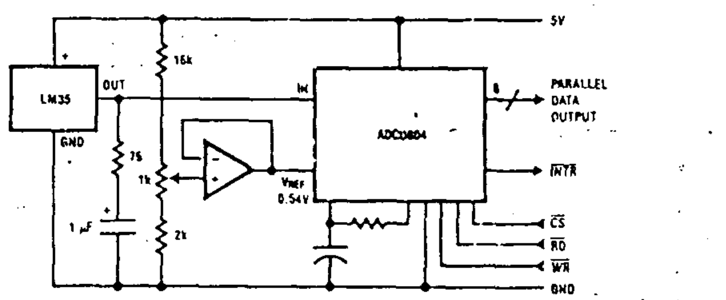
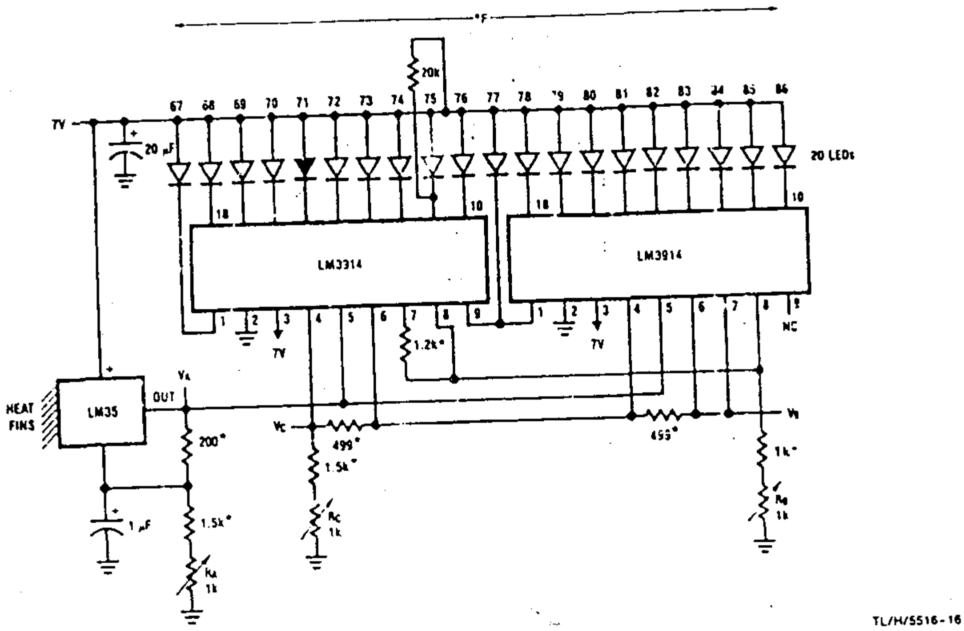



FIGURE 14. Temperature To Digital Converter (Parallel TRI-STATE® Outputs for Standard Data Bus to µP Interface) (128°C Full Scale)

## Typical Applications (Continued)




* = 1% or 2% film resistor
- Trim $R_B$ for $V_B$ = 3.075V
- Trim $R_C$ for $V_C$ = 1.955V
- Trim $R_A$ for $V_A$ = 0.075V + 100mV/°C · $T_{ambient}$
- Example, $V_A$ = 2.275V at 22°C

FIGURE 15. Bar-Graph Temperature Display (Dot Mode)

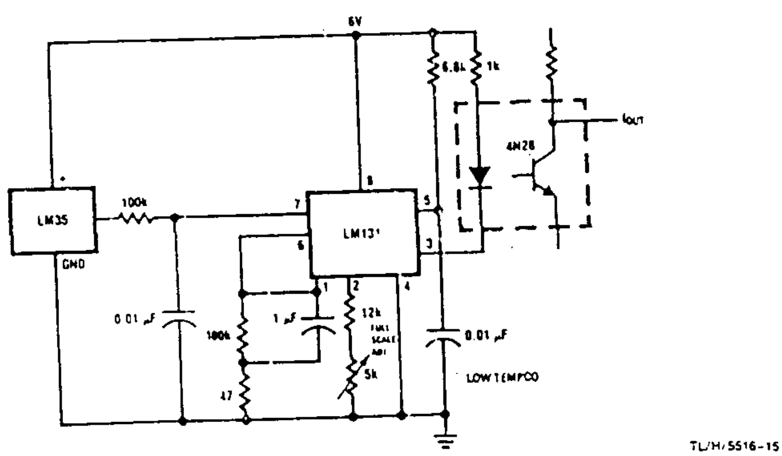
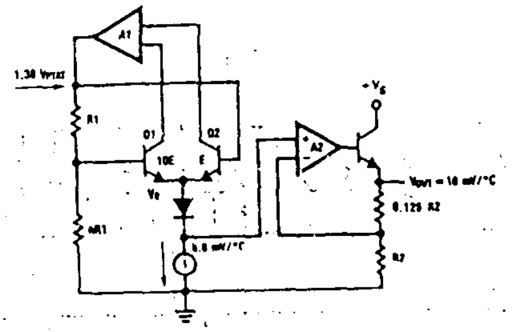



FIGURE 16. LM35 With Voltage-To-Frequency Converter And Isolated Output (2°C to +150°C; 20 Hz to 1500 Hz)

## Block Diagram




TL/H/5516–23

National Semiconductor

# LM136-2.5/LM236-2.5/LM336-2.5V Reference Diode

## General Description

The LM136-2.5/LM236-2.5 and LM336-2.5 integrated circuits are precision 2.5V shunt regulator diodes. These monolithic IC voltage references operate as a low-temperature-coefficient 2.5V zener with 0.2Ω dynamic impedance. A third terminal on the LM136-2.5 allows the reference voltage and temperature coefficient to be trimmed easily.

The LM136-2.5 series is useful as a precision 2.5V low voltage reference for digital voltmeters, power supplies or op amp circuitry. The 2.5V make it convenient to obtain a stable reference from 5V logic supplies. Further, since the LM136-2.5 operates as a shunt regulator, it can be used as either a positive or negative voltage reference.

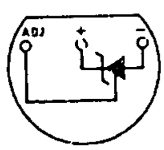
The LM136-2.5 is rated for operation over −55°C to +125°C while the LM236-2.5 is rated over a −25°C to +85°C temperature range. The LM336-2.5 is rated for operation over a 0°C to +70°C temperature range. See the connection diagrams for available packages.

## Features

- Low temperature coefficient
- Wide operating current of 400 μA to 10 mA
- 0.2Ω dynamic impedance
- ±1% initial tolerance available
- Guaranteed temperature stability
- Easily trimmed for minimum temperature drift
- Fast turn-on
- Three lead transistor package

## Connection Diagrams

**TO-92**
**Plastic Package**

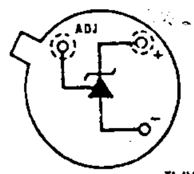



TL/H/5715-8

**Bottom View**

**Order Number LM236Z-2.5, LM236AZ-2.5, LM336Z-2.5 or LM336BZ-2.5**
**See NS Package Number Z03A**

**TO-46**
**Metal Can Package**

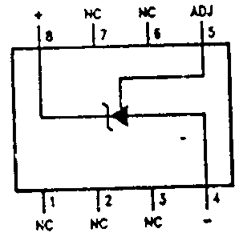



TL/H/5715-20

**Bottom View**

**Order Number LM136H-2.5, LM136H-2.5/883, LM236H-2.5, LM136AH-2.5, LM136AH-2.5/883 or LM236AH-2.5**
**See NS Package Number H03H**

**SO Package**



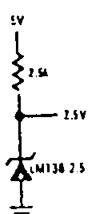

TL/H/5715-12

**Top View**

**Order Number LM236M-2.5, LM236AM-2.5, LM336M-2.5 or LM336BM-2.5**
**See NS Package Number M08A**

## Typical Applications

**2.5V Reference**

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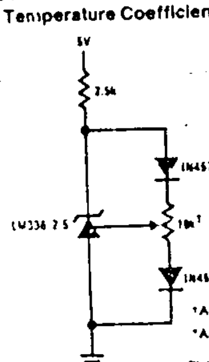
**2.5V Reference with Minimum Temperature Coefficient**




†Adjust to 2.490V
*Any silicon signal diode

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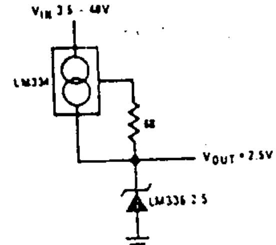
**Wide Input Range Reference**




TL/H/5715-11

## Absolute Maximum Ratings (Note 1)

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.**

| | |
|---|---|
| Reverse Current | 15 mA |
| Forward Current | 10 mA |
| Storage Temperature | −60°C to +150°C |
| *Operating Temperature Range (Note 2)* | |
| LM136 | −55°C to +150°C |
| LM236 | −25°C to +85°C |
| LM336 | 0°C to +70°C |

Soldering Information

| | |
|---|---|
| TO-92 Package (10 sec.) | 260°C |
| TO-46 Package (10 sec.) | 300°C |
| SO Package | |
| Vapor Phase (60 sec.) | 215°C |
| Infrared (15 sec.) | 220°C |

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" (Appendix D) for other methods of soldering surface mount devices.

## Electrical Characteristics (Note 3)

| Parameter | Conditions | LM136A-2.5/LM236A-2.5 LM136-2.5/LM236-2.5 | | | LM336B-2.5 LM336-2.5 | | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | |
| Reverse Breakdown Voltage | $T_A = 25°C$, $I_R = 1$ mA<br>LM136, LM236, LM336<br>LM136A, LM236A, LM336B | <br>2.440<br>2.465 | <br>2.490<br>2.490 | <br>2.540<br>2.515 | <br>2.390<br>2.440 | <br>2.490<br>2.490 | <br>2.590<br>2.540 | <br>V<br>V |
| Reverse Breakdown Change With Current | $T_A = 25°C$,<br>$400\ \mu A \le I_R \le 10$ mA | | 2.6 | 6 | | 2.6 | 10 | mV |
| Reverse Dynamic Impedance | $T_A = 25°C$, $I_R = 1$ mA, f = 100 Hz | | 0.2 | 0.6 | | 0.2 | 1 | Ω |
| Temperature Stability (Note 4) | $V_R$ Adjusted to 2.490V<br>$I_R = 1$ mA *(Figure 2)*<br>$0°C \le T_A \le 70°C$ (LM336)<br>$-25°C \le T_A \le +85°C$ (LM236H, LM236Z)<br>$-25°C \le T_A \le +85°C$ (LM236M)<br>$-55°C \le T_A \le +125°C$ (LM136) | <br><br><br><br><br> | <br><br><br>3.5<br>7.5<br>12 | <br><br><br>9<br>18<br>18 | | <br><br>1.8 | <br><br>6 | <br><br>mV<br>mV<br>mV<br>mV |
| Reverse Breakdown Change With Current | $400\ \mu A \le I_R \le 10$ mA | | 3 | 10 | | 3 | 12 | mV |
| Reverse Dynamic Impedance | $I_R = 1$ mA | | 0.4 | 1 | | 0.4 | 1.4 | Ω |
| Long Term Stability | $T_A = 25°C \pm 0.1°C$, $I_R = 1$ mA, t = 1000 hrs | | 20 | | | 20 | | ppm |

**Note 1:** Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Electrical specifications do not apply when operating the device beyond its specified operating conditions.

**Note 2:** For elevated temperature operation, $T_j$ max is:

| | |
|---|---|
| LM136 | 150°C |
| LM236 | 125°C |
| LM336 | 100°C |

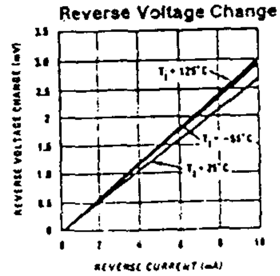
| Thermal Resistance | TO-92 | TO-46 | SO-8 |
|---|---|---|---|
| $\theta_{ja}$ (Junction to Ambient) | 180°C/W (0.4" leads)<br>170°C/W (0.125" lead) | 440°C/W | 165°C/W |
| $\theta_{ja}$ (Junction to Case) | n/a | 80°C/W | n/a |

**Note 3:** Unless otherwise specified, the LM136-2.5 is specified from $-55°C \le T_A \le +125°C$, the LM236-2.5 from $-25°C \le T_A \le +85°C$ and the LM336-2.5 from $0°C \le T_A \le +70°C$.

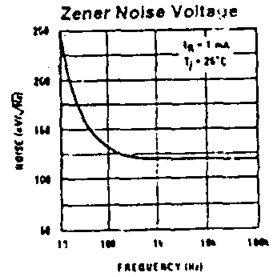
**Note 4:** Temperature stability for the LM336 and LM236 family is guaranteed by design. Design limits are guaranteed (but not 100% production tested) over the indicated temperature and supply voltage ranges. These limits are not used to calculate outgoing quality levels. Stability is defined as the maximum change in $V_{ref}$ from 25°C to $T_A$ (min) or $T_A$ (max).

## Typical Performance Characteristics

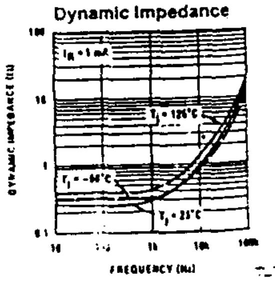
**Reverse Voltage Change**




**Zener Noise Voltage**

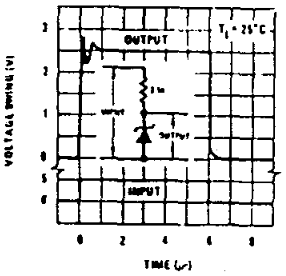



**Dynamic Impedance**

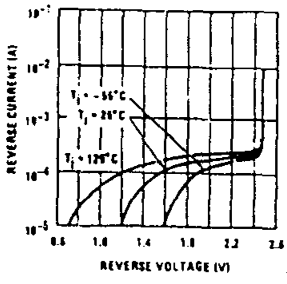


## Typical Performance Characteristics (Continued)

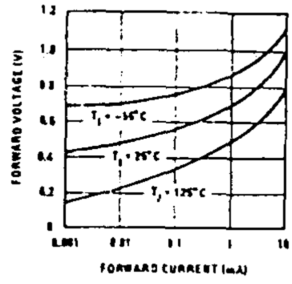
Response Time



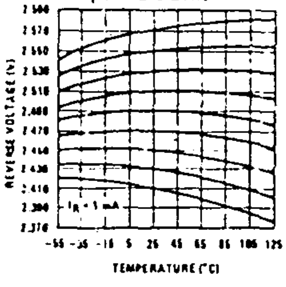

Reverse Characteristics




Forward Characteristics




Temperature Drift




TL/H/5715-3

## Application Hints

The LM136 series voltage references are much easier to use than ordinary zener diodes. Their low impedance and wide operating current range simplify biasing in almost any circuit. Further, either the breakdown voltage or the temperature coefficient can be adjusted to optimize circuit performance.

*Figure 1* shows an LM136 with a 10k potentiometer for adjusting the reverse breakdown voltage. With the addition of R1 the breakdown voltage can be adjusted without affecting the temperature coefficient of the device. The adjustment range is usually sufficient to adjust for both the initial device tolerance and inaccuracies in buffer circuitry.

If minimum temperature coefficient is desired, two diodes can be added in series with the adjustment potentiometer as shown in *Figure 2*. When the device is adjusted to 2.490V the temperature coefficient is minimized. Almost any silicon signal diode can be used for this purpose such as a 1N914, 1N4148 or a 1N457. For proper temperature compensation the diodes should be in the same thermal environment as the LM136. It is usually sufficient to mount the diodes near the LM136 on the printed circuit board. The absolute resistance of R1 is not critical and any value from 2k to 20k will work.

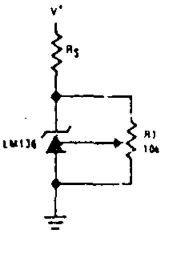



FIGURE 1. LM136 With Pot for Adjustment of Breakdown Voltage (Trim Range = ± 120 mV typical)

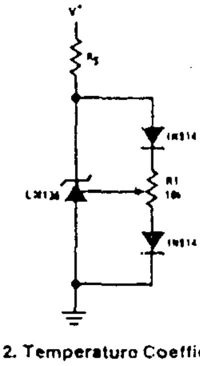



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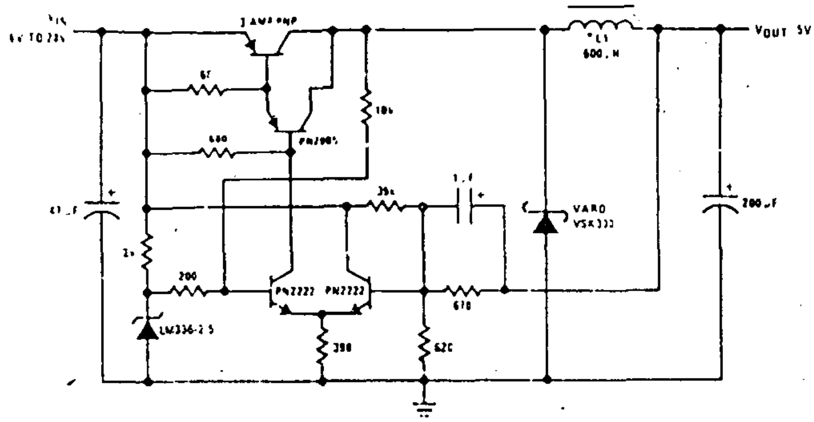
FIGURE 2. Temperature Coefficient Adjustment (Trim Range = ± 70 mV typical)

## Typical Applications (Continued)

### Low Cost 2 Amp Switching Regulator*




*L1 60 turns #16 wire on Arnold Core A-254168-2

†Efficiency = 80%

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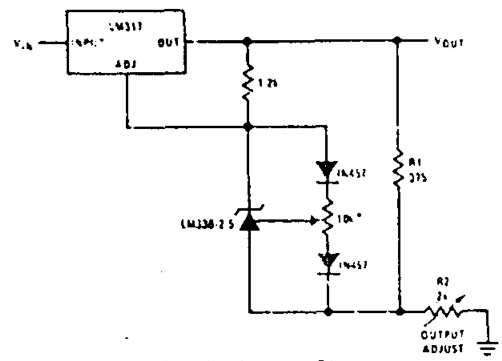
### Precision Power Regulator with Low Temperature Coefficient




*Adjust for 3.75V across R1

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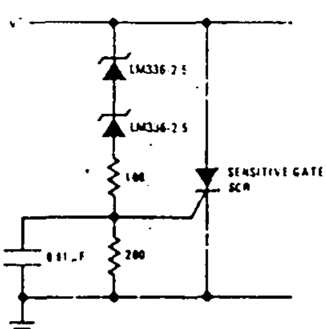
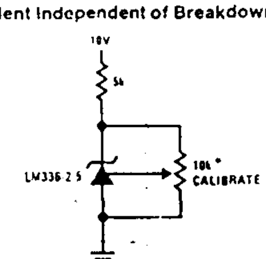
### 5V Crowbar




TL/H/5715-14

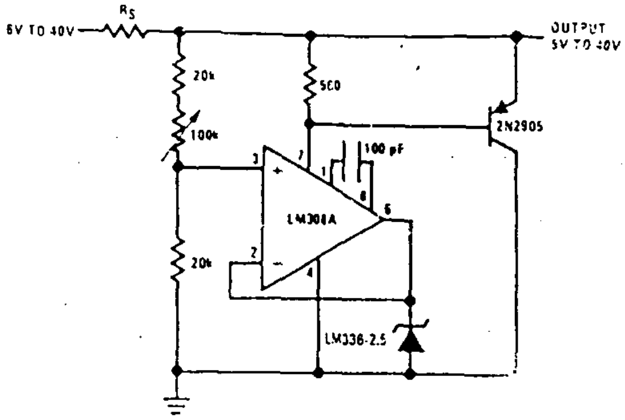
### Trimmed 2.5V Reference with Temperature Coefficient Independent of Breakdown Voltage




*Does not affect temperature coefficient

## Typical Applications (Continued)

**Adjustable Shunt Regulator**

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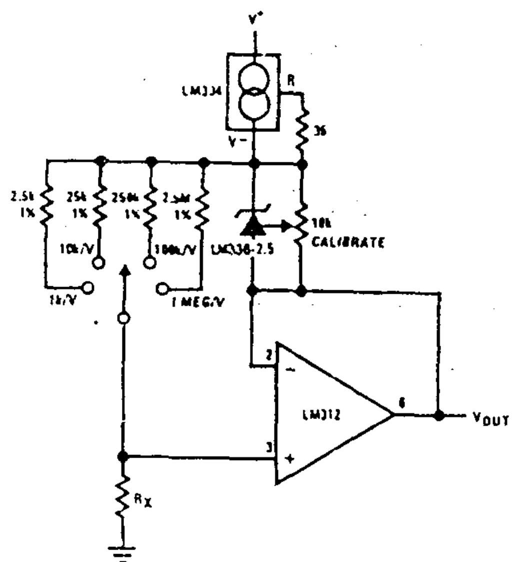
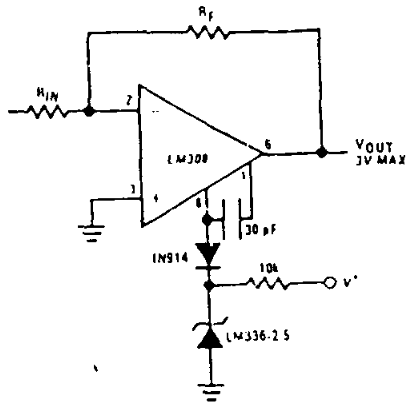
**Linear Ohmmeter**




TL/H/5715-16

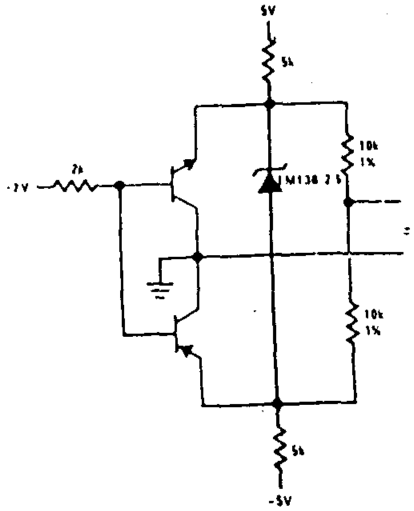
## Typical Applications (Continued)

**Op Amp with Output Clamped**



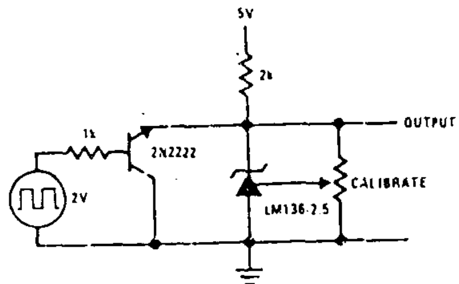

TL/H/5715-17

**Bipolar Output Reference**




TL/H/5715-18

**2.5V Square Wave Calibrator**




TL/H/5715-19

National Semiconductor Corporation

# ADC0801, ADC0802, ADC0803, ADC0804, ADC0805 8-Bit µP Compatible A/D Converters

## General Description

The ADC0801, ADC0802, ADC0803, ADC0804 and ADC0805 are CMOS 8-bit successive approximation A/D converters that use a differential potentiometric ladder—similar to the 256R products. These converters are designed to allow operation with the NSC800 and INS8080A derivative control bus with TRI-STATE® output latches directly driving the data bus. These A/Ds appear like memory locations or I/O ports to the microprocessor and no interfacing logic is needed.

Differential analog voltage inputs allow increasing the common-mode rejection and offsetting the analog zero input voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8 bits of resolution.

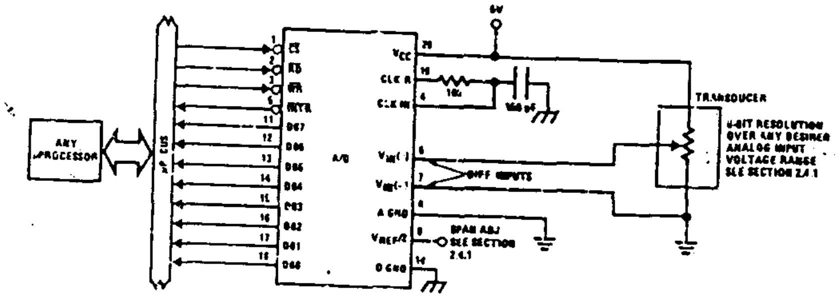
## Features

- Compatible with 8080 µP derivatives—no interfacing logic needed - access time - 135 ns
- Easy interface to all microprocessors, or operates "stand alone"
- Differential analog voltage inputs
- Logic inputs and outputs meet both MOS and TTL voltage level specifications
- Works with 2.5V (LM336) voltage reference
- On-chip clock generator
- 0V to 5V analog input voltage range with single 5V supply
- No zero adjust required
- 0.3" standard width 20-pin DIP package
- 20-pin molded chip carrier or small outline package
- Operates ratiometrically or with 5 $V_{DC}$, 2.5 $V_{DC}$, or analog span adjusted voltage reference

## Key Specifications

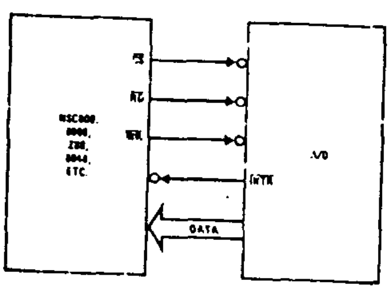
- Resolution: 8 bits
- Total error: ±¼ LSB, ±½ LSB and ±1 LSB
- Conversion time: 100 µs

## Typical Applications




TL/H/5671-1

8080 Interface




TL/H/5671-31

| Error Specification (Includes Full-Scale, Zero Error, and Non-Linearity) | | | |
|---|---|---|---|
| Part Number | Full-Scale Adjusted | $V_{REF}/2 = 2.500\ V_{DC}$ (No Adjustments) | $V_{REF}/2$ = No Connection (No Adjustments) |
| ADC0801 | ±¼ LSB | | |
| ADC0802 | | ±½ LSB | |
| ADC0803 | ±½ LSB | | |
| ADC0804 | | ±1 LSB | |
| ADC0805 | | | ±1 LSB |

## Absolute Maximum Ratings (Notes 1 & 2)

**If Military/Aerospace specified devices are required, contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | |
|---|---|
| Supply Voltage ($V_{CC}$) (Note 3) | 6.5V |
| Voltage | |
| Logic Control Inputs | −0.3V to +18V |
| At Other Input and Outputs | −0.3V to ($V_{CC}$+0.3V) |
| Lead Temp. (Soldering, 10 seconds) | |
| Dual-In-Line Package (plastic) | 260°C |
| Dual-In-Line Package (ceramic) | 300°C |
| Surface Mount Package | |
| Vapor Phase (60 seconds) | 215°C |
| Infrared (15 seconds) | 220°C |
| Storage Temperature Range | −65°C to +150°C |
| Package Dissipation at $T_A$=25°C | 875 mW |
| ESD Susceptibility (Note 10) | 800V |

## Operating Ratings (Notes 1 & 2)

| | |
|---|---|
| Temperature Range | $T_{MIN} \le T_A \le T_{MAX}$ |
| ADC0801/02LJ | $-55°C \le T_A \le +125°C$ |
| ADC0801/02/03/04LCJ | $-40°C \le T_A \le +85°C$ |
| ADC0801/02/03/05LCN | $-40°C \le T_A \le +85°C$ |
| ADC0804LCN | $0°C \le T_A \le +70°C$ |
| ADC0802/03/04LCV | $0°C \le T_A \le +70°C$ |
| ADC0802/03/04LCWM | $0°C \le T_A \le +70°C$ |
| Range of $V_{CC}$ | 4.5 $V_{DC}$ to 6.3 $V_{DC}$ |

## Electrical Characteristics

The following specifications apply for $V_{CC}$=5 $V_{DC}$, $T_{MIN} \le T_A \le T_{MAX}$ and $f_{CLK}$=640 kHz unless otherwise specified.

| Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| ADC0801: Total Adjusted Error (Note 8) | With Full-Scale Adj. (See Section 2.5.2) | | | ±1/4 | LSB |
| ADC0802: Total Unadjusted Error (Note 8) | $V_{REF}/2$=2.500 $V_{DC}$ | | | ±1/2 | LSB |
| ADC0803: Total Adjusted Error (Note 8) | With Full-Scale Adj. (See Section 2.5.2) | | | ±1/2 | LSB |
| ADC0804: Total Unadjusted Error (Note 8) | $V_{REF}/2$=2.500 $V_{DC}$ | | | ±1 | LSB |
| ADC0805: Total Unadjusted Error (Note 8) | $V_{REF}/2$-No Connection | | | ±1 | LSB |
| $V_{REF}/2$ Input Resistance (Pin 9) | ADC0801/02/03/05<br>ADC0804 (Note 9) | 2.5<br>0.75 | 8.0<br>1.1 | | kΩ<br>kΩ |
| Analog Input Voltage Range | (Note 4) V(+) or V(−) | Gnd−0.05 | | $V_{CC}$+0.05 | $V_{DC}$ |
| DC Common-Mode Error | Over Analog Input Voltage Range | | ±1/16 | ±1/8 | LSB |
| Power Supply Sensitivity | $V_{CC}$=5 $V_{DC}$ ±10% Over Allowed $V_{IN}(+)$ and $V_{IN}(-)$ Voltage Range (Note 4) | | ±1/16 | ±1/8 | LSB |

## AC Electrical Characteristics

The following specifications apply for $V_{CC}$=5 $V_{DC}$ and $T_A$=25°C unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $T_C$ | Conversion Time | $f_{CLK}$=640 kHz (Note 6) | 103 | | 114 | µs |
| $T_C$ | Conversion Time | (Note 5, 6) | 66 | | 73 | 1/$f_{CLK}$ |
| $f_{CLK}$ | Clock Frequency<br>Clock Duty Cycle | $V_{CC}$=5V, (Note 5)<br>(Note 5) | 100<br>40 | 640 | 1460<br>60 | kHz<br>% |
| CR | Conversion Rate in Free-Running Mode | $\overline{INTR}$ tied to $\overline{WR}$ with $\overline{CS}$=0 $V_{DC}$, $f_{CLK}$=640 kHz | 8770 | | 9708 | conv/s |
| $t_{W(\overline{WR})L}$ | Width of $\overline{WR}$ Input (Start Pulse Width) | $\overline{CS}$=0 $V_{DC}$ (Note 7) | 100 | | | ns |
| $t_{ACC}$ | Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Data Valid) | $C_L$=100 pF | | 135 | 200 | ns |
| $t_{1H}$, $t_{0H}$ | TRI-STATE Control (Delay from Rising Edge of $\overline{RD}$ to Hi-Z State) | $C_L$=10 pF, $R_L$=10k (See TRI-STATE Test Circuits) | | 125 | 200 | ns |
| $t_{WI}$, $t_{RI}$ | Delay from Falling Edge of $\overline{WR}$ or $\overline{RD}$ to Reset of $\overline{INTR}$ | | | 300 | 450 | ns |
| $C_{IN}$ | Input Capacitance of Logic Control Inputs | | | 5 | 7.5 | pF |
| $C_{OUT}$ | TRI-STATE Output Capacitance (Data Buffers) | | | 5 | 7.5 | pF |
| CONTROL INPUTS [Note: CLK IN (Pin 4) is the input of a Schmitt trigger circuit and is therefore specified separately] | | | | | | |
| $V_{IN}(1)$ | Logical "1" Input Voltage (Except Pin 4 CLK IN) | $V_{CC}$=5.25 $V_{DC}$ | 2.0 | | 15 | $V_{DC}$ |

## AC Electrical Characteristics (Continued)

The following specifications apply for $V_{CC} = 5V_{DC}$ and $T_{MIN} \le T_A \le T_{MAX}$, unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **CONTROL INPUTS** [Note: CLK IN (Pin 4) is the input of a Schmitt trigger circuit and is therefore specified separately] | | | | | | |
| $V_{IN}$ (0) | Logical "0" Input Voltage (Except Pin 4 CLK IN) | $V_{CC} = 4.75\ V_{DC}$ | | | 0.8 | $V_{DC}$ |
| $I_{IN}$ (1) | Logical "1" Input Current (All Inputs) | $V_{IN} = 5\ V_{DC}$ | | 0.005 | 1 | $\mu A_{DC}$ |
| $I_{IN}$ (0) | Logical "0" Input Current (All Inputs) | $V_{IN} = 0\ V_{DC}$ | −1 | −0.005 | | $\mu A_{DC}$ |
| **CLOCK IN AND CLOCK R** | | | | | | |
| $V_T+$ | CLK IN (Pin 4) Positive Going Threshold Voltage | | 2.7 | 3.1 | 3.5 | $V_{DC}$ |
| $V_T-$ | CLK IN (Pin 4) Negative Going Threshold Voltage | | 1.5 | 1.8 | 2.1 | $V_{DC}$ |
| $V_H$ | CLK IN (Pin 4) Hysteresis $(V_T+)-(V_T-)$ | | 0.6 | 1.3 | 2.0 | $V_{DC}$ |
| $V_{OUT}$ (0) | Logical "0" CLK R Output Voltage | $I_O = 360\ \mu A$<br>$V_{CC} = 4.75\ V_{DC}$ | | | 0.4 | $V_{DC}$ |
| $V_{OUT}$ (1) | Logical "1" CLK R Output Voltage | $I_O = -360\ \mu A$<br>$V_{CC} = 4.75\ V_{DC}$ | 2.4 | | | $V_{DC}$ |
| **DATA OUTPUTS AND $\overline{INTR}$** | | | | | | |
| $V_{OUT}$ (0) | Logical "0" Output Voltage<br>Data Outputs<br>$\overline{INTR}$ Output | <br>$I_{OUT} = 1.6$ mA, $V_{CC} = 4.75\ V_{DC}$<br>$I_{OUT} = 1.0$ mA, $V_{CC} = 4.75\ V_{DC}$ | | | <br>0.4<br>0.4 | <br>$V_{DC}$<br>$V_{DC}$ |
| $V_{OUT}$ (1) | Logical "1" Output Voltage | $I_O = -360\ \mu A$, $V_{CC} = 4.75\ V_{DC}$ | 2.4 | | | $V_{DC}$ |
| $V_{OUT}$ (1) | Logical "1" Output Voltage | $I_O = -10\ \mu A$, $V_{CC} = 4.75\ V_{DC}$ | 4.5 | | | $V_{DC}$ |
| $I_{OUT}$ | TRI-STATE Disabled Output Leakage (All Data Buffers) | $V_{OUT} = 0\ V_{DC}$<br>$V_{OUT} = 5\ V_{DC}$ | −3 | | <br>3 | $\mu A_{DC}$<br>$\mu A_{DC}$ |
| $I_{SOURCE}$ | | $V_{OUT}$ Short to Gnd, $T_A = 25°C$ | 4.5 | 6 | | $mA_{DC}$ |
| $I_{SINK}$ | | $V_{OUT}$ Short to $V_{CC}$, $T_A = 25°C$ | 9.0 | 16 | | $mA_{DC}$ |
| **POWER SUPPLY** | | | | | | |
| $I_{CC}$ | Supply Current (Includes Ladder Current)<br>ADC0801/02/03/04LCJ/05<br>ADC0804LCN/LCV/LCWM | $f_{CLK} = 640$ kHz, $V_{REF}/2 = NC$, $T_A = 25°C$ and $\overline{CS} = 5V$ | | <br>1.1<br>1.9 | <br>1.8<br>2.5 | <br>mA<br>mA |

**Note 1:** Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

**Note 2:** All voltages are measured with respect to Gnd, unless otherwise specified. The separate A Gnd point should always be wired to the D Gnd.

**Note 3:** A zener diode exists, internally, from $V_{CC}$ to Gnd and has a typical breakdown voltage of 7 $V_{DC}$.

**Note 4:** For $V_{IN}(-) \ge V_{IN}(+)$ the digital output code will be 0000 0000. Two on-chip diodes are tied to each analog input (see block diagram) which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the $V_{CC}$ supply. Be careful, during testing at low $V_{CC}$ levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct—especially at elevated temperatures, and cause errors for analog inputs near full-scale. The spec allows 50 mV forward bias of either diode. This means that as long as the analog $V_{IN}$ does not exceed the supply voltage by more than 50 mV, the output code will be correct. To achieve an absolute 0 $V_{DC}$ to 5 $V_{DC}$ input voltage range will therefore require a minimum supply voltage of 4.950 $V_{DC}$ over temperature variations, initial tolerance and loading.

**Note 5:** Accuracy is guaranteed at $f_{CLK} = 640$ kHz. At higher clock frequencies accuracy can degrade. For lower clock frequencies, the duty cycle limits can be extended so long as the minimum clock high time interval or minimum clock low time interval is no less than 275 ns.

**Note 6:** With an asynchronous start pulse, up to 8 clock periods may be required before the internal clock phases are proper to start the conversion process. The start request is internally latched, see *Figure 2* and section 2.0.

**Note 7:** The $\overline{CS}$ input is assumed to bracket the $\overline{WR}$ strobe input and therefore timing is dependent on the $\overline{WR}$ pulse width. An arbitrarily wide pulse width will hold the converter in a reset mode and the start of conversion is initiated by the low to high transition of the $\overline{WR}$ pulse (see timing diagrams).

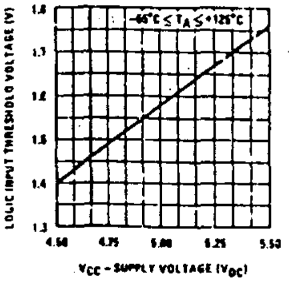
**Note 8:** None of these A/Ds requires a zero adjust (see section 2.5.1). To obtain zero code at other analog input voltages see section 2.5 and *Figure 5*.

**Note 9:** The $V_{REF}/2$ pin is the center point of a two resistor divider connected from $V_{CC}$ to ground. Each resistor is 2.2k, except for the ADC0804LCJ where each resistor is 16k. Total ladder input resistance is the sum of the two equal resistors.

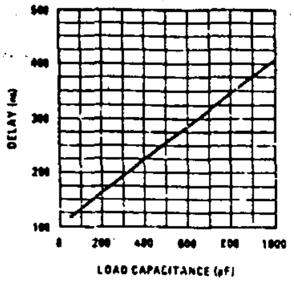
**Note 10:** Human body model, 100 pF discharged through a 1.5 kΩ resistor.

## Typical Performance Characteristics

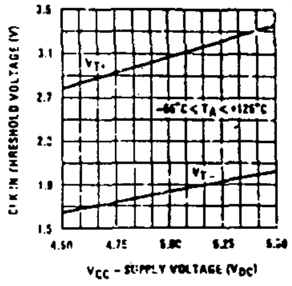
**Logic Input Threshold Voltage vs. Supply Voltage**



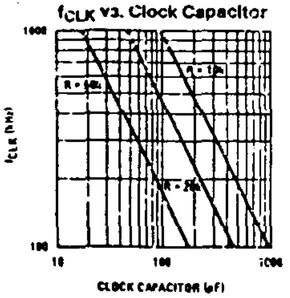

**Delay From Falling Edge of $\overline{RD}$ to Output Data Valid vs. Load Capacitance**



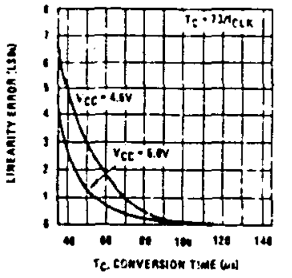

**CLK IN Schmitt Trip Levels vs. Supply Voltage**



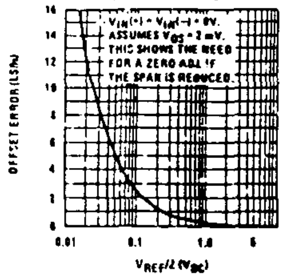

**$f_{CLK}$ vs. Clock Capacitor**



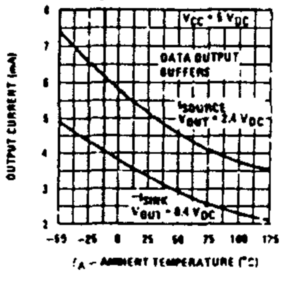

**Full-Scale Error vs Conversion Time**



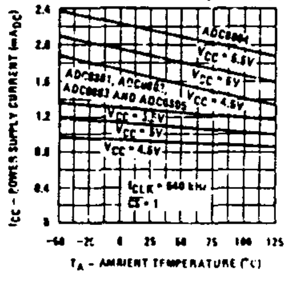

**Effect of Unadjusted Offset Error vs. $V_{REF}/2$ Voltage**



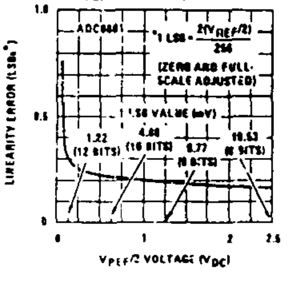

**Output Current vs Temperature**




**Power Supply Current vs Temperature (Note 9)**

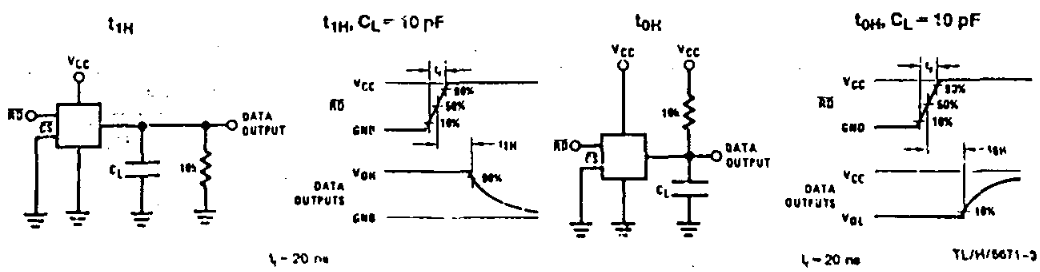



**Linearity Error at Low $V_{REF}/2$ Voltages**



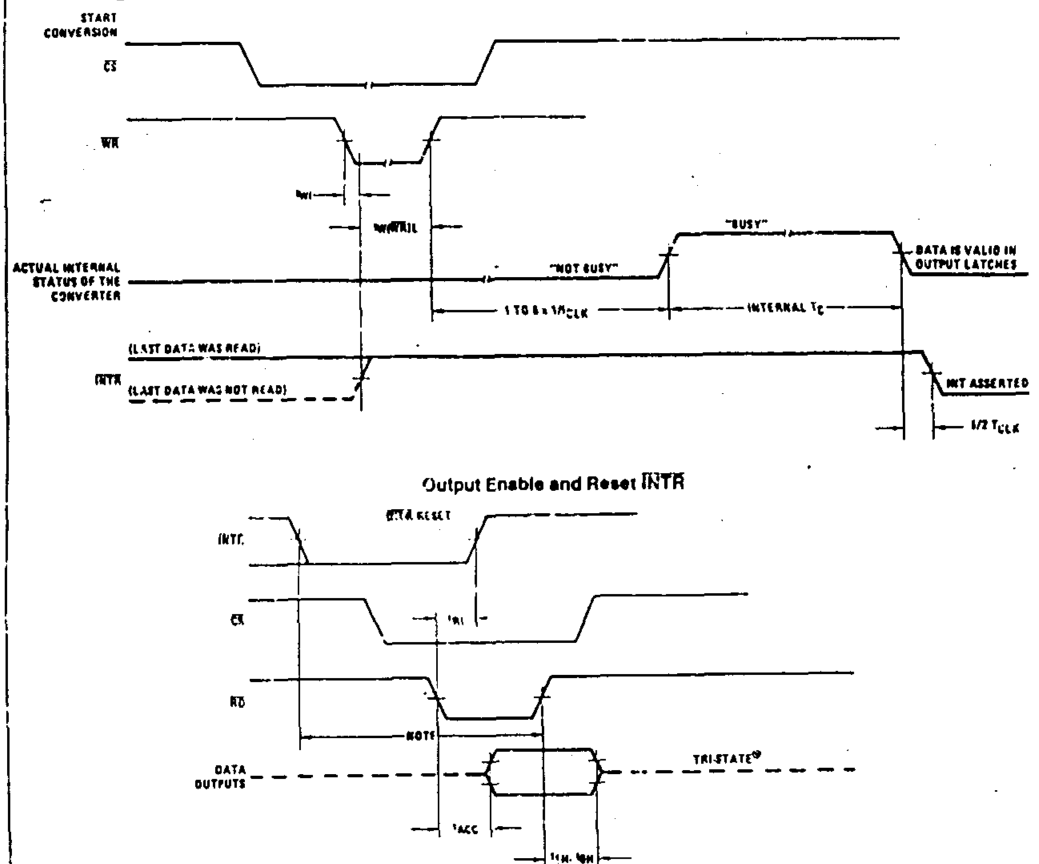

TL/H/5671–2

## TRI-STATE Test Circuits and Waveforms




TL/H/5671-3

## Timing Diagrams (All timing is measured from the 50% voltage points)

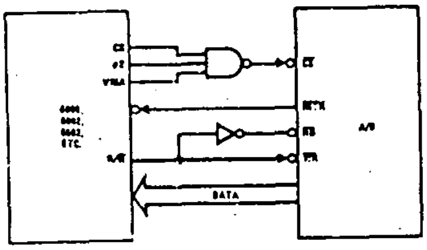



TL/H/5671-4

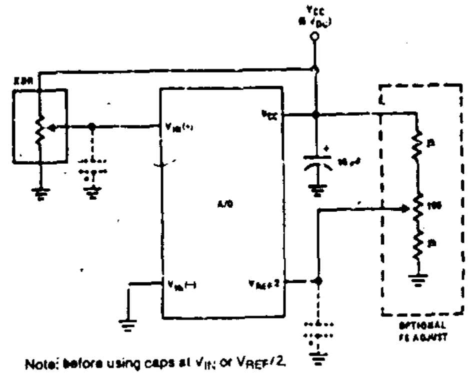
Note: Read strobe must occur 8 clock periods ($8/f_{CLK}$) after assertion of interrupt to guarantee reset of $\overline{INTR}$.

## Typical Applications (Continued)

**6800 Interface**

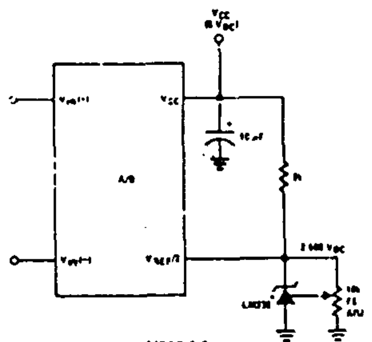



**Ratiometric with Full-Scale Adjust**



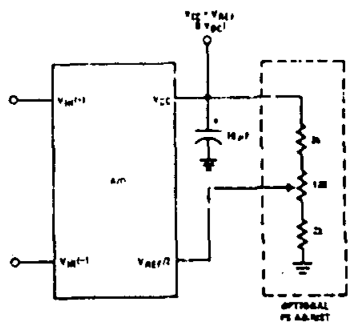

Note: before using caps at $V_{IN}$ or $V_{REF}/2$, see section 2.3.2 Input Bypass Capacitors.

**Absolute with a 2.500V Reference**

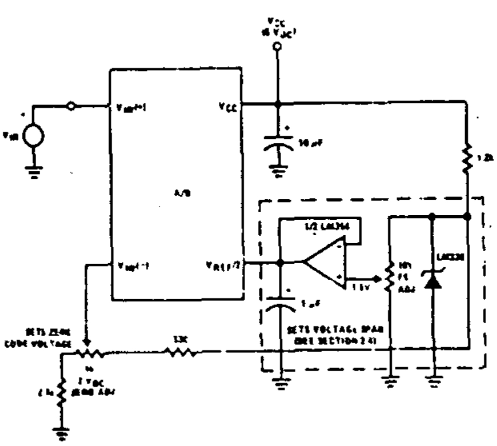



*For low power, see also LM385-2.5

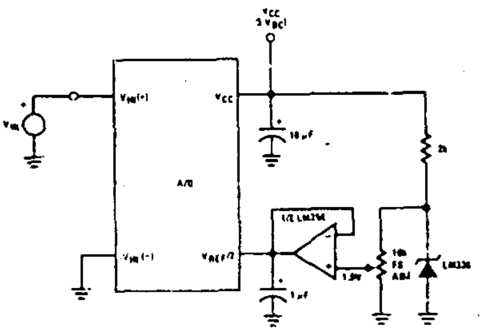
**Absolute with a 5V Reference**




**Zero-Shift and Span Adjust: $2V \leq V_{IN} \leq 5V$**

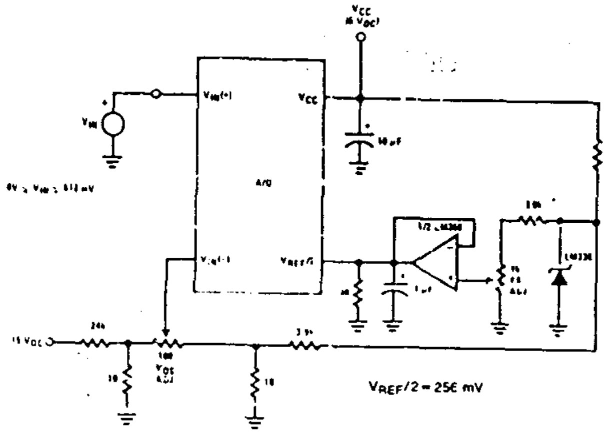



**Span Adjust: $0V \leq V_{IN} \leq 3V$**

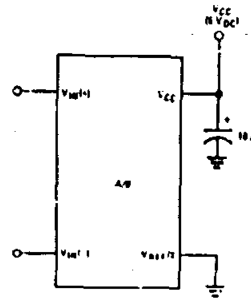



TL/H/5671-5

### Directly Converting a Low-Level Signal



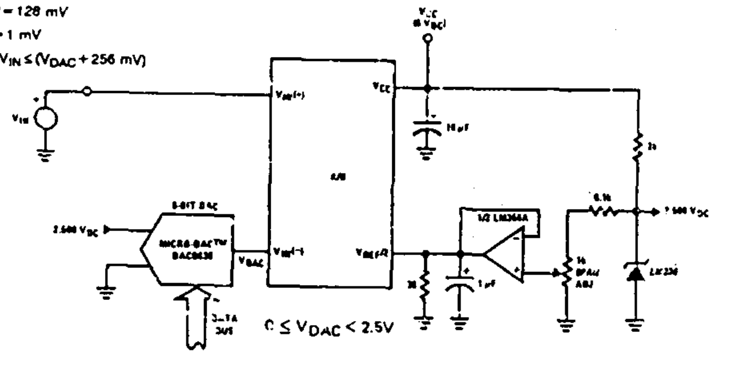

### A µP Interfaced Comparator



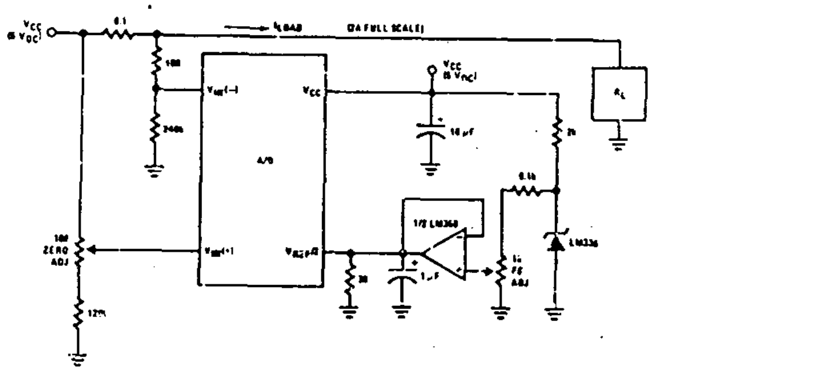

For $V_{IN}(+) > V_{IN}(-)$
Output = $FF_{HEX}$
For $V_{IN}(+) < V_{IN}(-)$
Output = $00_{HEX}$

### 1 mV Resolution with µP Controlled Range

$V_{REF}/2 = 128$ mV
1 LSB = 1 mV
$V_{DAC} \leq V_{IN} \leq (V_{DAC} + 256 \text{ mV})$

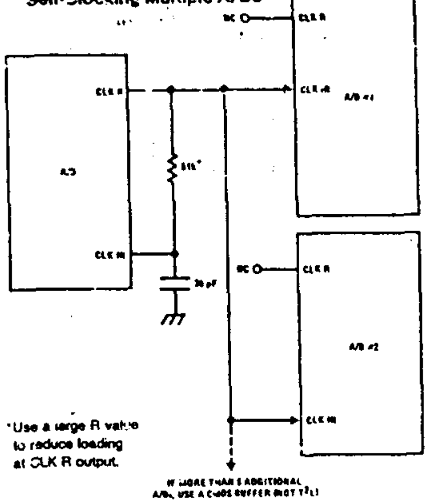



### Digitizing a Current Flow



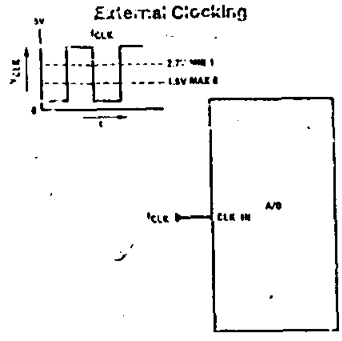

TL/H/5671-4

### Self-Clocking Multiple A/Ds



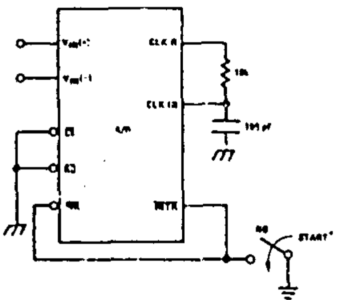

*Use a large R value to reduce loading at CLK R output.

### External Clocking



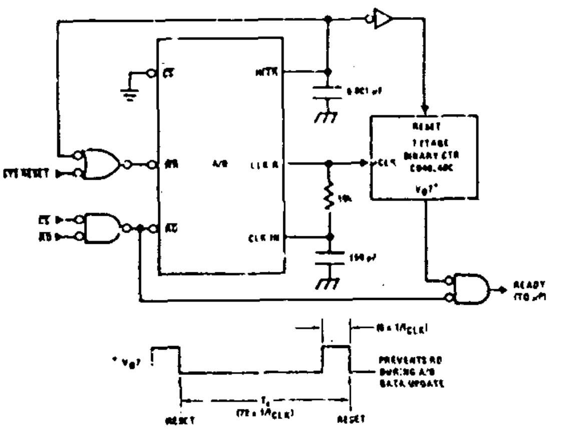

100 kHz ≤ $f_{CLK}$ ≤ 1460 kHz

### Self-Clocking in Free-Running Mode

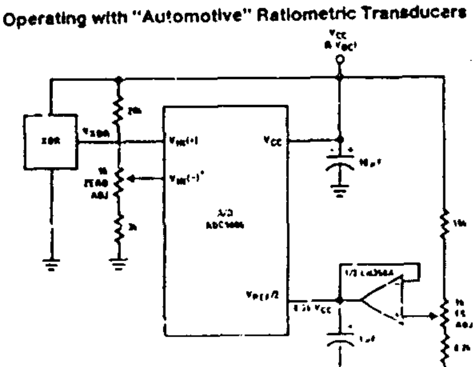



*After power-up, a momentary grounding of the $\overline{WR}$ input is needed to guarantee operation.

### µP Interface for Free-Running A/D

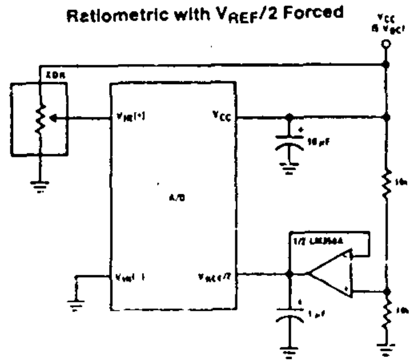



### Operating with "Automotive" Ratiometric Transducers




$*V_{IN}(-) = 0.15\ V_{CC}$
15% of $V_{CC} \le V_{XDR} \le 85\%$ of $V_{CC}$

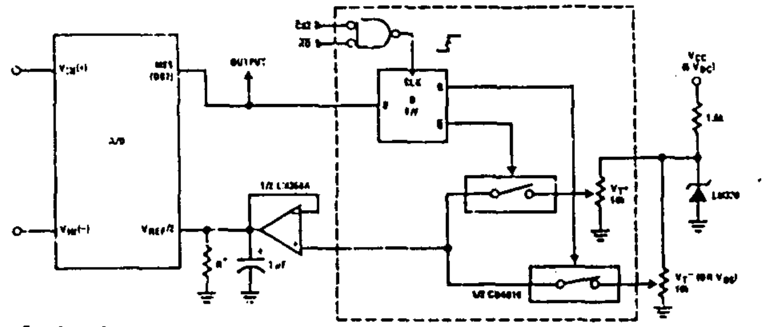
### Ratiometric with $V_{REF}/2$ Forced




TL/H/5671-7

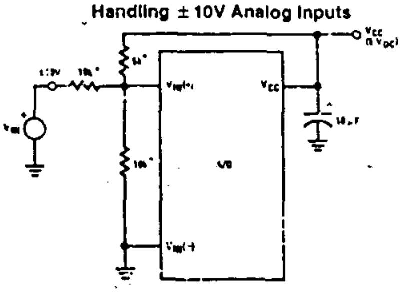
## Typical Applications (Continued)

### μP Compatible Differential-Input Comparator with Pre-Set $V_{OS}$ (with or without Hysteresis)



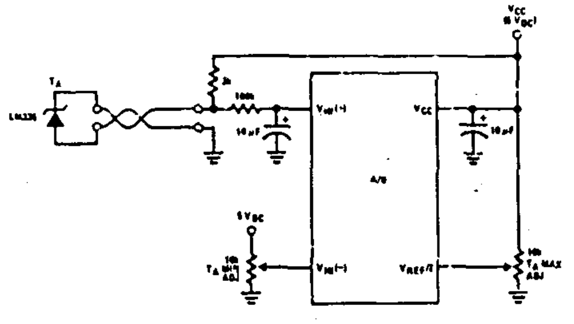
*See *Figure 5* to select R value
DB7 = "1" for $V_{IN}(+) > V_{IN}(-) + (V_{REF}/2)$
Omit circuitry within the dotted area if hysteresis is not needed

### Handling ± 10V Analog Inputs

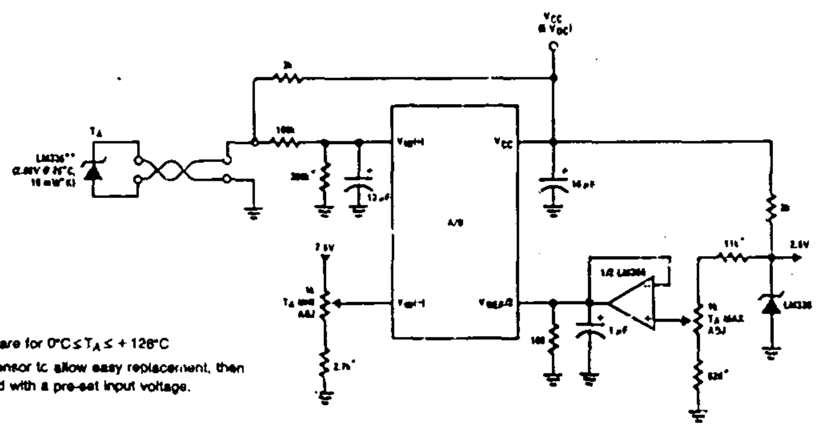


*Beckman Instruments #694-3-R10K resistor array

### Low-Cost, μP Interfaced, Temperature-to-Digital Converter



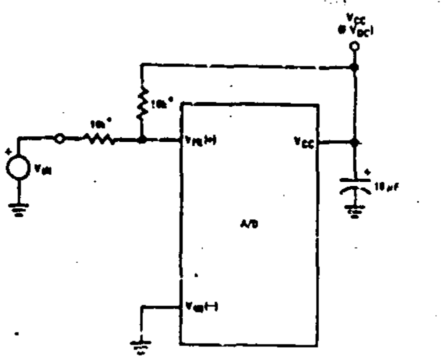
### μP Interfaced Temperature-to-Digital Converter



*Circuit values shown are for $0°C \le T_A \le +128°C$
**Can calibrate each sensor to allow easy replacement, then A/D can be calibrated with a pre-set input voltage.

TL/H/5671–8

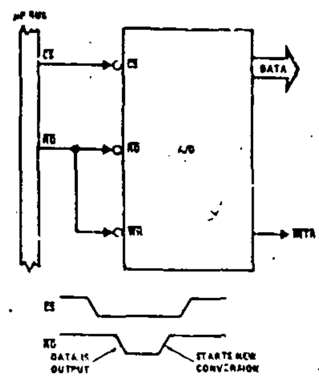
### Handling ±5V Analog Inputs



TL/H/5671-33

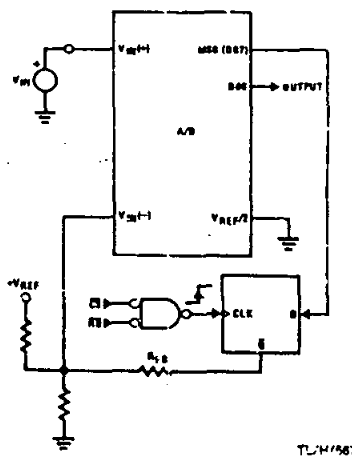
*Beckman Instruments # 694-3-R10K resistor array

### Read-Only Interface



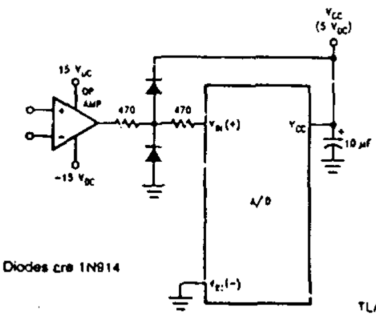
TL/H/5671-34

### µP Interfaced Comparator with Hysteresis



TL/H/5671-35

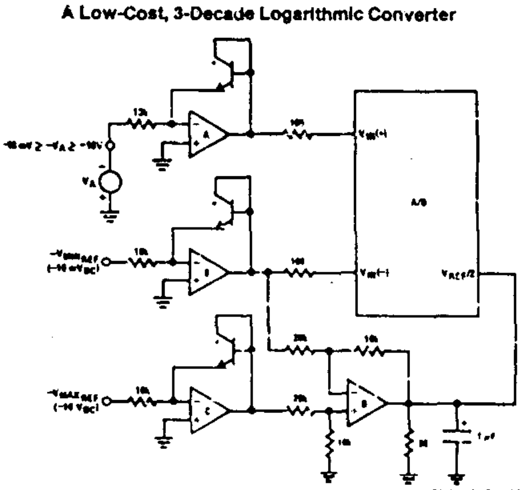
### Protecting the Input



Diodes are 1N914

TL/H/5671-9

### A Low-Cost, 3-Decade Logarithmic Converter

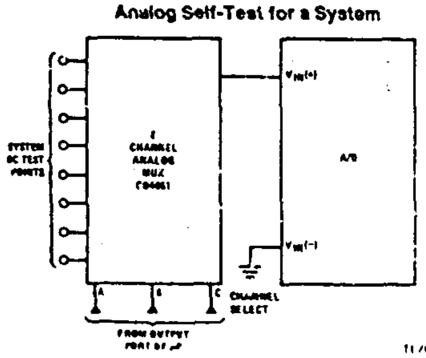


TL/H/5671-37

*LM389 transistors

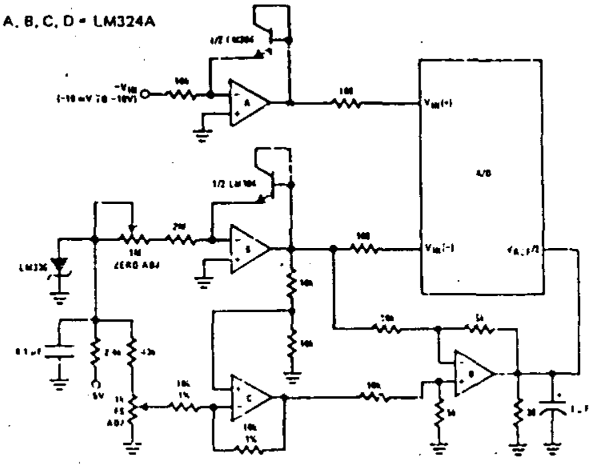
A, B, C, D = LM324A quad op amp

### Analog Self-Test for a System

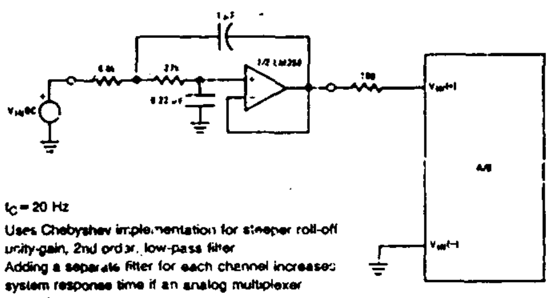


TL/H/5671-36

### 3-Decade Logarithmic A/D Converter

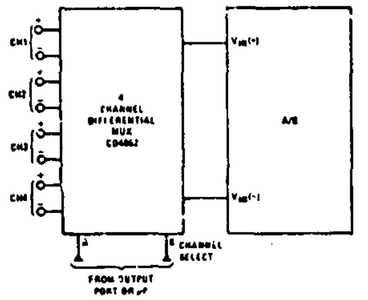



### Noise Filtering the Analog Input

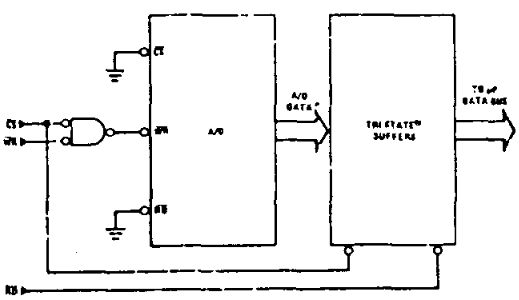



$f_C$ = 20 Hz
Uses Chebyshev implementation for steeper roll-off unity-gain, 2nd order, low-pass filter
Adding a separate filter for each channel increases system response time if an analog multiplexer is used

### Multiplexing Differential Inputs

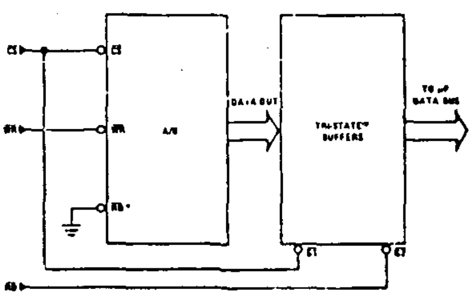



### Output Buffers with A/D Data Enabled




*A/D output data is updated 1 CLK period prior to assertion of $\overline{INTR}$

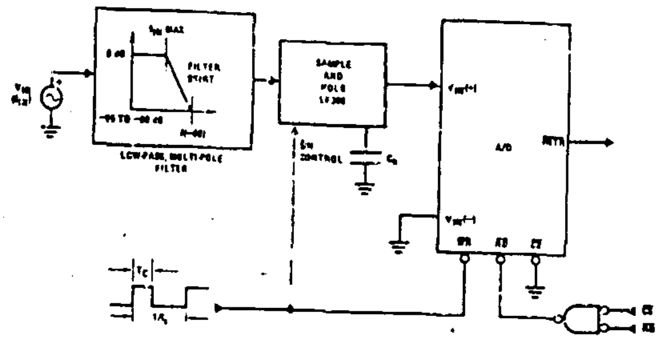
### Increasing Bus Drive and/or Reducing Time on Bus




TL/H/5671-10

*Allows output data to set-up at falling edge of $\overline{CS}$

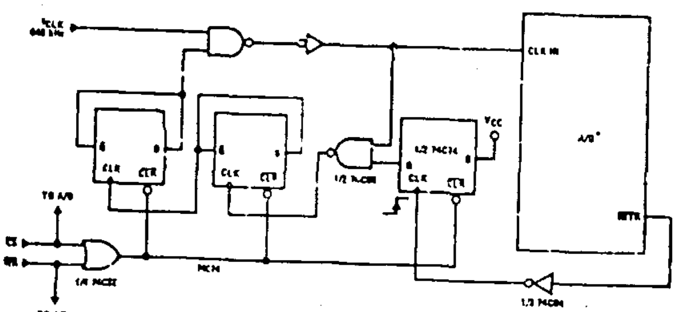
## Sampling an AC Input Signal



**Note 1:** Oversample whenever possible [i.e., fs > 2f(−60)] to eliminate input frequency folding (aliasing) and to allow for the skirt response of the filter.

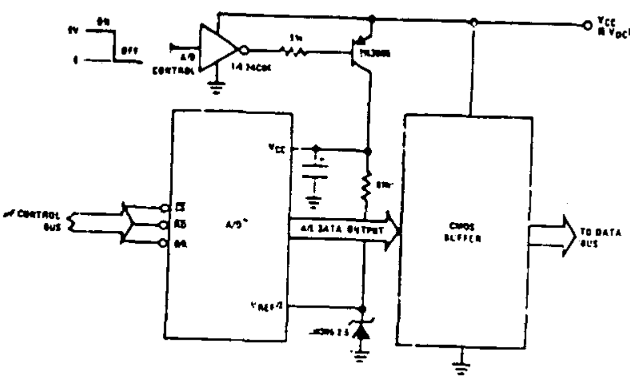
**Note 2:** Consider the amplitude errors which are introduced within the passband of the filter.

## 70% Power Savings by Clock Gating



(Complete shutdown takes ≈ 30 seconds.)

## Power Savings by A/D and $V_{REF}$ Shutdown



TL/H/5671-11

*Use ADC0801, 02, 03 or 05 for lowest power consumption.

Note: Logic inputs can be driven to $V_{CC}$ with A/D supply at zero volts.

Buffer prevents data bus from overdriving output of A/D when in shutdown mode.

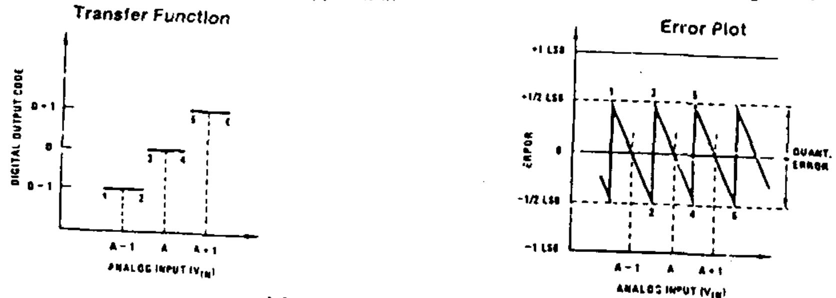
## 1.0 UNDERSTANDING A/D ERROR SPECS

A perfect A/D transfer characteristic (staircase waveform) is shown in *Figure 1a*. The horizontal scale is analog input voltage and the particular points labeled are in steps of 1 LSB (19.53 mV with 2.5V tied to the $V_{REF}/2$ pin). The digital output codes that correspond to these inputs are shown as D−1, D, and D+1. For the perfect A/D, not only will center-value (A−1, A, A+1, . . . .) analog inputs produce the correct output digital codes, but also each riser (the transitions between adjacent output codes) will be located ±½ LSB away from each center-value. As shown, the risers are ideal and have no width. Correct digital output codes will be provided for a range of analog input voltages that extend ±½ LSB from the ideal center-values. Each tread (the range of analog input voltage that provides the same digital output code) is therefore 1 LSB wide.

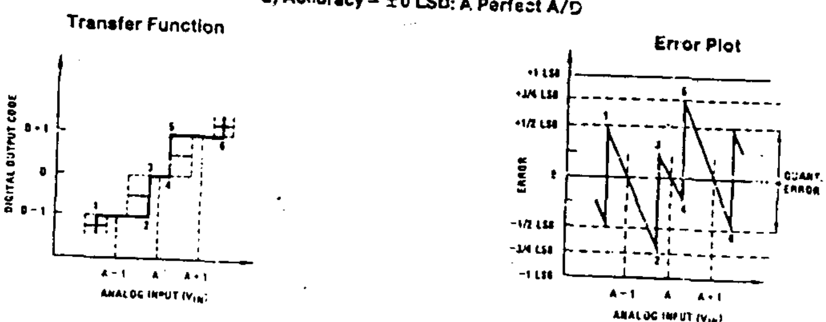
*Figure 1b* shows a worst case error plot for the ADC0801. All center-valued inputs are guaranteed to produce the correct output codes and the adjacent risers are guaranteed to be no closer to the center value points than ±¼ LSB. In other words, if we apply an analog input equal to the center-value ±¼ LSB, *we guarantee* that the A/D will produce the correct digital code. The maximum range of the position of the code transition is indicated by the horizontal arrow and it is guaranteed to be no more than ½ LSB.

The error curve of *Figure 1c* shows a worst case error plot for the ADC0802. Here we guarantee that if we apply an analog input equal to the LSB analog voltage center-value the A/D will produce the correct digital code.

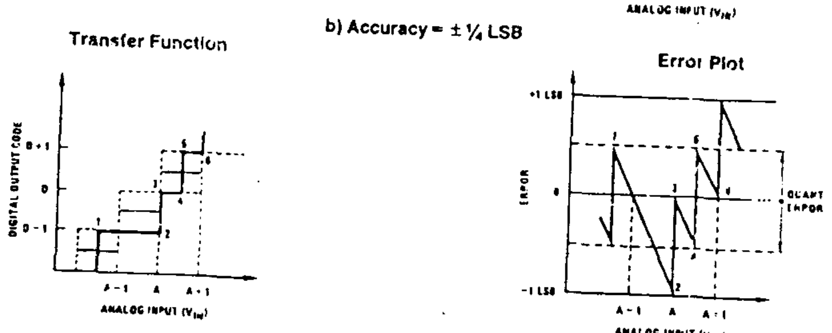
Next to each transfer function is shown the corresponding error plot. Many people may be more familiar with error plots then transfer functions. The analog input voltage to the A/D is provided by either a linear ramp or by the discrete output steps of a high resolution DAC. Notice that the error is continuously displayed and includes the quantization uncertainty of the A/D. For example the error at point 1 of *Figure 1a* is +½ LSB because the digital code appeared ½ LSB in advance of the center-value of the tread. The error plots always have a constant negative slope and the abrupt upside steps are always 1 LSB in magnitude.




a) Accuracy = ±0 LSB: A Perfect A/D




b) Accuracy = ±¼ LSB




c) Accuracy = ±½ LSB

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**FIGURE 1. Clarifying the Error Specs of an A/D Converter**

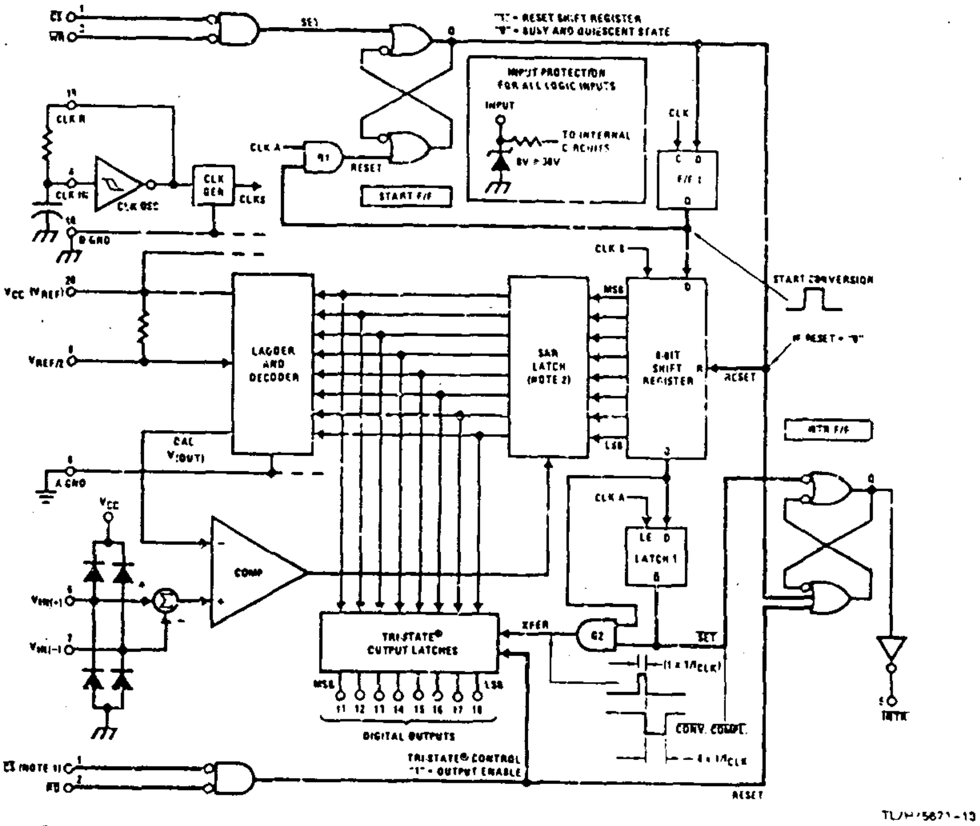
### 2.0 FUNCTIONAL DESCRIPTION

The ADC0801 series contains a circuit equivalent of the 256R network. Analog switches are sequenced by successive approximation logic to match the analog difference input voltage [$V_{IN}(+) - V_{IN}(-)$] to a corresponding tap on the R network. The most significant bit is tested first and after 8 comparisons (64 clock cycles) a digital 8-bit binary code (1111 1111 = full-scale) is transferred to an output latch and then an interrupt is asserted ($\overline{INTR}$ makes a high-to-low transition). A conversion in process can be interrupted by issuing a second start command. The device may be operated in the free-running mode by connecting $\overline{INTR}$ to the $\overline{WR}$ input with $\overline{CS}=0$. To ensure start-up under all possible conditions, an external $\overline{WR}$ pulse is required during the first power-up cycle.

On the high-to-low transition of the $\overline{WR}$ input the internal SAR latches and the shift register stages are reset. As long as the $\overline{CS}$ input and $\overline{WR}$ input remain low, the A/D will remain in a reset state. *Conversion will start from 1 to 8 clock periods after at least one of these inputs makes a low-to-high transition.*

A functional diagram of the A/D converter is shown in *Figure 2*. All of the package pinouts are shown and the major logic control paths are drawn in heavier weight lines.

The converter is started by having $\overline{CS}$ and $\overline{WR}$ simultaneously low. This sets the start flip-flop (F/F) and the resulting "1" level resets the 8-bit shift register, resets the Interrupt (INTR) F/F and inputs a "1" to the D flop, F/F1, which is at the input end of the 8-bit shift register. Internal clock signals then transfer this "1" to the Q output of F/F1. The AND gate, G1, combines this "1" output with a clock signal to provide a reset signal to the start F/F. If the set signal is no longer present (either $\overline{WR}$ or $\overline{CS}$ is a "1") the start F/F is reset and the 8-bit shift register then can have the "1" clocked in, which starts the conversion process. If the set signal were to still be present, this reset pulse would have no effect (both outputs of the start F/F would momentarily be at a "1" level) and the 8-bit shift register would continue to be held in the reset mode. This logic therefore allows for wide $\overline{CS}$ and $\overline{WR}$ signals and the converter will start after at least one of these signals returns high and the internal clocks again provide a reset signal for the start F/F.




Note 1: $\overline{CS}$ shown twice for clarity.

Note 2: SAR = Successive Approximation Register.

FIGURE 2. Block Diagram

After the "1" is clocked through the 8-bit shift register (which completes the SAR search) it appears as the input to the D-type latch, LATCH 1. As soon as this "1" is output from the shift register, the AND gate, G2, causes the new digital word to transfer to the TRI-STATE output latches. When LATCH 1 is subsequently enabled, the Q output makes a high-to-low transition which causes the INTR F/F to set. An inverting buffer then supplies the $\overline{INTR}$ input signal.

Note that this $\overline{SET}$ control of the INTR F/F remains low for 8 of the external clock periods (as the internal clocks run at ⅛ of the frequency of the external clock). If the data output is continuously enabled ($\overline{CS}$ and $\overline{RD}$ both held low), the $\overline{INTR}$ output will still signal the end of conversion (by a high-to-low transition), because the $\overline{SET}$ input can control the Q output of the INTR F/F even though the RESET input is constantly at a "1" level in this operating mode. This $\overline{INTR}$ output will therefore stay low for the duration of the $\overline{SET}$ signal, which is 8 periods of the external clock frequency (assuming the A/D is not started during this interval).

When operating in the free-running or continuous conversion mode ($\overline{INTR}$ pin tied to $\overline{WR}$ and $\overline{CS}$ wired low—see also section 2.8), the START F/F is SET by the high-to-low transition of the $\overline{INTR}$ signal. This resets the SHIFT REGISTER which causes the input to the D-type latch, LATCH 1, to go low. As the latch enable input is still present, the $\overline{Q}$ output will go high, which then allows the INTR F/F to be RESET. This reduces the width of the resulting $\overline{INTR}$ output pulse to only a few propagation delays (approximately 300 ns).

When data is to be read, the combination of both $\overline{CS}$ and $\overline{RD}$ being low will cause the INTR F/F to be reset and the TRI-STATE output latches will be enabled to provide the 8-bit digital outputs.

### 2.1 Digital Control Inputs

The digital control inputs ($\overline{CS}$, $\overline{RD}$, and $\overline{WR}$) meet standard $T^2L$ logic voltage levels. These signals have been renamed when compared to the standard A/D Start and Output Enable labels. In addition, these inputs are active low to allow an easy interface to microprocessor control busses. For non-microprocessor based applications, the $\overline{CS}$ input (pin 1) can be grounded and the standard A/D Start function is obtained by an active low pulse applied at the $\overline{WR}$ input (pin 3) and the Output Enable function is caused by an active low pulse at the $\overline{RD}$ input (pin 2).

### 2.2 Analog Differential Voltage Inputs and Common-Mode Rejection

This A/D has additional applications flexibility due to the analog differential voltage input. The $V_{IN}(-)$ input (pin 7) can be used to automatically subtract a fixed voltage value from the input reading (tare correction). This is also useful in 4 mA–20 mA current loop conversion. In addition, common-mode noise can be reduced by use of the differential input.

The time interval between sampling $V_{IN}(+)$ and $V_{IN}(-)$ is 4-½ clock periods. The maximum error voltage due to this slight time difference between the input voltage samples is given by:

$$\Delta V_e(MAX) = (V_P)(2\pi f_{cm})\left(\frac{4.5}{f_{CLK}}\right),$$

where:

$\Delta V_e$ is the error voltage due to sampling delay

$V_P$ is the peak value of the common-mode voltage

$f_{cm}$ is the common-mode frequency

As an example, to keep this error to ¼ LSB (~5 mV) when operating with a 60 Hz common-mode frequency, $f_{cm}$, and using a 640 kHz A/D clock, $f_{CLK}$, would allow a peak value of the common-mode voltage, $V_P$, which is given by:

$$V_P = \frac{[\Delta V_{e(MAX)}(f_{CLK})]}{(2\pi f_{cm})(4.5)}$$

or

$$V_P = \frac{(5 \times 10^{-3})(640 \times 10^3)}{(6.28)(60)(4.5)}$$

which gives

$V_P \cong 1.9V.$

The allowed range of analog input voltages usually places more severe restrictions on input common-mode noise levels.

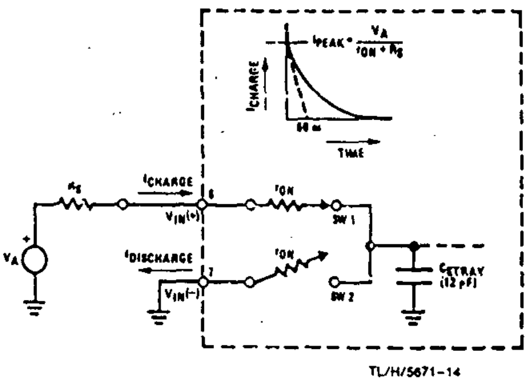
An analog input voltage with a reduced span and a relatively large zero offset can be handled easily by making use of the differential input (see section 2.4 Reference Voltage).

### 2.3 Analog Inputs

#### 2.3.1 Input Current

**Normal Mode**

Due to the internal switching action, displacement currents will flow at the analog inputs. This is due to on-chip stray capacitance to ground as shown in *Figure 3*.




$r_{ON}$ of SW 1 and SW 2 ≅ 5 kΩ

$r = r_{ON}\,C_{STRAY}$ ≅ 5 kΩ × 12 pF = 60 ns

**FIGURE 3. Analog Input Impedance**

The voltage on this capacitance is switched and will result in currents entering the $V_{IN}(+)$ input pin and leaving the $V_{IN}(-)$ input which will depend on the analog differential input voltage levels. These current transients occur at the leading edge of the internal clocks. They rapidly decay and *do not cause errors* as the on-chip comparator is strobed at the end of the clock period.

**Fault Mode**

If the voltage source applied to the $V_{IN}(+)$ or $V_{IN}(-)$ pin exceeds the allowed operating range of $V_{CC}+50$ mV, large input currents can flow through a parasitic diode to the $V_{CC}$ pin. If these currents can exceed the 1 mA max allowed spec, an external diode (1N914) should be added to bypass this current to the $V_{CC}$ pin (with the current bypassed with this diode, the voltage at the $V_{IN}(+)$ pin can exceed the $V_{CC}$ voltage by the forward voltage of this diode).

**2.3.2 Input Bypass Capacitors**

Bypass capacitors at the inputs will average these charges and cause a DC current to flow through the output resistances of the analog signal sources. This charge pumping action is worse for continuous conversions with the $V_{IN}(+)$ input voltage at full-scale. For continuous conversions with a 640 kHz clock frequency with the $V_{IN}(+)$ input at 5V, this DC current is at a maximum of approximately 5 μA. Therefore, *bypass capacitors should not be used at the analog inputs or the $V_{REF}/2$ pin* for high resistance sources (> 1 kΩ). If input bypass capacitors are necessary for noise filtering and high source resistance is desirable to minimize capacitor size, the detrimental effects of the voltage drop across this input resistance, which is due to the average value of the input current, can be eliminated with a full-scale adjustment while the given source resistor and input bypass capacitor are both in place. This is possible because the average value of the input current is a precise linear function of the differential input voltage.

**2.3.3 Input Source Resistance**

Large values of source resistance where an input bypass capacitor is not used, *will not cause errors* as the input currents settle out prior to the comparison time. If a low pass filter is required in the system, use a low valued series resistor (≤ 1 kΩ) for a passive RC section or add an op amp RC active low pass filter. For low source resistance applications, (≤ 1 kΩ), a 0.1 μF bypass capacitor at the inputs will prevent noise pickup due to series lead inductance of a long wire. A 100Ω series resistor can be used to isolate this capacitor—both the R and C are placed outside the feedback loop—from the output of an op amp, if used.

**2.3.4 Noise**

The leads to the analog inputs (pin 6 and 7) should be kept as short as possible to minimize input noise coupling. Both noise and undesired digital clock coupling to these inputs can cause system errors. The source resistance for these inputs should, in general, be kept below 5 kΩ. Larger values of source resistance can cause undesired system noise pickup. Input bypass capacitors, placed from the analog inputs to ground, will eliminate system noise pickup but can create analog scale errors as these capacitors will average the transient input switching currents of the A/D (see section 2.3.1.). This scale error depends on both a large source resistance and the use of an input bypass capacitor. This error can be eliminated by doing a full-scale adjustment of the A/D (adjust $V_{REF}/2$ for a proper full-scale reading—see section 2.5.2 on Full-Scale Adjustment) with the source resistance and input bypass capacitor in place.

**2.4 Reference Voltage**

**2.4.1 Span Adjust**

For maximum applications flexibility, these A/Ds have been designed to accommodate a 5 $V_{DC}$, 2.5 $V_{DC}$ or an adjusted voltage reference. This has been achieved in the design of the IC as shown in *Figure 4*.

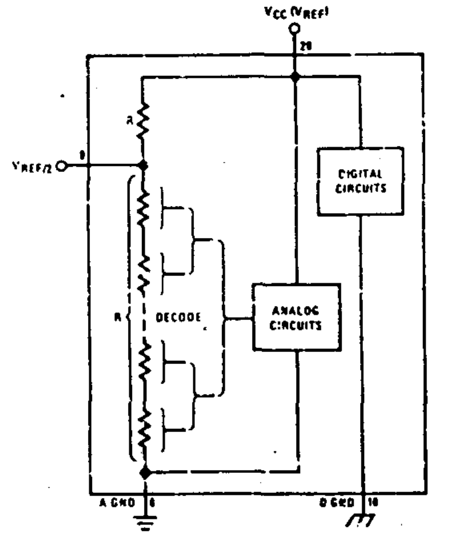



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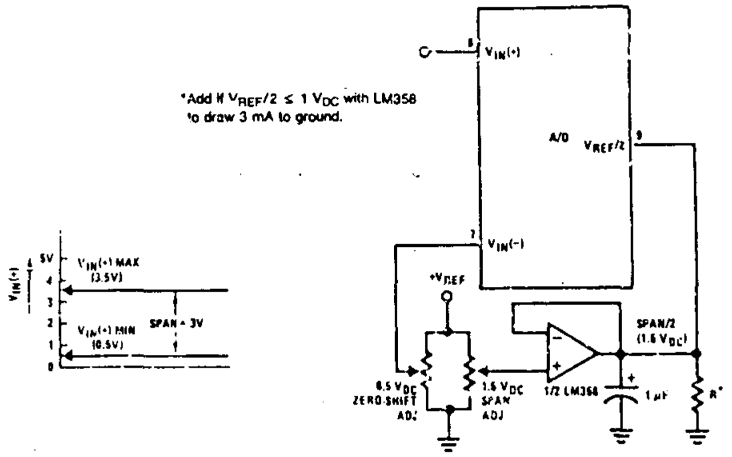
**FIGURE 4. The $V_{REFERENCE}$ Design on the IC**

Notice that the reference voltage for the IC is either ½ of the voltage applied to the $V_{CC}$ supply pin, or is equal to the voltage that is externally forced at the $V_{REF}/2$ pin. This allows for a ratiometric voltage reference using the $V_{CC}$ supply, a 5 $V_{DC}$ reference voltage can be used for the $V_{CC}$ supply or a voltage less than 2.5 $V_{DC}$ can be applied to the $V_{REF}/2$ input for increased application flexibility. The internal gain to the $V_{REF}/2$ input is 2, making the full-scale differential input voltage twice the voltage at pin 9.

An example of the use of an adjusted reference voltage is to accommodate a reduced span—or dynamic voltage range of the analog input voltage. If the analog input voltage were to range from 0.5 $V_{DC}$ to 3.5 $V_{DC}$, instead of 0V to 5 $V_{DC}$, the span would be 3V as shown in *Figure 5*. With 0.5 $V_{DC}$ applied to the $V_{IN}(-)$ pin to absorb the offset, the reference voltage can be made equal to ½ of the 3V span or 1.5 $V_{DC}$. The A/D now will encode the $V_{IN}(+)$ signal from 0.5V to 3.5 V with the 0.5V input corresponding to zero and the 3.5 $V_{DC}$ input corresponding to full-scale. The full 8 bits of resolution are therefore applied over this reduced analog input voltage range.

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a) Analog Input Signal Example

b) Accommodating an Analog Input from 0.5V (Digital Out = = $00_{HEX}$) to 3.5V (Digital Out = $FF_{HEX}$)

**FIGURE 5. Adapting the A/D Analog Input Voltages to Match an Arbitrary Input Signal Range**

### 2.4.2 Reference Accuracy Requirements

The converter can be operated in a ratiometric mode or an absolute mode. In ratiometric converter applications, the magnitude of the reference voltage is a factor in both the output of the source transducer and the output of the A/D converter and therefore cancels out in the final digital output code. The ADC0805 is specified particularly for use in ratiometric applications with no adjustments required. In absolute conversion applications, both the initial value and the temperature stability of the reference voltage are important factors in the accuracy of the A/D converter. For $V_{REF}/2$ voltages of 2.4 $V_{DC}$ nominal value, initial errors of $\pm 10$ $mV_{DC}$ will cause conversion errors of $\pm 1$ LSB due to the gain of 2 of the $V_{REF}/2$ input. In reduced span applications, the initial value and the stability of the $V_{REF}/2$ input voltage become even more important. For example, if the span is reduced to 2.5V, the analog input LSB voltage value is correspondingly reduced from 20 mV (5V span) to 10 mV and 1 LSB at the $V_{REF}/2$ input becomes 5 mV. As can be seen, this reduces the allowed initial tolerance of the reference voltage and requires correspondingly less absolute change with temperature variations. Note that spans smaller than 2.5V place even tighter requirements on the initial accuracy and stability of the reference source.

In general, the magnitude of the reference voltage will require an initial adjustment. Errors due to an improper value of reference voltage appear as full-scale errors in the A/D transfer function. IC voltage regulators may be used for references if the ambient temperature changes are not excessive. The LM336B 2.5V IC reference diode (from National Semiconductor) has a temperature stability of 1.8 mV typ (6 mV max) over $0°C \leq T_A \leq +70°C$. Other temperature range parts are also available.

### 2.5 Errors and Reference Voltage Adjustments

### 2.5.1 Zero Error

The zero of the A/D does not require adjustment. If the minimum analog input voltage value, $V_{IN(MIN)}$, is not ground, a zero offset can be done. The converter can be made to output 0000 0000 digital code for this minimum input voltage by biasing the A/D $V_{IN}(-)$ input at this $V_{IN(MIN)}$ value (see Applications section). This utilizes the differential mode operation of the A/D.

The zero error of the A/D converter relates to the location of the first riser of the transfer function and can be measured by grounding the $V_{IN}$ (−) input and applying a small magnitude positive voltage to the $V_{IN}$ (+) input. Zero error is the difference between the actual DC input voltage that is necessary to just cause an output digital code transition from 0000 0000 to 0000 0001 and the ideal ½ LSB value (½ LSB = 9.8 mV for $V_{REF}/2 = 2.500\ V_{DC}$).

### 2.5.2 Full-Scale

The full-scale adjustment can be made by applying a differential input voltage that is 1½ LSB less than the desired analog full-scale voltage range and then adjusting the magnitude of the $V_{REF}/2$ input (pin 9 or the $V_{CC}$ supply if pin 9 is not used) for a digital output code that is just changing from 1111 1110 to 1111 1111.

#### 2.5.3 Adjusting for an Arbitrary Analog Input Voltage Range

If the analog zero voltage of the A/D is shifted away from ground (for example, to accommodate an analog input signal that does not go to ground) this new zero reference should be properly adjusted first. A $V_{IN}(+)$ voltage that equals this desired zero reference plus ½ LSB (where the LSB is calculated for the desired analog span, 1 LSB = analog span/256) is applied to pin 6 and the zero reference voltage at pin 7 should then be adjusted to just obtain the $00_{HEX}$ to $01_{HEX}$ code transition.

The full-scale adjustment should then be made (with the proper $V_{IN}(-)$ voltage applied) by forcing a voltage to the $V_{IN}(+)$ input which is given by:

$$V_{IN}(+)\ \text{fs adj} = V_{MAX} - 1.5\left[\frac{(V_{MAX} - V_{MIN})}{256}\right],$$

where:

$V_{MAX}$ = The high end of the analog input range

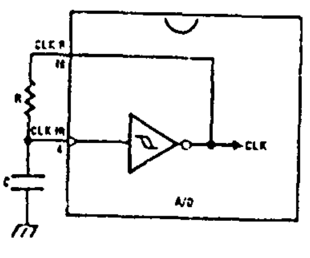
and

$V_{MIN}$ = the low end (the offset zero) of the analog range. (Both are ground referenced.)

The $V_{REF}/2$ (or $V_{CC}$) voltage is then adjusted to provide a code change from $FE_{HEX}$ to $FF_{HEX}$. This completes the adjustment procedure.

### 2.6 Clocking Option

The clock for the A/D can be derived from the CPU clock or an external RC can be added to provide self-clocking. The CLK IN (pin 4) makes use of a Schmitt trigger as shown in *Figure 6*.




$$f_{CLK} \cong \frac{1}{1.1\ RC}$$

$R \cong 10\ k\Omega$

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**FIGURE 6. Self-Clocking the A/D**

Heavy capacitive or DC loading of the clock R pin should be avoided as this will disturb normal converter operation. Loads less than 50 pF, such as driving up to 7 A/D converter clock inputs from a single clock R pin of 1 converter, are allowed. For larger clock line loading, a CMOS or low power TTL buffer or PNP input logic should be used to minimize the loading on the clock R pin (do not use a standard TTL buffer).

### 2.7 Restart During a Conversion

If the A/D is restarted ($\overline{CS}$ and $\overline{WR}$ go low and return high) during a conversion, the converter is reset and a new conversion is started. The output data latch is not updated if the conversion in process is not allowed to be completed, therefore the data of the previous conversion remains in this latch. The $\overline{INTR}$ output simply remains at the "1" level.

### 2.8 Continuous Conversions

For operation in the free-running mode an initializing pulse should be used, following power-up, to ensure circuit operation. In this application, the $\overline{CS}$ input is grounded and the $\overline{WR}$ input is tied to the $\overline{INTR}$ output. This $\overline{WR}$ and $\overline{INTR}$ node should be momentarily forced to logic low following a power-up cycle to guarantee operation.

### 2.9 Driving the Data Bus

This MCS A/D, like MCS microprocessors and memories, will require a bus driver when the total capacitance of the data bus gets large. Other circuitry, which is tied to the data bus, will add to the total capacitive loading, even in TRI-STATE (high impedance mode). Backplane bussing also greatly adds to the stray capacitance of the data bus.

There are some alternatives available to the designer to handle this problem. Basically, the capacitive loading of the data bus slows down the response time, even though DC specifications are still met. For systems operating with a relatively slow CPU clock frequency, more time is available in which to establish proper logic levels on the bus and therefore higher capacitive loads can be driven (see typical characteristics curves).

At higher CPU clock frequencies time can be extended for I/O reads (and/or writes) by inserting wait states (8080) or using clock extending circuits (6800).

Finally, if time is short and capacitive loading is high, external bus drivers must be used. These can be TRI-STATE buffers (low power Schottky such as the DM74LS240 series is recommended) or special higher drive current products which are designed as bus drivers. High current bipolar bus drivers with PNP inputs are recommended.

### 2.10 Power Supplies

Noise spikes on the $V_{CC}$ supply line can cause conversion errors as the comparator will respond to this noise. A low inductance tantalum filter capacitor should be used close to the converter $V_{CC}$ pin and values of 1 µF or greater are recommended. If an unregulated voltage is available in the system, a separate LM340LAZ-5.0, TO-92, 5V voltage regulator for the converter (and other analog circuitry) will greatly reduce digital noise on the $V_{CC}$ supply.

### 2.11 Wiring and Hook-Up Precautions

Standard digital wire wrap sockets are not satisfactory for breadboarding this A/D converter. Sockets on PC boards can be used and all logic signal wires and leads should be grouped and kept as far away as possible from the analog signal leads. Exposed leads to the analog inputs can cause undesired digital noise and hum pickup, therefore shielded leads may be necessary in many applications.

A single point analog ground that is separate from the logic ground points should be used. The power supply bypass capacitor and the self-clocking capacitor (if used) should both be returned to digital ground. Any $V_{REF}/2$ bypass capacitors, analog input filter capacitors, or input signal shielding should be returned to the analog ground point. A test for proper grounding is to measure the zero error of the A/D converter. Zero errors in excess of ¼ LSB can usually be traced to improper board layout and wiring (see section 2.5.1 for measuring the zero error).

## 3.0 TESTING THE A/D CONVERTER

There are many degrees of complexity associated with testing an A/D converter. One of the simplest tests is to apply a known analog input voltage to the converter and use LEDs to display the resulting digital output code as shown in *Figure 7*.

For ease of testing, the $V_{REF}/2$ (pin 9) should be supplied with 2.560 $V_{DC}$ and a $V_{CC}$ supply voltage of 5.12 $V_{DC}$ should be used. This provides an LSB value of 20 mV.

If a full-scale adjustment is to be made, an analog input voltage of 5.090 $V_{DC}$ (5.120–1½ LSB) should be applied to the $V_{IN}(+)$ pin with the $V_{IN}(-)$ pin grounded. The value of the $V_{REF}/2$ input voltage should then be adjusted until the digital output code is just changing from 1111 1110 to 1111 1111. This value of $V_{REF}/2$ should then be used for all the tests.

The digital output LED display can be decoded by dividing the 8 bits into 2 hex characters, the 4 most significant (MS) and the 4 least significant (LS). Table I shows the fractional binary equivalent of these two 4-bit groups. By adding the voltages obtained from the "VMS" and "VLS" columns in Table I, the nominal value of the digital display (when $V_{REF}/2$ = 2.560V) can be determined. For example, for an output LED display of 1011 0110 or B6 (in hex), the voltage values from the table are 3.520 + 0.120 or 3.640 $V_{DC}$. These voltage values represent the center-values of a perfect A/D converter. The effects of quantization error have to be accounted for in the interpretation of the test results.

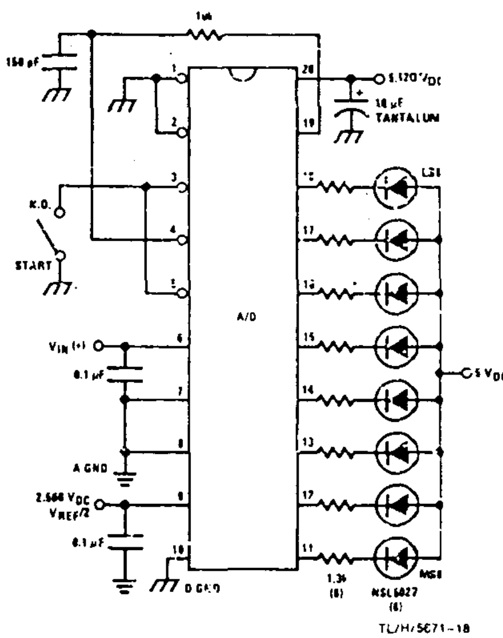


FIGURE 7. Basic A/D Tester

For a higher speed test system, or to obtain plotted data, a digital-to-analog converter is needed for the test set-up. An accurate 10-bit DAC can serve as the precision voltage source for the A/D. Errors of the A/D under test can be expressed as either analog voltages or differences in 2 digital words.

A basic A/D tester that uses a DAC and provides the error as an analog output voltage is shown in *Figure 8*. The 2 op amps can be eliminated if a lab DVM with a numerical subtraction feature is available to read the difference voltage, "A–C", directly. The analog input voltage can be supplied by a low frequency ramp generator and an X-Y plotter can be used to provide analog error (Y axis) versus analog input (X axis). The construction details of a tester of this type are provided in the NSC application note AN-179, "Analog-to-Digital Converter Testing".

For operation with a microprocessor or a computer-based test system, it is more convenient to present the errors digitally. This can be done with the circuit of *Figure 9*, where the output code transitions can be detected as the 10-bit DAC is incremented. This provides ¼ LSB steps for the 8-bit A/D under test. If the results of this test are automatically plotted with the analog input on the X axis and the error (in LSB's) as the Y axis, a useful transfer function of the A/D under test results. For acceptance testing, the plot is not necessary and the testing speed can be increased by establishing internal limits on the allowed error for each code.

## 4.0 MICROPROCESSOR INTERFACING

To discuss the interface with 8080A and 6800 microprocessors, a common sample subroutine structure is used. The microprocessor starts the A/D, reads and stores the results of 16 successive conversions, then returns to the user's program. The 16 data bytes are stored in 16 successive memory locations. All Data and Addresses will be given in hexadecimal form. Software and hardware details are provided separately for each type of microprocessor.

### 4.1 Interfacing 8080 Microprocessor Derivatives (8048, 8085)

This converter has been designed to directly interface with derivatives of the 8080 microprocessor. The A/D can be mapped into memory space (using standard memory address decoding for $\overline{CS}$ and the $\overline{MEMR}$ and $\overline{MEMW}$ strobes) or it can be controlled as an I/O device by using the $\overline{I/O\ R}$ and $\overline{I/O\ W}$ strobes and decoding the address bits A0 → A7 (or address bits A8 → A15 as they will contain the same 8-bit address information) to obtain the $\overline{CS}$ input. Using the I/O space provides 256 additional addresses and may allow a simpler 8-bit address decoder but the data can only be input to the accumulator. To make use of the additional memory reference instructions, the A/D should be mapped into memory space. An example of an A/D in I/O space is shown in *Figure 10*.

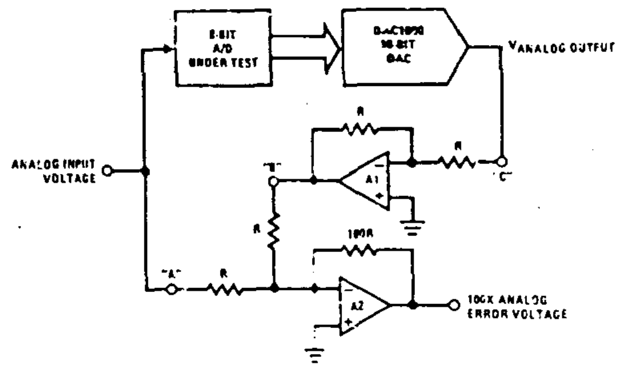


FIGURE 8. A/D Tester with Analog Error Output

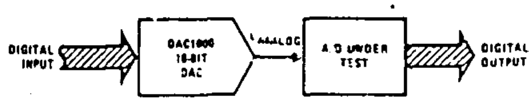


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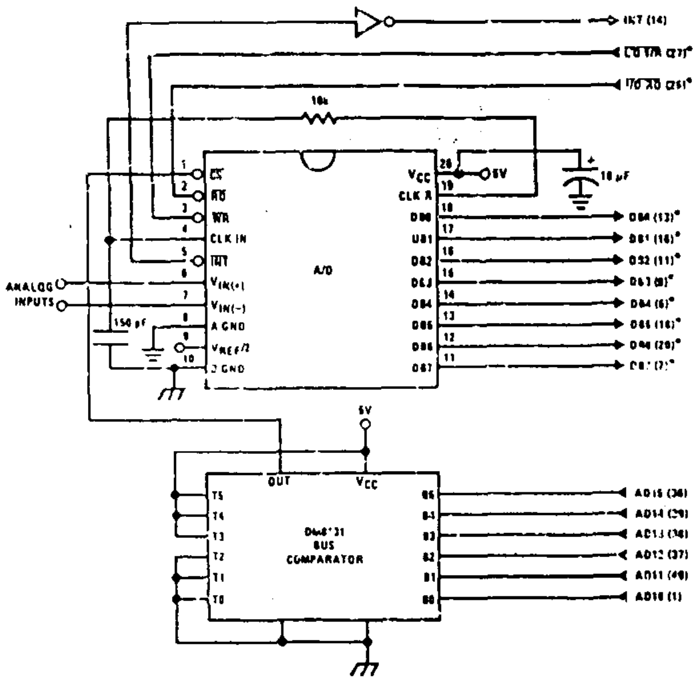
FIGURE 9. Basic "Digital" A/D Tester

**TABLE I. DECODING THE DIGITAL OUTPUT LEDs**

| HEX | BINARY | | | | FRACTIONAL BINARY VALUE FOR | | OUTPUT VOLTAGE CENTER VALUES WITH $V_{REF}/2 = 2.560\ V_{DC}$ | |
|---|---|---|---|---|---|---|---|---|
| | | | | | MS GROUP | LS GROUP | VMS GROUP* | VLS GROUP* |
| F | 1 | 1 | 1 | 1 | 15/16 | 15/256 | 4.800 | 0.300 |
| E | 1 | 1 | 1 | 0 | 7/8 | 7/128 | 4.480 | 0.280 |
| D | 1 | 1 | 0 | 1 | 13/16 | 13/256 | 4.160 | 0.260 |
| C | 1 | 1 | 0 | 0 | 3/4 | 3/64 | 3.840 | 0.240 |
| B | 1 | 0 | 1 | 1 | 11/16 | 11/256 | 3.520 | 0.220 |
| A | 1 | 0 | 1 | 0 | 5/8 | 5/128 | 3.200 | 0.200 |
| 9 | 1 | 0 | 0 | 1 | 9/16 | 9/256 | 2/880 | 0.180 |
| 8 | 1 | 0 | 0 | 0 | 1/2 | 1/32 | 2/560 | 0.160 |
| 7 | 0 | 1 | 1 | 1 | 7/16 | 7/256 | 2.240 | 0.140 |
| 6 | 0 | 1 | 1 | 0 | 3/8 | 3/128 | 1.920 | 0.120 |
| 5 | 0 | 1 | 0 | 1 | 5/16 | 2/256 | 1.600 | 0.100 |
| 4 | 0 | 1 | 0 | 0 | 1/4 | 1/64 | 1/280 | 0.080 |
| 3 | 0 | 0 | 1 | 1 | 3/16 | 3/256 | 0.960 | 0.060 |
| 2 | 0 | 0 | 1 | 0 | 1/8 | 1/128 | 0.640 | 0.040 |
| 1 | 0 | 0 | 0 | 1 | 1/16 | 1/256 | 0.320 | 0.020 |
| 0 | 0 | 0 | 0 | 0 | | | 0 | 0 |

*Display Output = VMS Group + VLS Group

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**Note 1:** *Pin numbers for the DP8228 system controller, others are INS8080A.

**Note 2:** Pin 23 of the INS8228 must be tied to +12V through a 1 kΩ resistor to generate the RST 7 instruction when an interrupt is acknowledged as required by the accompanying sample program.

**FIGURE 10. ADC0801-INS8080A CPU Interface**

**SAMPLE PROGRAM FOR *FIGURE 10* ADC0801-INS8080A CPU INTERFACE**

```
0038   C3 00 03   RST 7:             JMP    LD DATA
  •        •        •
  •        •        •
0100   21 00 02   START:             LXI H 0200H    ; HL pair will point to
                                                    ; data storage locations
0103   31 00 04   RETURN:            LXI SP 0400H   ; Initialize stack pointer (Note 1)
0106   7D                            MOV A, L       ; Test # of bytes entered
0107   FE 0F                         CPI 0F H       ; If # = 16. JMP to
0109   CA 13 01                      JZ CONT        ; user program
010C   D3 E0                         OUT E0 H       ; Start A/D
010E   FB                            EI             ; Enable interrupt
010F   00         LOOP:              NOP            ; Loop until end of
0110   C3 0F 01                      JMP LOOP       ; conversion
0113       •      CONT:                •
  •        •        •                  •
  •        •      (User program to     •
  •        •      process data)        •
  •        •        •                  •
  •        •        •                  •
0300   DB E0      LD DATA:           IN E0 H        ; Load data into accumulator
0302   77                            MOV M, A       ; Store data
0303   23                            INX H          ; Increment storage pointer
0304   C3 03 01                      JMP RETURN
```

**Note 1:** The stack pointer must be dimensioned because a RST 7 instruction pushes the PC onto the stack.

**Note 2:** All address used were arbitrarily chosen.

## Functional Description (Continued)

The standard control bus signals of the 8080 $\overline{CS}$, $\overline{RD}$ and $\overline{WR}$) can be directly wired to the digital control inputs of the A/D and the bus timing requirements are met to allow both starting the converter and outputting the data onto the data bus. A bus driver should be used for larger microprocessor systems where the data bus leaves the PC board and/or must drive capacitive loads larger than 100 pF.

### 4.1.1 Sample 8080A CPU Interfacing Circuitry and Program

The following sample program and associated hardware shown in *Figure 10* may be used to input data from the converter to the INS8080A CPU chip set (comprised of the INS8080A microprocessor, the INS8228 system controller and the INS8224 clock generator). For simplicity, the A/D is controlled as an I/O device, specifically an 8-bit bi-directional port located at an arbitrarily chosen port address, E0. The TRI-STATE output capability of the A/D eliminates the need for a peripheral interface device, however address decoding is still required to generate the appropriate $\overline{CS}$ for the converter.

It is important to note that in systems where the A/D converter is 1-of-8 or less I/O mapped devices, no address decoding circuitry is necessary. Each of the 8 address bits (A0 to A7) can be directly used as $\overline{CS}$ inputs—one for each I/O device.

### 4.1.2 INS8048 Interface

The INS8048 interface technique with the ADC0801 series (see *Figure 11*) is simpler than the 8080A CPU interface. There are 24 I/O lines and three test input lines in the 8048. With these extra I/O lines available, one of the I/O lines (bit 0 of port 1) is used as the chip select signal to the A/D, thus eliminating the use of an external address decoder. Bus control signals $\overline{RD}$, $\overline{WR}$ and $\overline{INT}$ of the 8048 are tied directly to the A/D. The 16 converted data words are stored at on-chip RAM locations from 20 to 2F (Hex). The $\overline{RD}$ and $\overline{WR}$ signals are generated by reading from and writing into a dummy address, respectively. A sample interface program is shown below.

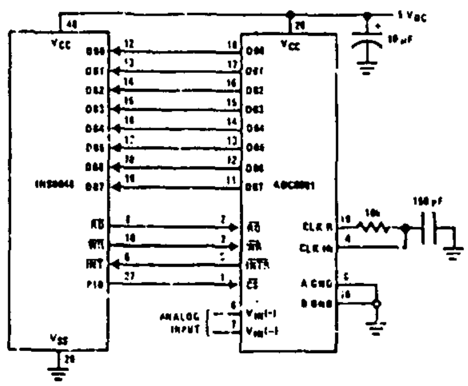

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**FIGURE 11. INS8048 Interface**

**SAMPLE PROGRAM FOR *FIGURE 11* INS8048 INTERFACE**

```
04 10                 JMP     10H        ; Program starts at addr 10
                      ORG     3H
04 50                 JMP     50H        ; Interrupt jump vector
                      ORG     10H        ; Main program
99 FE                 ANL     P1, #0FEH  ; Chip select
81                    MOVX    A, @R1     ; Read in the 1st data
                                         ; to reset the intr
89 01     START:      ORL     P1, #1     ; Set port pin high
B8 20                 MOV     R0, #20H   ; Data address
B9 FF                 MOV     R1, #0FFH  ; Dummy address
BA 10                 MOV     R2, #10H   ; Counter for 16 bytes
23 FF     AGAIN:      MOV     A, #0FFH   ; Set ACC for intr loop
99 FE                 ANL     P1, #0FEH  ; Send CS (bit 0 of P1)
91                    MOVX    @R1, A     ; Send WR out
05                    EN      I          ; Enable interrupt
96 21     LOOP:       JNZ     LOOP       ; Wait for interrupt
EA 1B                 DJNZ    R2, AGAIN  ; If 16 bytes are read
00                    NOP                ; go to user's program
00                    NOP
                      ORG     50H
81        INDATA:     MOVX    A, @R1     ; Input data, CS still low
A0                    MOV     @R0, A     ; Store in memory
18                    INC     R0         ; Increment storage counter
89 01                 ORL     P1, #1     ; Reset CS signal
27                    CLR     A          ; Clear ACC to get out of
93                    RETR               ; the interrupt loop
```

### 4.2 Interfacing the Z-80

The Z-80 control bus is slightly different from that of the 8080. General $\overline{RD}$ and $\overline{WR}$ strobes are provided and separate memory request, $\overline{MREQ}$, and I/O request, $\overline{IORQ}$, signals are used which have to be combined with the generalized strobes to provide the equivalent 8080 signals. An advantage of operating the A/D in I/O space with the Z-80 is that the CPU will automatically insert one wait state (the $\overline{RD}$ and $\overline{WR}$ strobes are extended one clock period) to allow more time for the I/O devices to respond. Logic to map the A/D in I/O space is shown in *Figure 13*.

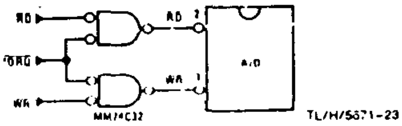



FIGURE 13. Mapping the A/D as an I/O Device for Use with the Z-80 CPU

Additional I/O advantages exist as software DMA routines are available and use can be made of the output data transfer which exists on the upper 8 address lines (A8 to A15) during I/O input instructions. For example, MUX channel selection for the A/D can be accomplished with this operating mode.

### 4.3 Interfacing 6800 Microprocessor Derivatives (6502, etc.)

The control bus for the 6800 microprocessor derivatives does not use the $\overline{RD}$ and $\overline{WR}$ strobe signals. Instead it employs a single R/$\overline{W}$ line and additional timing, if needed, can be derived fom the $\phi 2$ clock. All I/O devices are memory mapped in the 6800 system, and a special signal, VMA, indicates that the current address is valid. *Figure 14* shows an interface schematic where the A/D is memory mapped in the 6800 system. For simplicity, the $\overline{CS}$ decoding is shown using ½ DM8092. Note that in many 6800 systems, an already decoded ... brought out to the common bus at pin 21. This can be tied directly to the $\overline{CS}$ pin of the A/D, provided that no other devices are addressed at HX ADDR: 4XXX or 5XXX.

The following subroutine performs essentially the same function as in the case of the 8080A interface and it can be called from anywhere in the user's program.

In *Figure 15* the ADC0801 series is interfaced to the M6800 microprocessor through (the arbitrarily chosen) Port B of the MC6820 or MC6821 *Peripheral Interface Adapter*, (PIA). Here the $\overline{CS}$ pin of the A/D is grounded since the PIA is already memory mapped in the M6800 system and no $\overline{CS}$ decoding is necessary. Also notice that the A/D output data lines are connected to the microprocessor bus under program control through the PIA and therefore the A/D $\overline{RD}$ pin can be grounded.

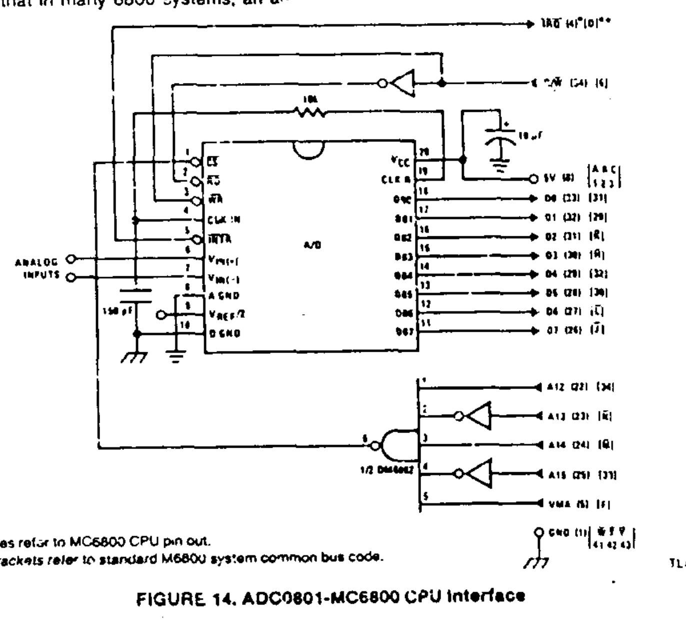
A sample interface program equivalent to the previous one is shown below *Figure 15*. The PIA Data and Control Registers of Port B are located at HEX addresses 8006 and 8007, respectively.

### 5.0 GENERAL APPLICATIONS

The following applications show some interesting uses for the A/D. The fact that one particular microprocessor is used is not meant to be restrictive. Each of these application circuits would have its counterpart using any microprocessor that is desired.

### 5.1 Multiple ADC0801 Series to MC6800 CPU Interface

To transfer analog data from several channels to a single microprocessor system, a multiple converter scheme presents several advantages over the conventional multiplexer *single-converter* approach. With the ADC0801 series, the differential inputs allow individual span adjustment for each channel. Furthermore, all analog input channels are sensed simultaneously, which essentially divides the microprocessor's total system servicing time by the number of channels, since all conversions occur simultaneously. This scheme is shown in *Figure 16*.




**Note 1:** Numbers in parentheses refer to MC6800 CPU pin out.

**Note 2:** Number or letters in brackets refer to standard M6800 system common bus code.

FIGURE 14. ADC0801-MC6800 CPU Interface

## Functional Description (Continued)

**SAMPLE PROGRAM FOR *FIGURE 14* ADC0801-MC6800 CPU INTERFACE**

```
0010   DF 36      DATAIN   STX    TEMP2     ; Save contents of X
0012   CE 00 2C            LDX    #$002C    ; Upon IRQ low CPU
0015   FF FF F8            STX    $FFF8     ; jumps to 002C
0018   B7 50 00            STAA   $5000     ; Start ADC0801
001B   0E                  CLI
001C   3E         CONVRT   WAI              ; Wait for interrupt
001D   DE 34               LDX    TEMP1
001F   8C 02 0F            CPX    #$020F    ; Is final data stored?
0022   27 14               BEQ    ENDP
0024   B7 50 00            STAA   $5000     ; Restarts ADC0801
0027   08                  INX
0028   DF 34               STX    TEMP1
002A   20 F0               BRA    CONVRT
002C   DE 34      INTRPT   LDX    TEMP1
002E   B6 50 00            LDAA   $5000     ; Read data
0031   A7 00               STAA   X         ; Store it at X
0033   3B                  RTI
0034   02 00      TEMP1    FDB    $0200     ; Starting address for
                                            ; data storage
0036   00 00      TEMP2    FDB    $0000
0038   CE 02 00   ENDP     LDX    #$0200    ; Reinitialize TEMP1
003B   DF 34               STX    TEMP1
003D   DE 36               LDX    TEMP2
003F   39                  RTS              ; Return from subroutine
                                            ; To user's program
```

Note 1: In order for the microprocessor to service subroutines and interrupts, the stack pointer must be dimensioned in the user's program.

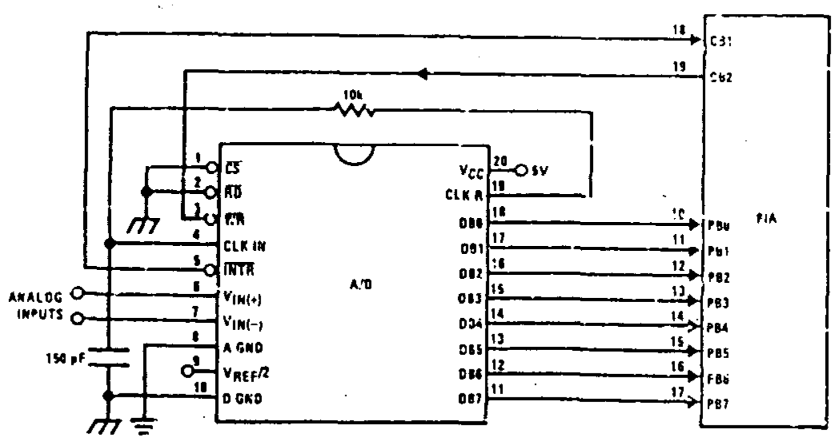



FIGURE 15. ADC0801-MC6820 PIA Interface

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## Functional Description (Continued)

**SAMPLE PROGRAM FOR *FIGURE 15* ADC0801–MC6820 PIA INTERFACE**

```
0010  CE 00 38   DATAIN   LDX   #$0038    ; Upon IRQ low CPU
0013  FF FF F8            STX   $FFF8     ; jumps to 0038
0016  B6 80 06            LDAA  PIAORB    ; Clear possible IRQ flags
0019  4F                  CLRA
001A  B7 80 07            STAA  PIACRB
001D  B7 80 06            STAA  PIAORB    ; Set Port B as input
0020  0E                  CLI
0021  C6 34               LDAB  #$34
0023  86 3D               LDAA  #$3D
0025  F7 80 07   CONVRT   STAB  PIACRB    ; Starts ADC0801
0028  B7 80 07            STAA  PIACRB
002B  3E                  WAI             ; Wait for interrupt
002C  DE 40               LDX   TEMP1
002E  8C 02 0F            CPX   #$020F    ; Is final data stored?
0031  27 0F               BEQ   ENDP
0033  08                  INX
0034  DF 40               STX   TEMP1
0036  20 ED               BRA   CONVRT
0038  DE 40      INTRPT   LDX   TEMP1
003A  B6 80 06            LDAA  PIAORB    ; Read data in
003D  A7 00               STAA  X         ; Store it at X
003F  3B                  RTI
0040  02 00      TEMP1    FDB   $0200     ; Starting address for
                                          ; data storage
0042  CE 02 00   ENDP     LDX   #$0200    ; Reinitialize TEMP1
0045  DF 40               STX   TEMP1
0047  39                  RTS             ; Return from subroutine
                 PIAORB   EQU   $8006     ; To user's program
                 PIACRB   EQU   $8007
```

The following schematic and sample subroutine (DATA IN) may be used to interface (up to) 8 ADC0801's directly to the MC6800 CPU. This scheme can easily be extended to allow the interface of more converters. In this configuration the converters are (arbitrarily) located at HEX address 5000 in the MC6800 memory space. To save components, the clock signal is derived from just one RC pair on the first converter. This output drives the other A/Ds.

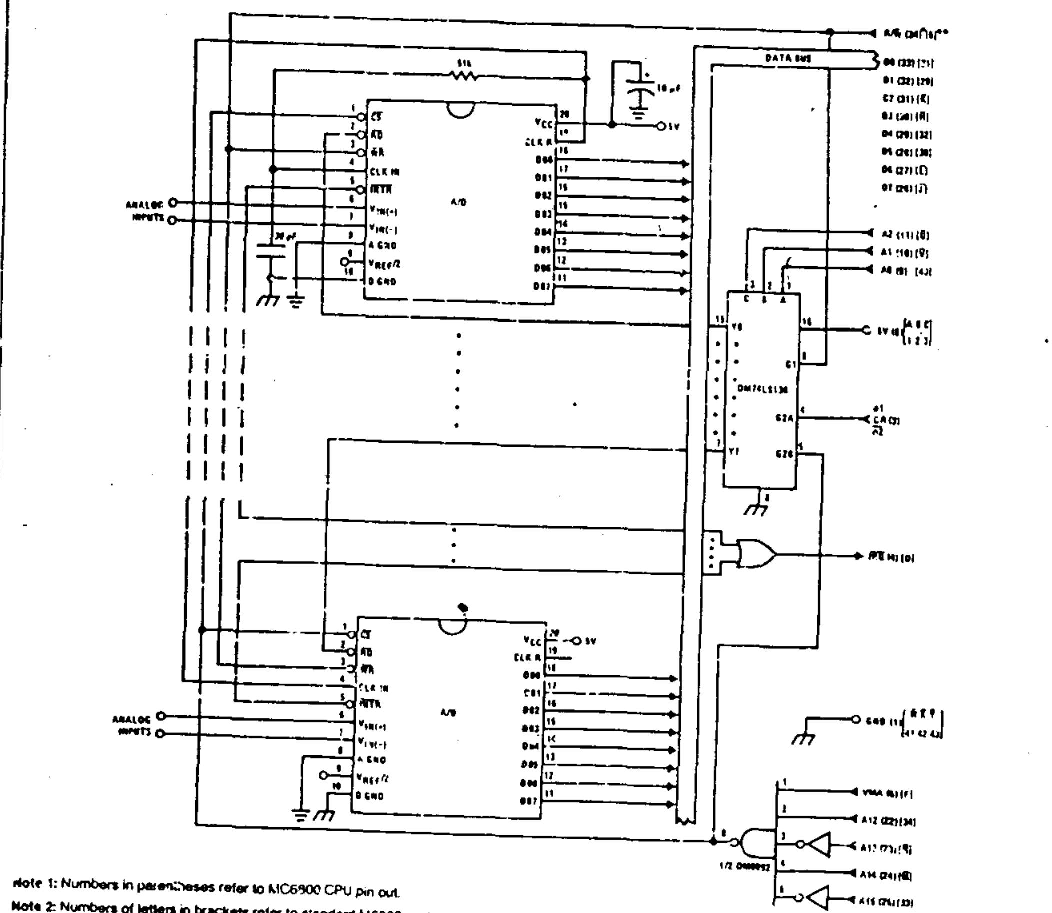
All the converters are started simultaneously with a STORE instruction at HEX address 5000. Note that any other HEX address of the form 5XXX will be decoded by the circuit, pulling all the $\overline{CS}$ inputs low. This can easily be avoided by using a more definitive address decoding scheme. All the interrupts are ORed together to insure that all A/Ds have completed their conversion before the microprocessor is interrupted.

The subroutine, DATA IN, may be called from anywhere in the user's program. Once called, this routine initializes the CPU, starts all the converters simultaneously and waits for the interrupt signal. Upon receiving the interrupt, it reads the converters (from HEX addresses 5000 through 5007) and stores the data successively at (arbitrarily chosen) HEX addresses 0200 to 0207, before returning to the user's program. All CPU registers then recover the original data they had before servicing DATA IN.

### 5.2 Auto-Zeroed Differential Transducer Amplifier and A/D Converter

The differential inputs of the ADC0801 series eliminate the need to perform a differential to single ended conversion for a differential transducer. Thus, one op amp can be eliminated since the differential to single ended conversion is provided by the differential input of the ADC0801 series. In general, a transducer preamp is required to take advantage of the full A/D converter input dynamic range.

## Functional Description (Continued)



Note 1: Numbers in parentheses refer to MC6800 CPU pin out.

Note 2: Numbers of letters in brackets refer to standard M6800 system common bus code.

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FIGURE 16. Interfacing Multiple A/Ds in an MC6800 System

**SAMPLE PROGRAM FOR *FIGURE 16* INTERFACING MULTIPLE A/Ds IN AN MC6800 SYSTEM**

| ADDRESS | HEX CODE | | MNEMONICS | | COMMENTS |
|---|---|---|---|---|---|
| 0010 | DF 44 | DATAIN | STX | TEMP | ; Save Contents of X |
| 0012 | CE 00 2A | | LDX | #$002A | ; Upon $\overline{IRQ}$ LOW CPU |
| 0015 | FF FF F8 | | STX | $FFF8 | ; Jumps to 002A |
| 0018 | B7 50 00 | | STAA | $5000 | ; Starts all A/D's |
| 001B | 0E | | CLI | | |
| 001C | 3E | | WAI | | ; Wait for interrupt |
| 001D | CE 50 00 | | LDX | #$5000 | |
| 0020 | DF 40 | | STX | INDEX1 | ; Reset both INDEX |
| 0022 | CE 02 00 | | LDX | #$0200 | ; 1 and 2 to starting |
| 0025 | DF 42 | | STX | INDEX2 | ; addresses |
| 0027 | DE 44 | | LDX | TEMP | |
| 0029 | 39 | | RTS | | ; Return from subroutine |
| 002A | DE 40 | INTRPT | LDX | INDEX1 | ; INDEX1 → X |
| 002C | A6 00 | | LDAA | X | ; Read data in from A/D at X |
| 002E | 08 | | INX | | ; Increment X by one |
| 002F | DF 40 | | STX | INDEX1 | ; X → INDEX1 |
| 0031 | DE 42 | | LDX | INDEX2 | ; INDEX2 → X |

**SAMPLE PROGRAM FOR *FIGURE 16* INTERFACING MULTIPLE A/Ds IN AN MC6800 SYSTEM**

| ADDRESS | HEX CODE | MNEMONICS | | | COMMENTS |
|---|---|---|---|---|---|
| 0033 | A7 00 | | STAA | X | ; Store data at X |
| 0035 | 8C 02 07 | | CPX | #$0207 | ; Have all A/D's been read? |
| 0038 | 27 05 | | BEQ | RETURN | ; Yes: branch to RETURN |
| 003A | 08 | | INX | | ; No: increment X by one |
| 003B | DF 42 | | STX | INDEX2 | ; X → INDEX2 |
| 003D | 20 EB | | BRA | INTRPT | ; Branch to 002A |
| 003F | 3B | RETURN | RTI | | |
| 0040 | 50 00 | INDEX1 | FDB | $5000 | ; Starting address for A/D |
| 0042 | 02 00 | INDEX2 | FDB | $0200 | ; Starting address for data storage |
| 0044 | 00 00 | TEMP | FDB | $0000 | |

**Note 1:** In order for the microprocessor to service subroutines and interrupts, the stack pointer must be dimensioned in the user's program.

For amplification of DC input signals, a major system error is the input offset voltage of the amplifiers used for the preamp. *Figure 17* is a gain of 100 differential preamp whose offset voltage errors will be cancelled by a zeroing subroutine which is performed by the INS8080A microprocessor system. The total allowable input offset voltage error for this preamp is only 50 $\mu$V for ¼ LSB error. This would obviously require very precise amplifiers. The expression for the differential output voltage of the preamp is:

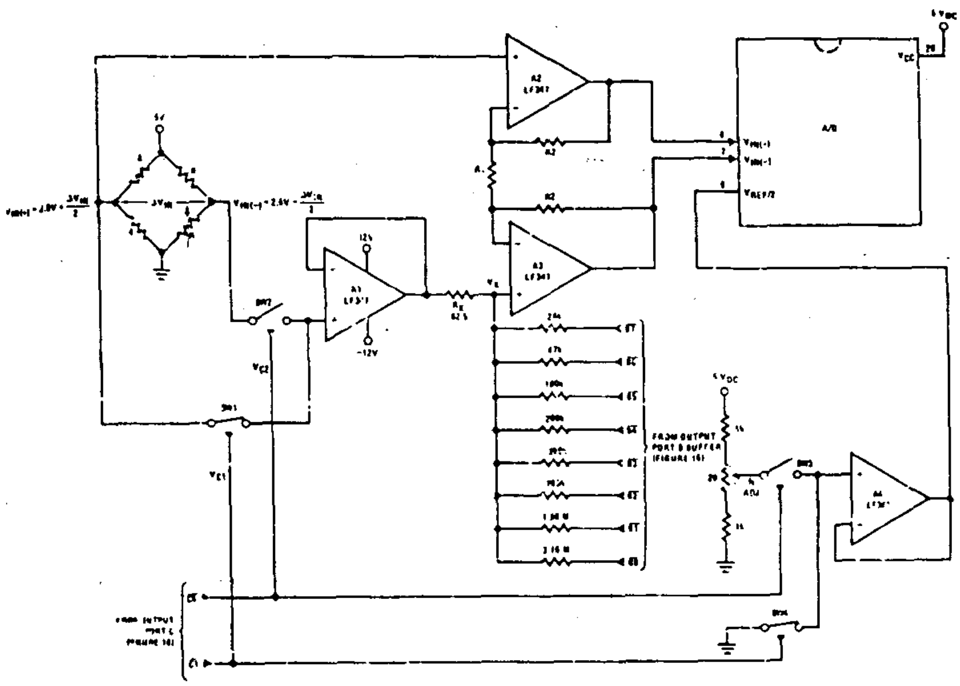
$$V_O = \underbrace{[V_{IN}(+) - V_{IN}(-)]}_{\text{SIGNAL}} \underbrace{\left[1 + \frac{2R2}{R1}\right]}_{\text{GAIN}} +$$

$$\underbrace{(V_{OS_2} - V_{OS_1} - V_{OS_3} \pm I_X R_X)}_{\text{DC ERROR TERM}} \underbrace{\left(1 + \frac{2R2}{R1}\right)}_{\text{GAIN}}$$

where $I_X$ is the current through resistor $R_X$. All of the offset error terms can be cancelled by making $\pm I_X R_X = V_{OS1} + V_{OS3} - V_{OS2}$. This is the principle of this auto-zeroing scheme.

The INS8080A uses the 3 I/O ports of an INS8255 Programable Peripheral Interface (PPI) to control the auto zeroing and input data from the ADC0801 as shown in *Figure 18*. The PPI is programmed for basic I/O operation (mode 0) with Port A being an input port and Ports B and C being output ports. Two bits of Port C are used to alternately open or close the 2 switches at the input of the preamp. Switch SW1 is closed to force the preamp's differential input to be zero during the zeroing subroutine and then opened and SW2 is then closed for conversion of the actual differential input signal. Using 2 switches in this manner eliminates concern for the ON resistance of the switches as they must conduct only the input bias current of the input amplifiers.

Output Port B is used as a successive approximation register by the 8080 and the binary scaled resistors in series with each output bit create a D/A converter. During the zeroing subroutine, the voltage at $V_x$ increases or decreases as required to make the differential output voltage equal to zero. This is accomplished by ensuring that the voltage at the output of A1 is approximately 2.5V so that a logic "1" (5V) on any output of Port B will source current into node $V_X$ thus raising the voltage at $V_X$ and making the output differential more negative. Conversely, a logic "0" (0V) will pull current out of node $V_X$ and decrease the voltage, causing the differential output to become more positive. For the resistor values shown, $V_X$ can move $\pm$12 mV with a resolution of 50 $\mu$V, which will null the offset error term to ¼ LSB of full-scale for the ADC0801. It is important that the voltage levels that drive the auto-zero resistors be constant. Also, for symmetry, a logic swing of 0V to 5V is convenient. To achieve this, a CMOS buffer is used for the logic output signals of Port B and this CMOS package is powered with a stable 5V source. Buffer amplifier A1 is necessary so that it can source or sink the D/A output current.



Note 1: R2 = 49.5 R1

Note 2: Switches are LMC 3334 CMOS analog switches.

Note 3: The 9 resistors used in the auto-zero section can be ±5% tolerance.

FIGURE 17. Gain of 100 Differential Transducer Preamp

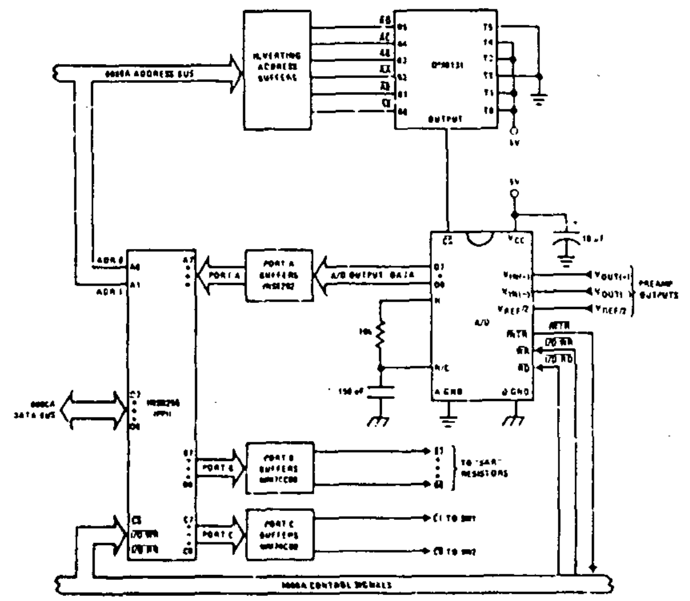


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FIGURE 18. Microprocessor Interface Circuitry for Differential Preamp

all zero code when it converts a negative input [$V_{IN}(-) \geq V_{IN}(+)$]. Also, a logic inversion exists as all of the I/O ports are buffered with inverting gates.

Basically, if the data read is zero, the differential output voltage is negative, so a bit in Port B is cleared to pull $V_X$ more negative which will make the output more positive for the next conversion. If the data read is not zero, the output voltage is positive so a bit in Port B is set to make $V_X$ more positive and the output more negative. This continues for 8 approximations and the differential output eventually converges to within 5 mV of zero.

The actual program is given in *Figure 20*. All addresses used are compatible with the BLC 80/10 microcomputer system. In particular:

Port A and the ADC0801 are at port address E4

Port B is at port address E5

Port C is at port address E6

PPI control word port is at port address E7

Program Counter automatically goes to ADDR:3C3D upon acknowledgement of an interrupt from the ADC0801

### 5.3 Multiple A/D Converters in a Z-80 Interrupt Driven Mode

In data acquisition systems where more than one A/D converter (or other peripheral device) will be interrupting program execution of a microprocessor, there is obviously a need for the CPU to determine which device requires servicing. *Figure 21* and the accompanying software is a method of determining which of 7 ADC0801 converters has completed a conversion ($\overline{INTR}$ asserted) and is requesting an interrupt. This circuit allows starting the A/D converters in any sequence, but will input and store valid data from the converters with a priority sequence of A/D 1 being read first, A/D 2 second, etc., through A/D 7 which would have the lowest priority for data being read. Only the converters whose INT is asserted will be read.

The key to decoding circuitry is the DM74LS373, 8-bit D type flip-flop. When the Z-80 acknowledges the interrupt, the program is vectored to a data input Z-80 subroutine. This subroutine will read a peripheral status word from the DM74LS373 which contains the logic state of the $\overline{INTR}$ outputs of all the converters. Each converter which initiates an interrupt will place a logic "0" in a unique bit position in the status word and the subroutine will determine the identity of the converter and execute a data read. An identifier word (which indicates which A/D the data came from) is stored in the next sequential memory location above the location of the data so the program can keep track of the identity of the data entered.

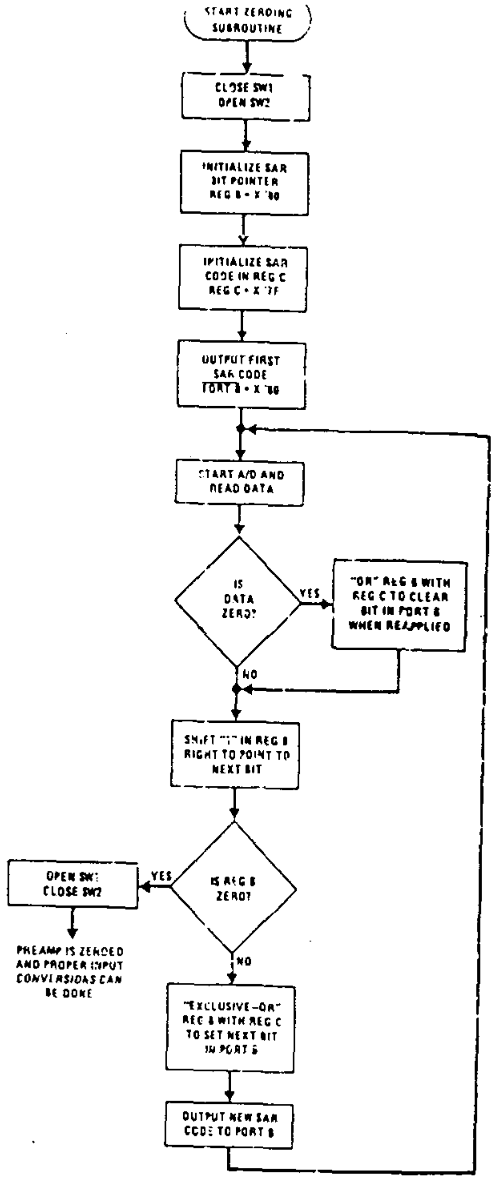


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FIGURE 19. Flow Chart for Auto-Zero Routine

```
3D02   D3??     Out Control Port
3D04   ??01     MVI ? 01                                    ; Program PPI
                                  Auto-Zero Subroutine
3D07   D3E6     OUT C
3D09   0680     MVI B 80                                    ; Close SW1 open SW2
3D0B   3E7F     MVI A 7F                                    ; Initialize SAR bit pointer
3D0D   4F       MOV C,A                                     ; Initialize SAR code
3D0E   D3E5     OUT B             Return
3D10   31AA3D   LXI SP 3DAA                                 ; Port B = SAR code
3D13   D3E4     OUT A             Start                     ; Dimension stack pointer
3D15   FB       EI                                          ; Start A/D
3D16   00       NOP
3D17   C3163D   JMP Loop          Loop                      ; Loop until INT asserted
3D1A   7A       MOV A,D
3D1B   C600     ADI 00            Auto-Zero
3D1D   CA2D3D   JZ Set C
3D20   78       MOV A,B                                     ; Test A/D output data for zero
3D21   F600     ORI 00            Shift B
3D23   1F       RAR                                         ; Clear carry
3D24   FE00     CPI 00                                      ; Shift "1" in B right one place
3D26   CA373D   JZ Done                                     ; Is B zero? If yes last
3D29   47       MOV B,A                                     ; approximation has been made
3D2A   C3333D   JMP New C
3D2D   79       MOV A,C
3D2E   B0       ORA B             Set C
3D2F   4F       MOV C,A                                     ; Set bit in C that is in same
3D30   C3203D   JMP Shift B                                 ; position as "1" in B
3D33   A9       XRA C
3D34   C30D3D   JMP Return        New C                     ; Clear bit in C that is in
3D37   47       MOV B,A                                     ; same position as "1" in B
3D38   7C       MOV A,H           Done                      ; then output new SAR code.
3D39   EE03     XRI 03                                      ; Open SW1, close SW2 then
3D3B   D3E6     OUT C                                       ; proceed with program. Preamp
3D3D            •                                           ; is now zeroed.
                •                 Normal
                •
                Program for processing
                proper data values
3C3D   DBE4     IN A              Read A/D Subroutine       ; Read A/D data
3C3F   EEFF     XRI FF                                      ; Invert data
3C41   57       MOV D,A
3C42   78       MOV A,B
3C43   E6FF     ANI FF                                      ; Is B Reg = 0? If not stay
3C45   C21A3D   JNZ Auto-Zero                               ; in auto zero subroutine
3C48   C33D3D   JMP Normal
```

Note: All numerical values are hexadecimal representations.

**FIGURE 20. Software for Auto-Zeroed Differential A/D**

### 5.3 Multiple A/D Converters in a Z-80® Interrupt Driven Mode (Continued)

The following notes apply:

1) It is assumed that the CPU automatically performs a RST 7 instruction when a valid interrupt is acknowledged (CPU is in interrupt mode 1). Hence, the subroutine starting address of X0038.

2) The address bus from the Z-80 and the data bus to the Z-80 are assumed to be inverted by bus drivers.

3) A/D data and identifying words will be stored in sequential memory locations starting at the arbitrarily chosen address X 3E00.

4) The stack pointer must be dimensioned in the main program as the RST 7 instruction automatically pushes the PC onto the stack and the subroutine uses an additional 6 stack addresses.

5) The peripherals of concern are mapped into I/O space with the following port assignments:

| HEX PORT ADDRESS | PERIPHERAL |
|---|---|
| 00 | MM74C374 8-bit flip-flop |
| 01 | A/D 1 |
| 02 | A/D 2 |
| 03 | A/D 3 |
| 04 | A/D 4 |
| 05 | A/D 5 |
| 06 | A/D 6 |
| 07 | A/D 7 |

This port address also serves as the A/D identifying word in the program.

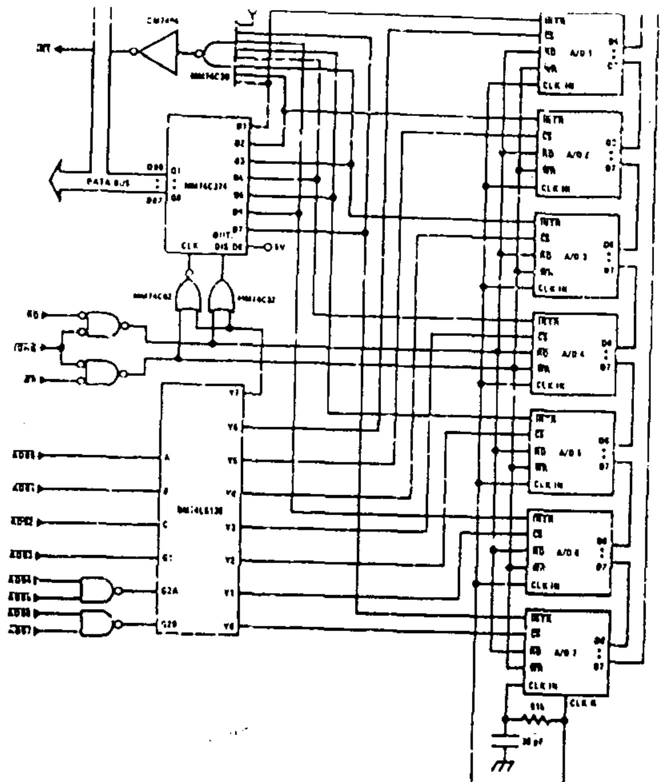


FIGURE 21. Multiple A/Ds with Z-80 Type Microprocessor

TL/H/5671-29

**INTERRUPT SERVICING SUBROUTINE**

| LOC | OBJ CODE | | SOURCE STATEMENT | COMMENT |
|---|---|---|---|---|
| 0038 | E5 | | PUSH HL | ; Save contents of all registers affected by |
| 0039 | C5 | | PUSH BC | ; this subroutine. |
| 003A | F5 | | PUSH AF | ; Assumed INT mode 1 earlier set. |
| 003B | 21 00 3E | | LD (HL), X3E00 | ; Initialize memory pointer where data will be stored. |
| 003E | 0E 01 | | LD C, X01 | ; C register will be port ADDR of A/D converters. |
| 0040 | D300 | | OUT X00, A | ; Load peripheral status word into 8-bit latch. |
| 0042 | DB00 | | IN A, X00 | ; Load status word into accumulator. |
| 0044 | 47 | | LD B, A | ; Save the status word. |
| 0045 | 79 | TEST | LD A, C | ; Test to see if the status of all A/D's have |
| 0046 | FE 08 | | CP, X08 | ; been checked. If so, exit subroutine |
| 0048 | CA 60 00 | | JPZ, DONE | |
| 04B | 78 | | LD A, B | ; Test a single bit in status word by looking for |
| 04C | 1F | | RRA | ; a "1" to be rotated into the CARRY (an $\overline{INT}$ |
| 04D | 47 | | LD B, A | ; is loaded as a "1"). If CARRY is set then load |
| 04E | DA 5500 | | JPC, LOAD | ; contents of A/D at port ADDR in C register. |
| 051 | 0C | NEXT | INC C | ; If CARRY is not set, increment C register to point |
| 052 | C3 4500 | | JP, TEST | ; to next A/D, then test next bit in status word. |
| 055 | ED 78 | LOAD | IN A, (C) | ; Read data from interrupting A/D and invert |
| 057 | EE FF | | XOR FF | ; the data. |
| 059 | 77 | | LD (HL), A | ; Store the data |
| 05A | 2C | | INC L | |
| 05B | 71 | | LD (HL), C | ; Store A/D identifier (A/D port ADDR). |
| 05C | 2C | | INC L | |
| 5D | C3 51 00 | | JP, NEXT | ; Test next bit in status word. |
| 60 | F1 | DONE | POP AF | ; Re-establish all registers as they were |
| 61 | C1 | | POP BC | ; before the interrupt. |
| 62 | E1 | | POP HL | |
| 63 | C9 | | RET | ; Return to original program |

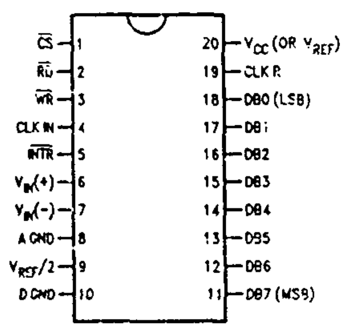
## Ordering Information

| TEMP RANGE | | 0°C TO 70°C | 0°C TO 70°C | 0°C TO 70°C | −40°C TO +85°C |
|---|---|---|---|---|---|
| ERROR | ± 1/4 Bit Adjusted | | | | ADC0801LCN |
| | ± 1/2 Bit Unadjusted | ADC0802LCWM | ADC0802LCV | | ADC0802LCN |
| | ± 1/2 Bit Adjusted | ADC0803LCWM | ADC0803LCV | | ADC0803LCN |
| | ± 1 Bit Unadjusted | ADC0804LCWM | ADC0804LCV | ADC0804LCN | ADC0805LCN |
| PACKAGE OUTLINE | | M20B—Small Outline | V20A—Chip Carrier | N20A—Molded DIP | |

| TEMP RANGE | | −40°C TO +85°C | −55°C TO +125°C |
|---|---|---|---|
| ERROR | ± 1/4 Bit Adjusted | ADC0801LCJ | ADC0801LJ |
| | ± 1/2 Bit Unadjusted | ADC0802LCJ | ADC0802LJ |
| | ± 1/2 Bit Adjusted | ADC0803LCJ | |
| | ± 1 Bit Unadjusted | ADC0804LCJ | |
| PACKAGE OUTLINE | | J20A—Cavity DIP | J20A—Cavity DIP |

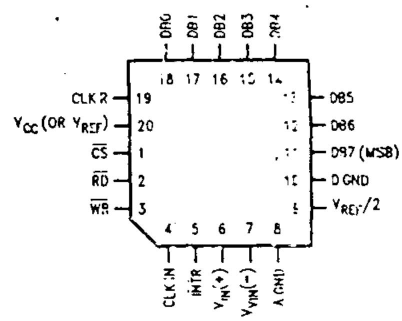
## Connection Diagrams

**ADC080X**
**Dual-In-Line and Small Outline (SO) Packages**




TL/H/5671-30

**ADC080X**
**Molded Chip Carrier (PCC) Package**




TL/H/5671-32

**See Ordering Information**

# LAMPIRAN B

```
;----------
; Constants
;----------

;-----------------
; Memory Allocation
;-----------------

Timer_Status        EQU   30h   ; status utk timer 0
                              ; 0 -> dipakai untuk delay geser pada header
                              ; 1 -> untuk menghitung lebar pulsa data infrared
Sec_Tick      EQU   31h   ; variabel utk counter timer
X_Header      EQU   32h   ; variabel utk posisi pergeseran tulisan pada header
J_Header      EQU   33h   ; variabel yg berisi banyaknya karakter pada tulisan
header
Mode          EQU   32h   ; variabel yg menunjukkan mode yg ditampilkan pada LCD
                          ; mode 1 = menampilkan nilai SP dan PV
                          ; mode 2 = menampilkan status kran
                          ; mode 3 = input nilai SP dari keypad
                          ; mode 4 = Verifikasi pembukaan kran isi
                          ; mode 5 = Verifikasi penutupan kran isi
                          ; mode 6 = Verifikasi pembukaan kran buang
                          ; mode 7 = Verifikasi penutupan kran buang
                          ; mode 8 = pesan error bila SP yg dimasukkan > 100
                          ; mode 9 = menampilkan level air dan status heater
                          ; mode 10= pesan error apabila membuka kran isi padahal
                          ;          air sudah penuh
X_Enter_SP   EQU   33h   ; variabel koordinat X posisi kursor saat menginputkan
SP
Present_Value       EQU   34h   ; variabel utk menyimpan nilai PV (suhu sekarang)
Set_Point    EQU   35h   ; variabel utk menyimpan nilai set point

Buffer_SP    EQU   36h   ; variabel untuk menampung 3 digit nilai
;                  37h   ; desimal dari SP pada saat diinputkan
;                  38h   ;

Tank_Status EQU   39h   ; Status level air : 0 -> kosong, 1 -> terisi, 2 ->
penuh
Data_Counter        EQU   3Ah   ; variabel counter jumlah pulsa data yg akan
dikirim ke kontroler 1
Ctrl_Status EQU   3Bh   ; variabel yg menampung nilai kontrol status
Counter             EQU   3Ch   ; variabel counter jumlah pulsa data yg diterima
dari kontroler 1
Set_Ctrl_St EQU   3Dh   ; variabel penampung nilai kontrol status yg akan
dikirimkan ke kontroler 1

;----------------
; Bit Addressable
;----------------

LCD_RS              BIT   p3.6  ; pin output untuk register select LCD
LCD_CS              BIT   p3.7  ; pin output enable LCD
Scan_Key_1   BIT   p2.6   ;
Scan_Key_2   BIT   p2.5   ; pin output pembacaan matrix keypad
Scan_Key_3   BIT   p2.4   ;
Scan_Key_4   BIT   p2.3   ;
IR_TX        BIT   p3.4   ; pin output transmitter IR
```

```
IR_RX        BIT   p3.2  ; pin input receiver IR

;-----------------
; Flag / Indicator
;-----------------

Button_F     BIT   00h   ; 0 -> idle, 1 -> lakukan pembacaan tombol
Header_F     BIT   01h   ; 0 -> idle, 1 -> refresh tampilan header pada LCD
Show_Header_F      BIT   02h   ; 0 -> header tdk ditampilkan, 1 -> header
ditampilkan
Upper_Valve BIT   03h   ; 0 -> close, 1 -> open
Lower_Valve BIT   04h   ; 0 -> close, 1 -> open
Upper_Valve_C      BIT   05h   ; 0 -> close, 1 -> open
Lower_Valve_C      BIT   06h   ; 0 -> close, 1 -> open
Heater             BIT   07h   ; 0 -> stop,  1 -> active
Update_Mode_F      BIT   08h   ; 0 -> idle, 1 -> refresh tampilan pada LCD
Data_Type_F BIT   09h   ; 0 -> data PV, 1 -> data kontrol status
Send_Data_F BIT   0Ah   ; data yg akan dikirim : 0 -> data SP, 1 -> data kontrol
status
No_Data_F    BIT   0Bh   ; 0 -> masih ada data yg diterima, 1 -> tidak ada data
yg masuk
                         ;                                  setelah 4 detik

;--------------
; Program Reset
;--------------

      ORG   0000h
      LJMP  Start

      ORG   0003h        ; vector address untuk interrupt 0
      LJMP  Int_0

      ORG   000Bh        ; vector address untuk timer 0
      LJMP  Timer_0

      ORG   001Bh        ; vector address untuk timer 1
      LJMP  Timer_1

;-------------
; ROM Database
;-------------

; ini adalah data karakter-karakter yang akan ditampilkan pada LCD
; untuk tiap-tiap mode

Header
      DB    149
      DB    '                ALAT PEMANTAU DAN PENGENDALI SUHU A'
      DB    'IR TANPA KABEL BERBASIS uC89C51 - Hartono Rahardjo'
      DB    ' - NRP. 5103094049 - Unika WIDYA MANDALA Surabaya '
      DB    '                '

Opened
      DB    'buka '
Closed
      DB    'tutup'
```

```
Y_or_N
        DB      '*=Y #=N'
Active
        DB      'aktif'
Stop
        DB      'stop '
Full
        DB      'penuh '
Not_Full
        DB      'terisi'
Empty
        DB      'kosong'

Status_1_Text
        DB      'PV = '
        DB      'SP = '

Status_2_Text
        DB      'Kran isi  :'
        DB      'Kran buang:'

Status_3_Text
        DB      'SP (',0DFh,'C) = '

Status_4_Text
        DB      'Buka kran isi ? '

Status_5_Text
        DB      'Tutup kran isi ?'

Status_6_Text
        DB      'Buka kran buang?'

Status_7_Text
        DB      'Ttp kran buang? '

Status_8_Text
        DB      'SP > 100 !!!'
        DB      'Tekan #'

Status_9_Text
        DB      'Vol. air: '
        DB      'Heater  : '

Status_10_Text
        DB      'Air sudah penuh.'
        DB      'Tekan #    '

;---------------------------
; Interrupt Service Routine
;---------------------------

; Interrupt timer 0 digunakan untuk :
; 1. menghitung pewaktuan 0.5 detik, setiap 0.5 dtk tampilan pada header
bergeser
; 2. menghitung pewaktuan 4 detik, kalau tidak ada data yg diterima maka
tampilkan
```

```
     tulisan --- pada LCD

Timer_0
       PUSH  a
       PUSH  psw
       MOV   th0,#03Ch
       MOV   tl0,#0AFh
       INC   Sec_Tick
       MOV   a,Timer_Status
       CJNE  a,#0,T0_J2
       MOV   a,Sec_Tick
       CJNE  a,#10,T0_J1
       MOV   Sec_Tick,#0
       SETB  Header_F
       AJMP  T0_J1

T0_J3  JNC   T0_J4
       AJMP  T0_J1

T0_J2  MOV   a,Sec_Tick
       CJNE  a,#60,T0_J3
T0_J4  MOV   Sec_Tick,#0
       MOV   Present_Value,#0FFh
       SETB  No_Data_F
       SETB  Update_Mode_F
;      CLR   tr0
;      CLR   et0
T0_J1  POP   psw
       POP   a
       RETI

; Interrupt 0 digunakan untuk menerima dan menghitung pulsa data
; yang diterima dari receiver IR

Int_0
       CLR   ea
       CLR   et0
       PUSH  a
       PUSH  psw
       MOV   Data_Counter,#0
       MOV   th0,#0
       MOV   tl0,#0
       SETB  tr0
       JNB   IR_RX,$
       CLR   tr0
       MOV   a,th0
       CJNE  a,#7,I0_J2
       CLR   Data_Type_F
       AJMP  I0_J5
I0_J2  CJNE  a,#9,I0_J1
       SETB  Data_Type_F
I0_J5  MOV   th0,#0E0h
       MOV   tl0,#0
       CLR   tf0
       SETB  tr0
I0_J3  JB    tf0,I0_J4
       JB    IR_RX,I0_J3
```

```
        JNB    IR_RX,$
        INC    Data_Counter
        AJMP   IO_J5

IO_J4   DEC    Data_Counter
        MOV    a,Mode
        CJNE   a,#1,IO_J7
IO_J8   SETB   Update_Mode_F
        AJMP   IO_J9
IO_J7   CJNE   a,#2,IO_J10 ; cek apakah data yg masuk = PV ?
        AJMP   IO_J8
IO_J10         CJNE  a,#9,IO_J9  ; cek apakah data yg masuk = status kontrol ?
        AJMP   IO_J8

IO_J9   CLR    tf0
        CLR    tr0
        JB     Data_Type_F,IO_J6
        MOV    Present_Value,Data_Counter
        AJMP   IO_J11

IO_J6   MOV    Ctrl_Status,Data_Counter

IO_J11         CLR   No_Data_F
        MOV    th0,#03Ch
        MOV    tl0,#0AFh
        MOV    Sec_Tick,#0

IO_J1
        SETB   et0
        SETB   tr0
        CLR    ie0
        POP    psw
        POP    a
        SETB   ea
        RETI

; timer 1 digunakan untuk membangkitkan frekuensi 40 kHz (carrier)

Timer_1
        CPL    IR_TX
        RETI

;-----------
; Procedures
;-----------

; digunakan untuk menghasilkan delay kurang lebih 50 us (digunakan untuk
; penulisan data pada LCD)

Delay_50
        PUSH   7
        MOV    r7,#50              ; Delay 50 us
        DJNZ   r7,$
        POP    7
        RET

; digunakan untuk menghasilkan delay kurang lebih 4 ms (digunakan untuk
```

```
; penulisan instruksi pada LCD)

Delay_2
      PUSH  7
      PUSH  6
      MOV   r7,#0
D_2_J1      MOV   r6,#0Eh
      DJNZ  r6,$
      DJNZ  r7,D_2_J1
      POP   6
      POP   7
      RET

; prosedur penulisan instruksi pada LCD

LCD_Write_Inst
      CLR   LCD_RS
      SETB  LCD_CS
      MOV   p1,a
      CLR   LCD_CS
      LCALL       Delay_2
      RET

; prosedur penulisan data pada LCD

LCD_Write_Data
      SETB  LCD_RS
      SETB  LCD_CS
      MOV   p1,a
      CLR   LCD_CS
      LCALL Delay_50
      RET

; prosedur inisialisasi LCD

Initialize_LCD
      MOV   r7,#5
I_L_J1      LCALL Delay_2
      DJNZ  r7,I_L_J1
      MOV   a,#03Fh
      LCALL LCD_Write_Inst
      LCALL LCD_Write_Inst
      LCALL LCD_Write_Inst
      MOV   a,#0Eh
      LCALL LCD_Write_Inst
      MOV   a,#06h
      LCALL LCD_Write_Inst
      MOV   a,#01h
      LCALL LCD_Write_Inst
      MOV   a,#0Ch
      LCALL LCD_Write_Inst
      RET

; Ini adalah prosedur untuk setting timer, interrupt, dan nilai awal variabel

Initialize_Data
      MOV   tmod,#21h   ; timer 0 -> timer 16 bit, timer 1 -> timer auto reload
```

```
      MOV    th0,#03Ch   ; timer 0 digunakan utk pewaktuan 50.000 us
      MOV    tl0,#0AFh   ;

      MOV    th1,#0F4h   ; timer 1 digunakan utk pewaktuan 25 us (periode dari 40
kHz)
      MOV    tl1,#0F4h   ;

      MOV    ie,#82h             ; aktifkan int. timer 0

      CLR    Button_F
      SETB   Header_F
      SETB   Show_Header_F
      SETB   No_Data_F
      MOV    X_Header,#0
      MOV    Sec_Tick,#0
      MOV    Timer_Status,#0
      MOV    Set_Point,#0FFh
      MOV    Present_Value,#0FFh
      MOV    Buffer_SP,#0
      MOV    Buffer_SP+1,#0
      MOV    Buffer_SP+2,#0
      CLR    Upper_Valve
      CLR    Lower_Valve
      CLR    Heater
      SETB   IR_TX
      MOV    Tank_Status,#0

      MOV    dptr,#Header
      CLR    a
      MOVC   a,@a+dptr
      MOV    J_Header,a
      SETB   tr0
      RET

; prosedur untuk menampilkan tulisan header pada LCD

Show_Header
      JNB    Header_F,H_J1
      CLR    Header_F
      MOV    a,#080h
      LCALL  LCD_Write_Inst
      MOV    dptr,#Header
      INC    dptr
      MOV    r7,#16
H_J2
      MOV    a,X_Header
      MOVC   a,@a+dptr
      LCALL  LCD_Write_Data
      INC    dptr
      DJNZ   r7,H_J2
      INC    X_Header
      MOV    a,X_Header
      CJNE   a,J_Header,H_J1
      MOV    X_Header,#0
H_J1  RET
```

```
; prosedur delay untuk menghilangkan bouncing saat tombol ditekan

Remove_Bouncing
       MOV    r4,#0FFh
RB_J1  MOV    r3,#0FFh
       DJNZ   r3,$
       DJNZ   r4,RB_J1
       RET

; prosedur pengecekan tombol

Check_Button
       MOV    r7,#1
       CLR    Scan_Key_1
       SETB   Scan_Key_2
       SETB   Scan_Key_3
       SETB   Scan_Key_4
       MOV    a,p2
       ANL    a,#7h
       CJNE   a,#7h,CB_J2
       MOV    r7,#4
       SETB   Scan_Key_1
       CLR    Scan_Key_2
       SETB   Scan_Key_3
       SETB   Scan_Key_4
       MOV    a,p2
       ANL    a,#7h
       CJNE   a,#7h,CB_J2
       MOV    r7,#7
       SETB   Scan_Key_1
       SETB   Scan_Key_2
       CLR    Scan_Key_3
       SETB   Scan_Key_4
       MOV    a,p2
       ANL    a,#7h
       CJNE   a,#7h,CB_J2
       MOV    r7,#10
       SETB   Scan_Key_1
       SETB   Scan_Key_2
       SETB   Scan_Key_3
       CLR    Scan_Key_4
       MOV    a,p2
       ANL    a,#7h
       CJNE   a,#7h,CB_J2
       CLR    Button_F
CB_J1  RET

CB_J2  JB     Button_F,CB_J1
       SETB   Button_F
       LCALL  Remove_Bouncing
       JNB    Show_Header_F,CB_J3
       MOV    ie,#089h
       SETB   it0
       MOV    Mode,#1
       SETB   Update_Mode_F
       CLR    Show_Header_F
       CLR    tr0
```

```
        MOV    Timer_Status,#1
        CLR    Header_F
        RET
CB_J3   CJNE   a,#3,CB_J4
        MOV    a,#0
        AJMP   CB_J6
CB_J4   CJNE   a,#5,CB_J5
        MOV    a,#1
        AJMP   CB_J6
CB_J5   CJNE   a,#6,CB_J1
        MOV    a,#2
CB_J6   MOV    b,r7
        ADD    a,b

; Button 1

        CJNE   a,#1,CB_J7
        MOV    a,Mode
        CJNE   a,#3,Btn1_J1
        MOV    a,X_Enter_SP
        CJNE   a,#3,Btn1_J2
        RET
Btn1_J2        MOV    r0,#Buffer_SP
        ADD    a,r0
        MOV    r0,a
        MOV    @r0,#1
        MOV    a,#31h
        LCALL  LCD_Write_Data
        INC    X_Enter_SP
Btn1_J1        RET

; Button 2

CB_J7   CJNE   a,#2,CB_J8
        MOV    a,Mode
        CJNE   a,#3,Btn2_J1
        MOV    a,X_Enter_SP
        CJNE   a,#3,Btn2_J2
        RET
Btn2_J2        MOV    r0,#Buffer_SP
        ADD    a,r0
        MOV    r0,a
        MOV    @r0,#2
        MOV    a,#32h
        LCALL  LCD_Write_Data
        INC    X_Enter_SP
Btn2_J1        RET

; Button 3

CB_J8   CJNE   a,#3,CB_J9
        MOV    a,Mode
        CJNE   a,#3,Btn3_J1
        MOV    a,X_Enter_SP
        CJNE   a,#3,Btn3_J2
        RET
Btn3_J2        MOV    r0,#Buffer_SP
```

```
        ADD   a,r0
        MOV   r0,a
        MOV   @r0,#3
        MOV   a,#33h
        LCALL LCD_Write_Data
        INC   X_Enter_SP
Btn3_J1       RET

; Button 4

CB_J9   CJNE  a,#4,CB_J10
        MOV   a,Mode
        CJNE  a,#3,Btn4_J1
        MOV   a,X_Enter_SP
        CJNE  a,#3,Btn4_J2
        RET
Btn4_J2       MOV    r0,#Buffer_SP
        ADD   a,r0
        MOV   r0,a
        MOV   @r0,#4
        MOV   a,#34h
        LCALL LCD_Write_Data
        INC   X_Enter_SP
Btn4_J1       RET

; Button 5

CB_J10        CJNE  a,#5,CB_J11
        MOV   a,Mode
        CJNE  a,#3,Btn5_J1
        MOV   a,X_Enter_SP
        CJNE  a,#3,Btn5_J2
        RET
Btn5_J2       MOV    r0,#Buffer_SP
        ADD   a,r0
        MOV   r0,a
        MOV   @r0,#5
        MOV   a,#35h
        LCALL LCD_Write_Data
        INC   X_Enter_SP
Btn5_J1       RET

; Button 6

CB_J11        CJNE  a,#6,CB_J12
        MOV   a,Mode
        CJNE  a,#3,Btn6_J1
        MOV   a,X_Enter_SP
        CJNE  a,#3,Btn6_J2
        RET
Btn6_J2       MOV    r0,#Buffer_SP
        ADD   a,r0
        MOV   r0,a
        MOV   @r0,#6
        MOV   a,#36h
        LCALL LCD_Write_Data
        INC   X_Enter_SP
```

```
Btn6_J1      RET

; Button 7

CB_J12       CJNE  a,#7,CB_J13
      MOV    a,Mode
      CJNE   a,#3,Btn7_J1
      MOV    a,X_Enter_SP
      CJNE   a,#3,Btn7_J2
      RET
Btn7_J2      MOV   r0,#Buffer_SP
      ADD    a,r0
      MOV    r0,a
      MOV    @r0,#7
      MOV    a,#37h
      LCALL  LCD_Write_Data
      INC    X_Enter_SP
Btn7_J1      RET

; Button 8

CB_J13       CJNE  a,#8,CB_J14
      MOV    a,Mode
      CJNE   a,#3,Btn8_J1
      MOV    a,X_Enter_SP
      CJNE   a,#3,Btn8_J2
      RET
Btn8_J2      MOV   r0,#Buffer_SP
      ADD    a,r0
      MOV    r0,a
      MOV    @r0,#8
      MOV    a,#38h
      LCALL  LCD_Write_Data
      INC    X_Enter_SP
Btn8_J1      RET

; Button 9

CB_J14       CJNE  a,#9,CB_J15
      MOV    a,Mode
      CJNE   a,#3,Btn9_J1
      MOV    a,X_Enter_SP
      CJNE   a,#3,Btn9_J2
      RET
Btn9_J2      MOV   r0,#Buffer_SP
      ADD    a,r0
      MOV    r0,a
      MOV    @r0,#9
      MOV    a,#39h
      LCALL  LCD_Write_Data
      INC    X_Enter_SP
Btn9_J1      RET


CB_J19       LJMP  CB_J16

; Button 10
```

```
CB_J15      CJNE  a,#10,CB_J19
       MOV   a,Mode
       CJNE  a,#1,Bt10_J1
       MOV   Mode,#2
       SETB  Update_Mode_F
       RET
Bt10_J1     CJNE  a,#2,Bt10_J2
       MOV   Mode,#9
       SETB  Update_Mode_F
       RET
Bt10_J2     CJNE  a,#3,Bt10_J3
       MOV   a,X_Enter_SP
       CJNE  a,#0,Bt10_J4
       RET
Bt10_J4     MOV   a,#10h
       LCALL LCD_Write_Inst
       MOV   a,#20h
       LCALL LCD_Write_Data
       MOV   a,#10h
       LCALL LCD_Write_Inst
       DEC   X_Enter_SP
       RET
Bt10_J3     CJNE  a,#4,Bt10_J5
       MOV   a,Tank_Status
       CJNE  a,#3,B10_J10
       MOV   Mode,#10
       SETB  Update_Mode_F
       RET

B10_J10     SETB  Upper_Valve_C

       LCALL Turn_Upper_Valve
       SETB  Send_Data_F
       LCALL Send_Data

       MOV   Mode,#2
       SETB  Update_Mode_F
       RET
Bt10_J5     CJNE  a,#5,Bt10_J6
       CLR   Upper_Valve_C

       LCALL Turn_Upper_Valve
       SETB  Send_Data_F
       LCALL Send_Data

       MOV   Mode,#2
       SETB  Update_Mode_F
       RET
Bt10_J6     CJNE  a,#6,Bt10_J7
       SETB  Lower_Valve_C

       LCALL Turn_Lower_Valve
       SETB  Send_Data_F
       LCALL Send_Data

       MOV   Mode,#2
```

```
        SETB  Update_Mode_F
        RET
Bt10_J7       CJNE  a,#7,Bt10_J8
        CLR   Lower_Valve_C

        LCALL Turn_Lower_Valve
        SETB  Send_Data_F
        LCALL Send_Data

        MOV   Mode,#2
        SETB  Update_Mode_F
        RET
Bt10_J8       CJNE  a,#9,Bt10_J9
        MOV   Mode,#1
        SETB  Update_Mode_F
        RET
Bt10_J9
        RET

; Button 11

CB_J16        CJNE  a,#11,CB_J17
        MOV   a,Mode
        CJNE  a,#3,Bt11_J1
        MOV   a,X_Enter_SP
        CJNE  a,#3,Bt11_J2
        RET
Bt11_J2       MOV   r0,#Buffer_SP
        ADD   a,r0
        MOV   r0,a
        MOV   @r0,#0
        MOV   a,#30h
        LCALL LCD_Write_Data
        INC   X_Enter_SP
        RET
Bt11_J1       CJNE  a,#2,Bt11_J3
        JNB   No_Data_F,Bt11_J5
        RET
Bt11_J5       MOV   Mode,#4
        SETB  Update_Mode_F
        JNB   Upper_Valve,Bt11_J4
        MOV   Mode,#5
Bt11_J4       RET

Bt11_J3
        RET

; Button 12

CB_J17        CJNE  a,#12,CB_J18
        MOV   a,Mode
        CJNE  a,#1,Bt12_J1
        JNB   No_Data_F,B12_J16
        RET
B12_J16       MOV   Mode,#3
        SETB  Update_Mode_F
        RET
```

```
Bt12_J1     CJNE  a,#3,Bt12_J2
      LCALL Calculate_SP
      MOV   a,#0Ch
      LCALL LCD_Write_Inst
      MOV   a,r6
      CJNE  a,#100,Bt12_J3
      AJMP  Bt12_J4
Bt12_J3     JC    Bt12_J4
      CJNE  a,#0FFh,Bt12_J7
      AJMP  Bt12_J6
Bt12_J7     MOV   Mode,#8
      SETB  Update_Mode_F
      RET
Bt12_J4     MOV   Set_Point,r6

      CLR   Send_Data_F
      LCALL Send_Data

Bt12_J6     MOV   Mode,#1
      SETB  Update_Mode_F
      RET

Bt12_J2     CJNE  a,#8,Bt12_J5
      AJMP  Bt12_J6

Bt12_J5     CJNE  a,#2,Bt12_J8
      JNB   No_Data_F,B12_J17
      RET
B12_J17     MOV   Mode,#6
      SETB  Update_Mode_F
      JNB   Lower_Valve,Bt12_J9
      MOV   Mode,#7
Bt12_J9     RET

Bt12_J8     CJNE  a,#4,B12_J10
B12_J14     MOV   Mode,#2
      SETB  Update_Mode_F
      RET
B12_J10     CJNE  a,#5,B12_J11
      AJMP  B12_J14
B12_J11     CJNE  a,#6,B12_J12
      AJMP  B12_J14
B12_J12     CJNE  a,#7,B12_J13
      AJMP  B12_J14
B12_J13     CJNE  a,#10,B12_J15
      AJMP  B12_J14
B12_J15
      RET

CB_J18      RET

; prosedur untuk menghitung SP dalam hexadesimal dari nilai SP
; yang diinputkan melalui keypad

Calculate_SP
      MOV   r6,#0
```

```
MOV    r7,X_Enter_SP
MOV    r0,#Buffer_SP
MOV    a,r7
CJNE   a,#0,CSP_J3
MOV    r6,Set_Point
```

```
        MOV    a,b
        ADD    a,#30h
        LCALL LCD_Write_Data
CHD_J2       MOV    a,#020h
        LCALL LCD_Write_Data
        MOV    a,#0DFh
        LCALL LCD_Write_Data
        MOV    a,#043h
        LCALL LCD_Write_Data
        RET

Mode_4_to_7
        MOV    r7,#16
Md47_J1      CLR    a
        MOVC   a,@a+dptr
        LCALL LCD_Write_Data
        INC    dptr
        DJNZ   r7,Md47_J1
        MOV    dptr,#Y_or_N
        MOV    a,#0C0h
        LCALL LCD_Write_Inst
        MOV    r7,#7
Md47_J2      CLR    a
        MOVC   a,@a+dptr
        LCALL LCD_Write_Data
        INC    dptr
        DJNZ   r7,Md47_J2
        RET

; prosedur untuk menampilkan tulisan tulisan untuk setiap mode pada LCD

Update_Mode
        JB     Update_Mode_F,UM_J1
        RET
UM_J1   CLR    Update_Mode_F
        MOV    a,#1
        LCALL LCD_Write_Inst
        MOV    a,Mode

; Mode 1

        CJNE   a,#1,UM_J2
        MOV    dptr,#Status_1_Text
        MOV    r7,#5
Md1_J1       CLR    a
        MOVC   a,@a+dptr
        LCALL LCD_Write_Data
        INC    dptr
        DJNZ   r7,Md1_J1
        MOV    a,Present_Value
        LCALL Calculate_Hex_2_Dec
        MOV    a,#0C0h
        LCALL LCD_Write_Inst
        MOV    r7,#5
Md1_J2       CLR    a
        MOVC   a,@a+dptr
        LCALL LCD_Write_Data
```

```
        INC    dptr
        DJNZ   r7,Md1_J2
        MOV    a,Set_Point
        LCALL  Calculate_Hex_2_Dec
        RET

; Mode 2

UM_J2   CJNE   a,#2,UM_J3
        LCALL  Check_Ctrl_Status
        MOV    dptr,#Status_2_Text
        MOV    r7,#11
Md2_J1         CLR    a
        MOVC   a,@a+dptr
        LCALL  LCD_Write_Data
        INC    dptr
        DJNZ   r7,Md2_J1
        PUSH   dpl
        PUSH   dph
        JNB    No_Data_F,Md2_J7
        MOV    a,#020h
        LCALL  LCD_Write_Data
        MOV    a,#02Dh
        LCALL  LCD_Write_Data
        MOV    a,#02Dh
        LCALL  LCD_Write_Data
        MOV    a,#02Dh
        LCALL  LCD_Write_Data
        AJMP   Md2_J8

Md2_J7         MOV    dptr,#Closed
        JNB    Upper_Valve,Md2_J3
        MOV    dptr,#Opened
Md2_J3         MOV    r7,#5
Md2_J4         CLR    a
        MOVC   a,@a+dptr
        LCALL  LCD_Write_Data
        INC    dptr
        DJNZ   r7,Md2_J4

Md2_J8         POP    dph
        POP    dpl
        MOV    a,#0C0h
        LCALL  LCD_Write_Inst
        MOV    r7,#11
Md2_J2         CLR    a
        MOVC   a,@a+dptr
        LCALL  LCD_Write_Data
        INC    dptr
        DJNZ   r7,Md2_J2
        JNB    No_Data_F,Md2_J9
        MOV    a,#020h
        LCALL  LCD_Write_Data
        MOV    a,#02Dh
        LCALL  LCD_Write_Data
        MOV    a,#02Dh
        LCALL  LCD_Write_Data
```

```
      MOV   a,#02Dh
      LCALL LCD_Write_Data
      RET

Md2_J9      MOV   dptr,#Closed
      JNB   Lower_Valve,Md2_J5
      MOV   dptr,#Opened
Md2_J5      MOV   r7,#5
Md2_J6      CLR   a
      MOVC  a,@a+dptr
      LCALL LCD_Write_Data
      INC   dptr
      DJNZ  r7,Md2_J6
      RET

; Mode 3

UM_J3 CJNE  a,#3,UM_J4
      MOV   dptr,#Status_3_Text
      MOV   r7,#10
Md3_J1      CLR   a
      MOVC  a,@a+dptr
      LCALL LCD_Write_Data
      INC   dptr
      DJNZ  r7,Md3_J1
      MOV   a,#0Eh
      LCALL LCD_Write_Inst
      MOV   X_Enter_SP,#0
      RET

; Mode 4

UM_J4 CJNE  a,#4,UM_J5
      MOV   dptr,#Status_4_Text
      LCALL Mode_4_to_7
      RET

; Mode 5

UM_J5 CJNE  a,#5,UM_J6
      MOV   dptr,#Status_5_Text
      LCALL Mode_4_to_7
      RET

; Mode 6

UM_J6 CJNE  a,#6,UM_J7
      MOV   dptr,#Status_6_Text
      LCALL Mode_4_to_7
      RET

; Mode 7

UM_J7 CJNE  a,#7,UM_J8
      MOV   dptr,#Status_7_Text
      LCALL Mode_4_to_7
      RET
```

```
; Mode 8

UM_J8 CJNE  a,#8,UM_J9
      MOV   r7,#12
      MOV   dptr,#Status_8_Text
Md8_J1      CLR   a
      MOVC  a,@a+dptr
      LCALL LCD_Write_Data
      INC   dptr
      DJNZ  r7,Md8_J1
      MOV   a,#0C0h
      LCALL LCD_Write_Inst
      MOV   r7,#7
Md8_J2      CLR   a
      MOVC  a,@a+dptr
      LCALL LCD_Write_Data
      INC   dptr
      DJNZ  r7,Md8_J2
      RET

UM_J9 CJNE  a,#9,UM_J10
      LCALL Check_Ctrl_Status
      MOV   r7,#10
      MOV   dptr,#Status_9_Text
Md9_J1      CLR   a
      MOVC  a,@a+dptr
      LCALL LCD_Write_Data
      INC   dptr
      DJNZ  r7,Md9_J1
      PUSH  dpl
      PUSH  dph
      JNB   No_Data_F,Md9_J8
      MOV   a,#02Dh
      LCALL LCD_Write_Data
      MOV   a,#02Dh
      LCALL LCD_Write_Data
      MOV   a,#02Dh
      LCALL LCD_Write_Data
      AJMP  Md9_J9

Md9_J8      MOV   dptr,#Full
      MOV   a,Tank_Status
      CJNE  a,#0,Md9_J3
      MOV   dptr,#Empty
      AJMP  Md9_J4
Md9_J3      CJNE  a,#1,Md9_J4
      MOV   dptr,#Not_Full
Md9_J4      MOV   r7,#6
Md9_J5      CLR   a
      MOVC  a,@a+dptr
      LCALL LCD_Write_Data
      INC   dptr
      DJNZ  r7,Md9_J5

Md9_J9      POP   dph
      POP   dpl
```

```
        MOV   a,#0C0h
        LCALL LCD_Write_Inst
        MOV   r7,#10
Md9_J2        CLR   a
        MOVC  a,@a+dptr
        LCALL LCD_Write_Data
        INC   dptr
        DJNZ  r7,Md9_J2
        JNB   No_Data_F,Md9_J10
        MOV   a,#02Dh
        LCALL LCD_Write_Data
        MOV   a,#02Dh
        LCALL LCD_Write_Data
        MOV   a,#02Dh
        LCALL LCD_Write_Data
        RET

Md9_J10       MOV   dptr,#Active
        JB    Heater,Md9_J6
        MOV   dptr,#Stop
Md9_J6        MOV   r7,#5
Md9_J7        CLR   a
        MOVC  a,@a+dptr
        LCALL LCD_Write_Data
        INC   dptr
        DJNZ  r7,Md9_J7
        RET

UM_J10        CJNE  a,#10,UM_J11
        MOV   r7,#16
        MOV   dptr,#Status_10_Text
Md10_J1       CLR   a
        MOVC  a,@a+dptr
        LCALL LCD_Write_Data
        INC   dptr
        DJNZ  r7,Md10_J1
        MOV   a,#0C0h
        LCALL LCD_Write_Inst
        MOV   r7,#7
Md10_J2       CLR   a
        MOVC  a,@a+dptr
        LCALL LCD_Write_Data
        INC   dptr
        DJNZ  r7,Md10_J2
        RET
UM_J11
        RET

; prosedur untuk mengirimkan data pada kontroler 1

Send_Data
        CLR   ex0
        CLR   et0
        SETB  et1
        MOV   r7,#2              ; !!!

SD_J4 JB      Send_Data_F,SD_J1
```

```
        MOV    Counter,Set_Point
        MOV    th0,#0F5h
        MOV    tl0,#041h
        SETB   tr0
        SETB   tr1
        JNB    tf0,$
        CLR    tr1
        SETB   IR_TX
        LJMP   SD_J2

SD_J1   MOV    Counter,Set_Ctrl_St
        MOV    th0,#0F3h
        MOV    tl0,#07Fh
        SETB   tr0
        SETB   tr1
        JNB    tf0,$
        CLR    tr1
        SETB   IR_TX

SD_J2   CLR    tr0
        CLR    tf0
        INC    Counter
SD_J3   MOV    th0,#0FDh
        MOV    tl0,#0A7h
        SETB   tr0
        JNB    tf0,$
        CLR    tf0
        MOV    th0,#0FDh
        MOV    tl0,#0A7h
        SETB   tr1
        JNB    tf0,$
        CLR    tr0
        CLR    tr1
        CLR    tf0
        DJNZ   Counter,SD_J3
        MOV    th0,#0C0h              ; !!!
        MOV    tl0,#000h
        SETB   tr0
        JNB    tf0,$
        CLR    tr0
        CLR    tf0
        DJNZ   r7,SD_J4

        CLR    et1
        CLR    ie0
        SETB   ex0
        RET

; prosedur untuk meng update nilai kontrol status yg akan dikirimkan
; (membuka / menutup kran isi)

Turn_Upper_Valve
        MOV    Set_Ctrl_St,Ctrl_Status
        ANL    Set_Ctrl_St,#3
        JB     Upper_Valve_C,TUV_J1
        ANL    Set_Ctrl_St,#0FEh
        RET
```

```
TUV_J1      ORL   Set_Ctrl_St,#1
      RET

; prosedur untuk meng update nilai kontrol status yg akan dikirimkan
; (membuka / menutup kran buang)

Turn_Lower_Valve
      MOV   Set_Ctrl_St,Ctrl_Status
      ANL   Set_Ctrl_St,#3
      JB    Lower_Valve_C,TLV_J1
      ANL   Set_Ctrl_St,#0FDh
      RET
TLV_J1      ORL   Set_Ctrl_St,#2
      RET

; prosedur untuk pembacaan nilai data kontrol status yang diterima dari
; kontroler 1, untuk ditampilkan pada LCD

Check_Ctrl_Status
      MOV   a,Ctrl_Status
      ANL   a,#1
      CLR   Upper_Valve
      CJNE  a,#1,CCS_J1
      SETB  Upper_Valve
CCS_J1      MOV   a,Ctrl_Status
      ANL   a,#2
      CLR   Lower_Valve
      CJNE  a,#2,CCS_J2
      SETB  Lower_Valve
CCS_J2      MOV   a,Ctrl_Status
      ANL   a,#0Ch
      RR    a
      RR    a
      MOV   Tank_Status,a
      CJNE  a,#0,CCS_J4
      MOV   Set_Point,#0FFh
CCS_J4      MOV   a,Ctrl_Status
      ANL   a,#10h
      CLR   Heater
      MOV   Set_Point,#0FFh
      CJNE  a,#10h,CCS_J3
      SETB  Heater
CCS_J3
      RET

;-------------
; Main Program
;-------------

Start
      MOV   sp,#7
      LCALL Initialize_LCD
      LCALL Initialize_Data

Loop
      LCALL Show_Header
      LCALL Check_Button
```

```
LCALL Update_Mode
LJMP  Loop
```

```
;----------
; Constants
;----------

;------------------
; Memory Allocation
;------------------

Num_Lo              EQU   30h
Num_Hi              EQU   31h
Div_0       EQU   32h
Div_1       EQU   33h
Div_2       EQU   34h
Div_3       EQU   35h
Tmp_0       EQU   36h
Tmp_1       EQU   37h    ; Num_Lo s/d Tmp_3 adalah variabel
Tmp_2       EQU   38h    ; untuk perhitungan aritmatika
Tmp_3       EQU   39h    ;

Present_Value       EQU   3Ah   ; variabel utk menyimpan nilai PV (suhu sekarang)
Sec_Tick    EQU   3Bh    ; variabel utk counter timer

Ctrl_Status EQU   3Ch    ; 0000 0000b
                         ;     ³ ³³³ \
                         ;     ' +Ù³ Upper valve : 0 -> close, 1 -> open
                         ;     ³  ³ Lower Valve : 0 -> close, 1 -> open
                         ;     ³ Water level : 00 -> kosong, 01 -> terisi, 11 ->
penuh
                         ;    Heater status : 0 -> stop, 1 -> aktif

Timer_Reg   EQU   3Dh    ; variabel counter utk menghitung jml pulsa data yang
akan dikirim
Tank_Status EQU   3Eh    ; Status level air : 0 -> kosong, 1 -> terisi, 2 ->
penuh
Dummy       EQU   3Fh    ; variabel penampung sementara, serba guna
Set_Point   EQU   40h    ; variabel utk menyimpan nilai set point dari kontroler
2
Data_Counter        EQU   41h   ; variabel counter utk menghitung jml pulsa data
yang diterima dari kontroler 2
Dummy_2             EQU   42h   ; variabel penampung sementara, serba guna

;----------------
; Bit Addressable
;----------------

SOC         BIT   p3.1  ; pin pengontrol ADC start konversi: 0 -> reset, 1 ->
start konversi
EOC         BIT   p3.2  ; pin flag/indikator dari ADC bahwa ADC telah selesai
mengkonversi: 1 -> belum selesai, 0 -> sudah selesai
IR_RX       BIT   p3.3  ; pin input dari receiver infrared: 0 -> ada data, 1 ->
no data
IR_TX       BIT   p2.4  ; pin output untuk transmitter infrared: 0 -> on, 1 ->
off
Heater              BIT   p2.5  ; pin output relay heater: 0 -> off, 1 -> on

U_Valve_1   BIT   p2.0  ; pin output driver motor utk kran isi (#1)
U_Valve_2   BIT   p2.1  ; pin output driver motor utk kran isi (#2)
```

```
                          ; #1 = 1, #2 = 1 : stop motor
                          ; #1 = 0, #2 = 1 : motor putar ke kiri
                          ; #1 = 1, #2 = 0 : motor putar ke kanan

L_Valve_1    BIT    p2.2  ; pin output driver motor utk kran buang (#1)
L_Valve_2    BIT    p2.3  ; pin output driver motor utk kran buang (#2)
                          ; #1 = 1, #2 = 1 : stop motor
                          ; #1 = 0, #2 = 1 : motor putar ke kiri
                          ; #1 = 1, #2 = 0 : motor putar ke kanan

U_Level             BIT    p3.4  ; pin input dari sensor level air (atas): 0 -> tdk
ada air, 1 -> ada air
L_Level             BIT    p3.5  ; pin input dari sensor level air (bawah): 0 ->
tdk ada air, 1 -> ada air

;-----------------
; Flag / Indicator
;-----------------

Send_Data_F BIT    00h    ; 0 -> idle,    1 -> kirim data
Read_ADC_F  BIT    01h    ; 0 -> idle,    1 -> baca ADC
Upper_Valve BIT    03h    ; 0 -> close,   1 -> open
Lower_Valve BIT    04h    ; 0 -> close,   1 -> open
Heater_Status      BIT    05h    ; 0 -> stop,    1 -> active
Heater_F    BIT    06h    ; 0 -> idle,    1 -> kontroler heater aktif
Data_Type_F BIT    07h    ; 0 -> data SP, 1 -> data status kontrol
Check_Ctrl_F       BIT    08h    ; 0 -> idle,      1 -> cek kontrol

;--------------
; Program Reset
;--------------

      ORG    0000h
      LJMP   Start

      ORG    000Bh        ; vector address untuk timer 0
      LJMP   Timer_0

      ORG    0013h        ; vector address untuk interrupt 1
      LJMP   Int_1

      ORG    001Bh        ; vector address untuk timer 1
      LJMP   Timer_1

;--------------------------
; Interrupt Service Routine
;--------------------------

; Timer 0 digunakan untuk menghitung 0.5 detik.
; Tiap 0.5 detik kontroler mengirim data PV, 0.5 detik berikutnya
; kontroler mengirim data status kontrol (heater,water level,status kran),
; 0.5 detik kemudian mengirim data PV lagi, dan seterusnya.

Timer_0
      PUSH   a
      PUSH   psw
      MOV    th0,#03Ch    ; nilai th0 dan tl0 ini akan menghasilkan
```

```
        MOV    tl0,#0AFh    ; penghitungan waktu utk 50.000 us

        SETB   Read_ADC_F   ; pengkonversian / pembacaan ADC diaktifkan
                            ; setiap 50.000 us

        INC    Sec_Tick     ; counter untuk 50.000 us

        MOV    a,Sec_Tick   ; apakah sudah terjadi penghitungan waktu
        CJNE   a,#10,T0_J1  ; sebanyak 10 x 50.000 us = 500.000 us =
                            ; 500 ms = 0.5 dtk ?

        SETB   Heater_F     ; lakukan pengecekan / pengontrolan heater

        CLR    ex1

        MOV    Sec_Tick,#0
        CLR    et0

        CPL    Send_Data_F
        JB     Send_Data_F,T0_J2

        MOV    Timer_Reg,Present_Value
        MOV    th0,#0F9h            ; timer 0 digunakan utk menghasilkan
        MOV    tl0,#0BDh            ; pewaktuan 1100 us (header data PV)
        SETB   tr1                  ; timer 1 diaktifkan
        JNB    tf0,$
        CLR    tr1
        SETB   IR_TX
        AJMP   T0_J3

T0_J2   MOV    Timer_Reg,Ctrl_Status
        MOV    th0,#0F7h            ; timer 0 digunakan utk menghasilkan
        MOV    tl0,#067h            ; pewaktuan 1650 us (header data status kontrol)
        SETB   tr1                  ; timer 1 diaktifkan
        JNB    tf0,$
        CLR    tr1
        SETB   IR_TX
T0_J3   CLR    tr0
        CLR    tf0
        INC    Timer_Reg
T0_J4   MOV    th0,#0FDh            ; timer 0 digunakan utk menghasilkan
        MOV    tl0,#0A7h            ; pewaktuan 600 us (jedah utk tiap data)
        SETB   tr0
        JNB    tf0,$
        CLR    tf0
        MOV    th0,#0FDh            ; timer 0 digunakan utk menghasilkan
        MOV    tl0,#0A7h            ; pewaktuan 600 us (lebar 1 pulsa data)
        SETB   tr1
        JNB    tf0,$
        CLR    tr0
        CLR    tr1
        CLR    tf0
        DJNZ   Timer_Reg,T0_J4
        MOV    th0,#03Ch
        MOV    tl0,#0AFh
        SETB   tr0
        SETB   et0
```

```
T0_J1 POP   psw
      POP   a

;     CLR   ie1

      SETB  ex1
      RETI

; interrupt 1 digunakan untuk menerima input data dan menghitung data
; yang masuk dari receiver infrared

Int_1
      CLR   ea
      PUSH  a
      PUSH  psw
      PUSH  tl0
      PUSH  th0
      MOV   Data_Counter,#0
      MOV   th0,#0
      MOV   tl0,#0
      SETB  tr0
      JNB   IR_RX,$
      CLR   tr0
      MOV   a,th0
      CJNE  a,#0Bh,I1_J2          ; cek apakah data yg masuk = SP ?
      CLR   Data_Type_F
      AJMP  I1_J5
I1_J2 CJNE  a,#0Dh,I1_J1          ; cek apakah data yg masuk = status kontrol
?
      SETB  Data_Type_F
I1_J5 MOV   th0,#0E0h
      MOV   tl0,#0
      CLR   tf0
      SETB  tr0
I1_J3 JB    tf0,I1_J4
      JB    IR_RX,I1_J3
      JNB   IR_RX,$
      INC   Data_Counter
      AJMP  I1_J5

I1_J4 DEC   Data_Counter
      CLR   tf0
      CLR   tr0

      JB    Data_Type_F,I1_J6
      MOV   Set_Point,Data_Counter
      SETB  Heater_Status
      SETB  Heater_F
      AJMP  I1_J1

I1_J6 SETB  Check_Ctrl_F
      MOV   Dummy_2,Data_Counter

I1_J1 CLR   ie1
      POP   th0
      POP   tl0
```

```
	POP	psw
	POP	a
	SETB	ea
	SETB	tr0
	RETI

; timer 1 digunakan untuk membangkitkan frekuensi 40 kHz (carrier)

Timer_1
	CPL	IR_TX
	RETI

;-----------
; Procedures
;-----------

; Ini adalah prosedur untuk setting timer, interrupt, dan nilai awal variabel

Initialize_Data
	MOV	tmod,#21h	; timer 0 -> timer 16 bit, timer 1 -> timer auto reload

	MOV	ie,#8Eh		; aktifkan interrupt 1, int. timer 0, int. timer 1

	SETB	it1		; interrupt 1 aktif low edge

	MOV	ip,#0Ch		; prioritaskan interrupt 1 dan int. timer 1

	MOV	th0,#03Ch	; timer 0 digunakan utk pewaktuan 50.000 us
	MOV	tl0,#0AFh	;

	MOV	th1,#0F4h	; timer 1 digunakan utk pewaktuan 25 us (periode dari 40
kHz)
	MOV	tl1,#0F4h	;

	MOV	Set_Point,#0	; nilai set point sementara diisi 0
	CLR	Heater		; matikan heater
	CLR	Heater_Status	; heater status = mati / off
	CLR	Upper_Valve ; status kran isi = tutup
	CLR	Lower_Valve ; status kran buang = tutup

	SETB	tr0		; nyalakan timer 0
	SETB	IR_TX		; matikan transmitter IR
	SETB	Read_ADC_F ; perintahkan prosedur Read_ADC utk membaca ADC
	MOV	Ctrl_Status,#0	; Status kontrol sementara diisi nilai 0
	RET

;----------------------------------------
; Div_16 : Routine untuk pembagian
; 32 bit : 16 bit -> 32 bit
;
;		MSB			LSB
; Pembagi  -> Num_Hi			Num_Lo
; Bilangan -> Div_3  Div_2  Div_1  Div_0
; Hasil    -> Div_3  Div_2  Div_1  Div_0
;----------------------------------------

Div_16:
```

```
        ;This divides the 32 bit OP register by the value supplied
            MOV     R7,#0
            MOV     R6,#0               ;zero out partial remainder
            MOV     Tmp_0,#0
            MOV     Tmp_1,#0
            MOV     Tmp_2,#0
            MOV     Tmp_3,#0
            MOV     R1,Num_Hi           ;load divisor
            MOV     R0,Num_Lo
            MOV     R5,#32              ;loop count

        ;This begins the loop
Div_loop:
        ACALL   Shift_D             ;shift the dividend and return MSB in C
            MOV     A,R6                ;shift carry into LSB of partial remainder
            RLC     A
            MOV     R6,A
            MOV     A,R7
            RLC     A
            MOV     R7,A
        JC      can_sub             ; Revisi tgl 20 okt 1998

        ;now test to see if R7:R6 >= R1:R0
            CLR     C
            MOV     A,R7                ;subtract R1 from R7 to see if R1 < R7
            SUBB    A,R1                ; A = R7 - R1, carry set if R7 < R1
            JC      Cant_sub

        ;at this point R7>R1 or R7=R1
            JNZ     Can_sub             ;jump if R7>R1

        ;if R7 = R1, test for R6>=R0
            CLR     C
            MOV     A,R6
            SUBB    A,R0                ; A = R6 - R0, carry set if R6 < R0
            JC      Cant_sub
Can_sub:
        ;subtract the divisor from the partial remainder
            CLR     C
            MOV     A,R6
            SUBB    A,R0                ; A = R6 - R0
            MOV     R6,A
            MOV     A,R7
            SUBB    A,R1                ; A = R7 - R1 - Borrow
            MOV     R7,A
            SETB    C                   ; shift a 1 into the quotient
            AJMP    Quot
Cant_sub:
        ;shift a 0 into the quotient
            CLR     C
Quot:
        ;shift the carry bit into the quotient
            ACALL   Shift_Q

        ; Test for competion
            DJNZ    R5,Div_loop
```

```
        ; Now we are all done, move the TMP values back into OP
            MOV     Div_0,Tmp_0
            MOV     Div_1,Tmp_1
            MOV     Div_2,Tmp_2
            MOV     Div_3,Tmp_3
            RET

Shift_D:
        ;shift the dividend one bit to the left and return the MSB in C
            CLR     C
            MOV     A,Div_0
            RLC     A
            MOV     Div_0,A
            MOV     A,Div_1
            RLC     A
            MOV     Div_1,A
            MOV     A,Div_2
            RLC     A
            MOV     Div_2,A
            MOV     A,Div_3
            RLC     A
            MOV     Div_3,A
            RET

Shift_Q:
        ;shift the quotent one bit to the left and shift the C into LSB
            MOV     A,Tmp_0
            RLC     A
            MOV     Tmp_0,A
            MOV     A,Tmp_1
            RLC     A
            MOV     Tmp_1,A
            MOV     A,Tmp_2
            RLC     A
            MOV     Tmp_2,A
            MOV     A,Tmp_3
            RLC     A
            MOV     Tmp_3,A
            RET

; prosedur untuk start konversi dan membaca hasil konversi ADC

Read_ADC
      JNB    Read_ADC_F,RADC_J1       ; kalau Read_ADC_F = 0, jangan lakukan
                                      ; pembacaan ADC
      CLR    Read_ADC_F
      CLR    SOC                      ; start konversi
      MOV    r7,#50                       ;
      DJNZ   r7,$                     ;
      SETB   SOC                      ;

      CLR    ea                       ; matikan semua interrupt
      JB     EOC,$                    ; tunggu sampai selesai konversi
      SETB   ea                       ; nyalakan interrupt

      MOV    a,p1                     ; baca data ADC dari port 1
```

```
        MOV    b,#100                      ; data ADC adalah 0 s/d 255,
                                     ; untuk mengubahnya menjadi suhu
                                     ; digunakan persamaan :
                                     ;        (Data_ADC x 100)
                                     ; suhu = ----------------
                                     ;              255
        MUL    ab
        MOV    Div_0,a
        MOV    Div_1,b
        MOV    Div_2,#0
        MOV    Div_3,#0
        MOV    Num_Lo,#255
        MOV    Num_Hi,#0
        LCALL  Div_16
        MOV    Present_Value,Div_0
RADC_J1        RET

; prosedur untuk mengisi nilai variabel kontrol status yg akan dikirimkan
; ke kontroler 2 dengan melakukan pengecekan sensor level air dan bit-bit
; indicator

Check_Ctrl_Status
        MOV    Dummy,#0
        MOV    Tank_Status,#0
        JNB    L_Level,CCS_J5
        MOV    Dummy,#4
        MOV    Tank_Status,#1
        JNB    U_Level,CCS_J5
        MOV    Dummy,#12
        MOV    Tank_Status,#2
CCS_J5
        JB     Upper_Valve,CCS_J1
        ANL    Dummy,#0FEh
        AJMP   CCS_J3
CCS_J1         ORL    Dummy,#1
CCS_J3         JB     Lower_Valve,CCS_J2
        ANL    Dummy,#0FDh
        AJMP   CCS_J4
CCS_J2         ORL    Dummy,#2
CCS_J4         JB     Heater_Status,CCS_J6
        ANL    Dummy,#0EFh
        AJMP   CCS_J7
CCS_J6         ORL    Dummy,#10h
CCS_J7
        MOV    Ctrl_Status,Dummy
        RET

; prosedur untuk kontrol heater secara otomatis

Check_Heater
        JB     Heater_F,CH_J1          ; apakah boleh melakukan kontrol heater ?
        RET
CH_J1   CLR    Heater_F
        JB     Heater_Status,CH_J2     ; apakah status heater stop / aktif ?
        RET                            ; kalau aktif, lakukan pengecekan suhu
CH_J2   MOV    a,Present_Value
        MOV    b,Set_Point
```

```
        CJNE   a,b,CH_J3          ; apakah suhu sekarang = set point ?

CH_J4   CLR    Heater                   ; kalau sama, matikan
        RET
CH_J3   JNC    CH_J4              ; kalau lebih besar, matikan

        SETB   Heater                   ; kalau lebih kecil, nyalakan
        RET

; prosedur untuk membuka kran isi

Open_Upper_Valve
        CLR    ea
        CLR    tr0
        SETB   U_Valve_1          ; nyalakan motor
        CLR    U_Valve_2          ;

        MOV    r7,#200                  ;
OUV_J2         MOV    r6,#250                ;
OUV_J1         MOV    r5,#20                 ; Ini adalah delay lama motor
        DJNZ   r5,$               ; berputar
        DJNZ   r6,OUV_J1          ;
        DJNZ   r7,OUV_J2          ;

        SETB   U_Valve_1          ; matikan motor
        SETB   U_Valve_2          ;
        CLR    ie1
        SETB   tr0
        SETB   ea
        RET

; prosedur untuk menutup kran isi

Close_Upper_Valve
        CLR    ea
        CLR    tr0
        CLR    U_Valve_1          ; nyalakan motor
        SETB   U_Valve_2          ;

        MOV    r7,#200                  ;
CUV_J2         MOV    r6,#250                ;
CUV_J1         MOV    r5,#20                 ; Ini adalah delay lama motor
        DJNZ   r5,$               ; berputar
        DJNZ   r6,CUV_J1          ;
        DJNZ   r7,CUV_J2          ;

        SETB   U_Valve_1          ; matikan motor
        SETB   U_Valve_2          ;
        CLR    ie1
        SETB   tr0
        SETB   ea
        RET

; prosedur untuk membuka kran buang

Open_Lower_Valve
        CLR    ea
```

```
      CLR   tr0
      SETB  L_Valve_1          ; nyalakan motor
      CLR   L_Valve_2          ;

      MOV   r7,#200                  ;
OLV_J2      MOV   r6,#250                  ;
OLV_J1      MOV   r5,#20                   ; Ini adalah delay lama motor
      DJNZ  r5,$               ; berputar
      DJNZ  r6,OLV_J1          ;
      DJNZ  r7,OLV_J2          ;

      SETB  L_Valve_1          ; matikan motor
      SETB  L_Valve_2          ;
      CLR   ie1
      SETB  tr0
      SETB  ea
      RET

; prosedur untuk menutup kran buang

Close_Lower_Valve
      CLR   ea
      CLR   tr0
      CLR   L_Valve_1          ; nyalakan motor
      SETB  L_Valve_2          ;

      MOV   r7,#200                  ;
CLV_J2      MOV   r6,#250                  ;
CLV_J1      MOV   r5,#20                   ; Ini adalah delay lama motor
      DJNZ  r5,$               ; berputar
      DJNZ  r6,CLV_J1          ;
      DJNZ  r7,CLV_J2          ;

      SETB  L_Valve_1          ; matikan motor
      SETB  L_Valve_2          ;
      CLR   ie1
      SETB  tr0
      SETB  ea
      RET

; prosedur pengecekan / pengontrol pembukaan / penutupan kran secara otomatis

Valve_Ctrl
      MOV   a,Tank_Status
      CJNE  a,#0,VC_J1         ; kalau air kosong, lakukan :
      CLR   Heater_Status             ;
      CLR   Heater                    ; 1. matikan heater
      JNB   Lower_Valve,VC_J2         ; 2. tutup kran buang (kalau masih terbuka)
      CLR   Lower_Valve        ; 3. buka kran isi (kalau tertutup)
      LCALL Close_Lower_Valve
VC_J2 JB    Upper_Valve,VC_J3
      SETB  Upper_Valve
      LCALL Open_Upper_Valve
VC_J3 RET

VC_J1 CJNE  a,#2,VC_J3
      JNB   Upper_Valve,VC_J3
```

```
        CLR   Upper_Valve
        LCALL Close_Upper_Valve
        RET

; prosedur pengecekan / pengontrol pembukaan / penutupan kran
; yang dikontrol manual dari kontroler 2

Check_Valve_Ctrl
        JB    Check_Ctrl_F,CVC_J1      ; apakah ada pengontrolan manual ?
        RET                            ; (ada data kontrol status yg masuk)
CVC_J1        CLR   Check_Ctrl_F
        MOV   a,Dummy_2
        ANL   a,#1
        CJNE  a,#1,CVC_J2
        JB    Upper_Valve,CVC_J3       ; buka kran isi
        SETB  Upper_Valve
        LCALL Open_Upper_Valve
        AJMP  CVC_J3
CVC_J2        CJNE  a,#0,CVC_J3
        JNB   Upper_Valve,CVC_J3       ; tutup kran isi
        CLR   Upper_Valve
        LCALL Close_Upper_Valve

CVC_J3        MOV   a,Dummy_2
        ANL   a,#2
        CJNE  a,#2,CVC_J4
        JB    Lower_Valve,CVC_J5       ; buka kran buang
        SETB  Lower_Valve
        LCALL Open_Lower_Valve
        AJMP  CVC_J5
CVC_J4        CJNE  a,#0,CVC_J5
        JNB   Lower_Valve,CVC_J5       ; tutup kran buang
        CLR   Lower_Valve
        LCALL Close_Lower_Valve
CVC_J5
        RET

;-------------
; Main Program
;-------------

Start
        LCALL Initialize_Data

Loop
        LCALL Read_ADC
        LCALL Check_Ctrl_Status
        LCALL Check_Heater
        LCALL Valve_Ctrl
        LCALL Check_Valve_Ctrl
        AJMP  Loop
```

# LAMPIRAN C

## 2.4 Instruction Outline

Table 5 List of instructions

| Instruction | Code RS | R/W | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | Function | Execution time |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| (1) Display clear | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | Clears all display and returns cursor to home position (address 0) | 1.64 ms |
| (2) Cursor Home | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | * | Returns cursor to home position. Shifted display returns to home position and DD RAM contents do not change. | 1.64 ms |
| (3) Entry Mode Set | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | I/D | S | Sets direction of cursor movement and whether display will be shifted when data is written or read | 40 µs |
| (4) Display ON / OFF control | 0 | 0 | 0 | 0 | 0 | 0 | 1 | D | C | B | Turns ON/OFF total display (D) and cursor (C), and makes cursor position column start blinking (B) | 40 µs |
| (5) Cursor/Display Shift | 0 | 0 | 0 | 0 | 0 | 1 | S/C | R/L | * | * | Moves cursor and shifts display without changing DD RAM contents | 40 µs |
| (6) Function Set | 0 | 0 | 0 | 0 | 1 | DL | 1 | * | * | * | Sets interface data length (DL) | 40 µs |
| (7) CG RAM Address Set | 0 | 0 | 0 | 1 | $A_{CG}$ | | | | | | Sets CG RAM address to start transmitting or receiving CG RAM data | 40 µs |
| (8) DD RAM Address Set | 0 | 0 | 1 | $A_{DD}$ | | | | | | | Sets DD RAM address to start transmitting or receiving DD RAM data | 40 µs |
| (9) BF/Address Read | 0 | 1 | BF | AC | | | | | | | Reads BF indicating module in internal operation and AC contents (used for both CG RAM and DD RAM) | 0 µs |
| (10) Data Write to CG RAM or DD RAM | 1 | 0 | Write Data | | | | | | | | Writes data into DD RAM or CG RAM | 40 µs |
| (11) Data Read from CG RAM or DD RAM | 1 | 1 | Read Data | | | | | | | | Reads data from DD RAM or CG RAM | 40 µs |

* : Invalid bit
$A_{CG}$ : CG RAM address
$A_{DD}$ : DD RAM address

I/D = 1 : Increment
I/D = 0 : Decrement

S = 1 : Display shift
S = 0 : No display shift

D = 1 : Display ON
D = 0 : Display OFF

C = 1 : Cursor ON
C = 0 : Cursor OFF

B = 1 : Blink ON
B = 0 : Blink OFF

S/C = 1 : Display shift
S/C = 0 : Cursor movement

R/L = 1 : Right shift
R/L = 0 : Left shift

DL = 1 : 8 bits
DL = 0 : 4 bits

BF = 1 : Internal operation in progress
BF = 0 : Instruction can be accepted

Table 3 Correspondence between character codes and character patterns

| Lower bit 4 bit \ Upper bit 4 bit | 0000 | 0010 | 0011 | 0100 | 0101 | 0110 | 0111 | 1010 | 1011 | 1100 | 1101 | 1110 | 1111 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ××××0000 | CG RAM (1) | | 0 | @ | P | ` | p | | ー | タ | ミ | α | p |
| ××××0001 | (2) | ! | 1 | A | Q | a | q | 。 | ア | チ | ム | ä | q |
| ××××0010 | (3) | " | 2 | B | R | b | r | 「 | イ | ツ | メ | β | θ |
| ××××0011 | (4) | # | 3 | C | S | c | s | 」 | ウ | テ | モ | ε | ∞ |
| ××××0100 | (5) | $ | 4 | D | T | d | t | 、 | エ | ト | ヤ | μ | Ω |
| ××××0101 | (6) | % | 5 | E | U | e | u | ・ | オ | ナ | ユ | σ | ü |
| ××××0110 | (7) | & | 6 | F | V | f | v | ヲ | カ | ニ | ヨ | ρ | Σ |
| ××××0111 | (8) | ' | 7 | G | W | g | w | ァ | キ | ヌ | ラ | g | π |
| ××××1000 | (1) | ( | 8 | H | X | h | x | ィ | ク | ネ | リ | √ | x̄ |
| ××××1001 | (2) | ) | 9 | I | Y | i | y | ゥ | ケ | ノ | ル | ⁻¹ | y |
| ××××1010 | (3) | * | : | J | Z | j | z | ェ | コ | ハ | レ | j | 千 |
| ××××1011 | (4) | + | ; | K | [ | k | { | ォ | サ | ヒ | ロ | ˣ | 万 |
| ××××1100 | (5) | , | < | L | ¥ | l | \| | ャ | シ | フ | ワ | ¢ | 円 |
| ××××1101 | (6) | - | = | M | ] | m | } | ュ | ス | ヘ | ン | £ | ÷ |
| ××××1110 | (7) | . | > | N | ^ | n | → | ョ | セ | ホ | ゛ | ñ | |
| ××××1111 | (8) | / | ? | O | _ | o | ← | ッ | ソ | マ | ゜ | ö | █ |

# BIODATA

# BIODATA

| | |
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